```
.section .vectors, "ax"
 2
                                                  // reset vector
                             start
                             SERVICE UND
 3
                                                 // undefined instruction vector
                     В
                                                 // software interrupt vector
 4
                             SERVICE SVC
                     В
                                                 // aborted prefetch vector // aborted data vector
 5
                     В
                             SERVICE ABT INST
                             SERVICE ABT_DATA
 6
 7
                     .word
                             0
                                                  // unused vector
                             SERVICE IRQ
8
                                                 // IRQ interrupt vector
                     В
9
                             SERVICE FIQ
                     В
                                                  // FIQ interrupt vector
10
                     .text
                     .global start
11
12
      start:
     \overline{/*} Set up stack pointers for IRQ and SVC processor modes */
13
                                               // interrupts masked, MODE = IRQ
                             R1, #0b11010010
14
                     MOV
                                                  // change to IRQ mode
15
                     MSR
                             CPSR c, R1
16
                             SP, =0xFFFFFFFF - 3 // set IRQ stack to A9 onchip memory
                     LDR
17
                                                  // interrupts masked, MODE = SVC
18
                     MOV
                             R1, #0b11010011
19
                     MSR
                             CPSR, R1
                                                  // change to supervisor mode
20
                             SP, =0x3FFFFFFF - 3 // set SVC stack to top of DDR3 memory
                     LDR
21
22
                     BL
                             CONFIG GIC
                                                  // configure the ARM generic interrupt
                     controller
23
                     RT.
                             CONFIG TIMER
                                                 // configure the Interval Timer
24
                     BL
                             CONFIG KEYS
                                                  // configure the pushbutton KEYs port
25
26
    /* Enable IRQ interrupts in the ARM processor */
                              RO, \#0b01010011 // IRQ unmasked, MODE = SVC
27
                     MOV
                              CPSR c, R0
28
                     MSR
29
30
                                                 // LEDR base address
                     LDR
                             R5, =0xFF200000
31
  LOOP:
32
                     LDR
                             R3, COUNT
                                                 // global variable
                                                 // write to the LEDR lights
33
                     STR
                             R3, [R5]
34
                     R
                             LOOP
35
36
     /* Configure the Interval Timer to create interrupts at 0.25 second intervals */
37
     CONFIG TIMER:
                   LDR
                          RO, =0xFF202000 // FPGA timer base address
38
                     LDR
                             R1, = 30784
39
                     STR
                             R1, [R0, #8]
                                                  // Set lower bits of timer
40
                     LDR
                             R1, =381
                                                 // Set upper bits of timer
41
                     STR
                             R1, [R0, #12]
42
                     VOM
                             R1, #0b0111
                                                 // Control register bits
43
                     STR
                             R1, [R0, #4]
                                                 // Start timer, set auto-reload and enable
                     interrupts
44
                     ВХ
                             LR
45
46
     /* Configure the pushbutton KEYS to generate interrupts */
47
     CONFIG_KEYS:
48
                             R0, =0 \times FF200050
                                                 // KEY address
                     LDR
49
                     VOM
                             R1, #0xF
                                                 // set interrupt mask bits
50
                     STR
                             R1, [R0, #0x8]
                                                 // interrupt mask register (base + 8)
51
                     ВХ
                             LR
52
53
    /* Define the exception service routines */
54
     SERVICE IRQ:
                     PUSH
                             \{R0-R7, LR\}
55
                     LDR
                             R4, =0xFFFEC100
                                                 // GIC CPU interface base address
56
                                                 // read the ICCIAR in the CPU interface
                     LDR
                             R5, [R4, #0x0C]
57
58
     FPGA IRQ1 HANDLER:
59
                             R5, #73
                     CMP
                                                  // check the interrupt ID
60
                     BEO
                             KEY INTERRUPT
61
                     CMP
                             R5, #72
62
                             CLK INTERRUPT
                     BEQ
63
64
    UNEXPECTED:
                     В
                             UNEXPECTED
                                                // if not recognized, stop here
65
    KEY INTERRUPT: BL
                             KEY ISR
     CLK_INTERRUPT: BL
66
                             TIMER ISR
```

67

```
68
      EXIT IRO:
                      STR
                              R5, [R4, #0x10] // write to the End of Interrupt Register
      (ICCEOIR)
 69
                      POP
                              \{R0-R7, LR\}
 70
                              PC, LR, #4
                                                  // return from exception
                      SUBS
 71
      /* Check if it has been 0.25 seconds and adds RUN to COUNT */
 72
 73
                              RO, =0xFF202000 // base address of FPGA timer
      TIMER ISR:
                      LDR
 74
                      LDR
                              R1, [R0] // read edge capture register
 75
                      MOV
                              R2, #0
 76
                      STR
                              R2, [R0]
                                                  // clear the interrupt
 77
                      LDR
                              R0, =RUN
                                                  // Load RUN toggle
 78
                              R0, [R0]
                      LDR
 79
                      LDR
                              R1, =COUNT
                                                  // Load counter
                              R2, [R1]
 80
                      LDR
                              R2, R0
                                                  // Increment counter by RUN
 81
                      ADD
                                                  // Store incremented counter
 82
                      STR
                              R2, [R1]
                                                  // Return
 83
     END_TIMER_ISR: BX
                              LR
 84
 85
      /* Check if a key has been pressed and toggles RUN */
 86
                              R0, =0xFF200050
                                                  // base address of pushbutton KEY port
     KEY ISR:
                      LDR
 87
                              R1, [R0, #0xC]
                      LDR
                                                  // read edge capture register
 88
                      VOM
                              R2, \#0xF
 89
                      STR
                              R2, [R0, #0xC]
                                                  // clear the interrupt
 90
                              R0, =RUN
                      LDR
                                                  // Address of RUN toggle
 91
                              R3, #0b1111
 92
      CHECK KEYS:
                      MOV
 93
                              R3, R1
                      ORRS
                                                  // Check for any KEY
                              END KEY_ISR
 94
                      BEO
 95
                      LDR
                              R1, [R0]
                                                  // Get RUN from memory
 96
                      EOR
                              R1, #1
                                                  // Toggle RUN
 97
                      STR
                              R1, [R0]
                                                  // Set RUN in memory
 98
 99
     END KEY ISR:
                      BX
                              LR
                                                  // Return
100
101
     /* Global variables */
102
                      .global COUNT
103
     COUNT:
                            0 \times 0
                                             // used by timer
                      .word
104
                      .global RUN
                                                  // used by pushbutton KEYs
105
     RUN:
                      .word
                            0x1
                                                  // initial value to increment COUNT
106
107
                      .end
```

108