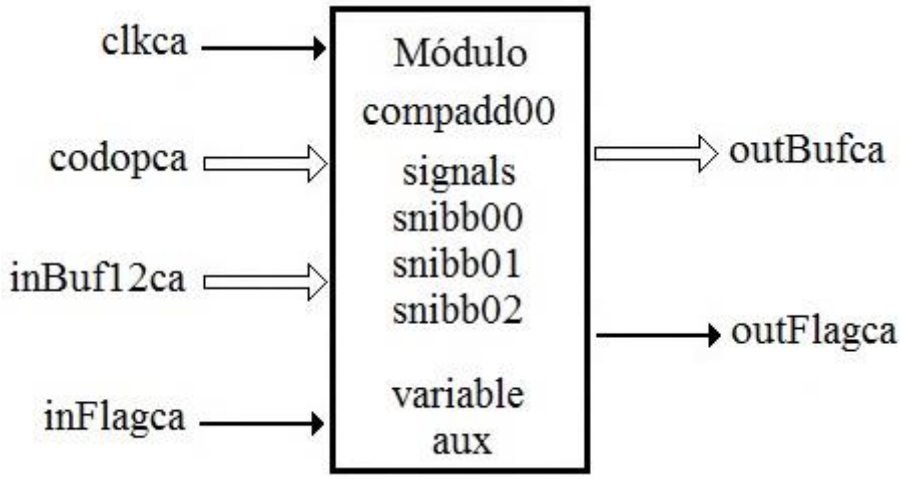
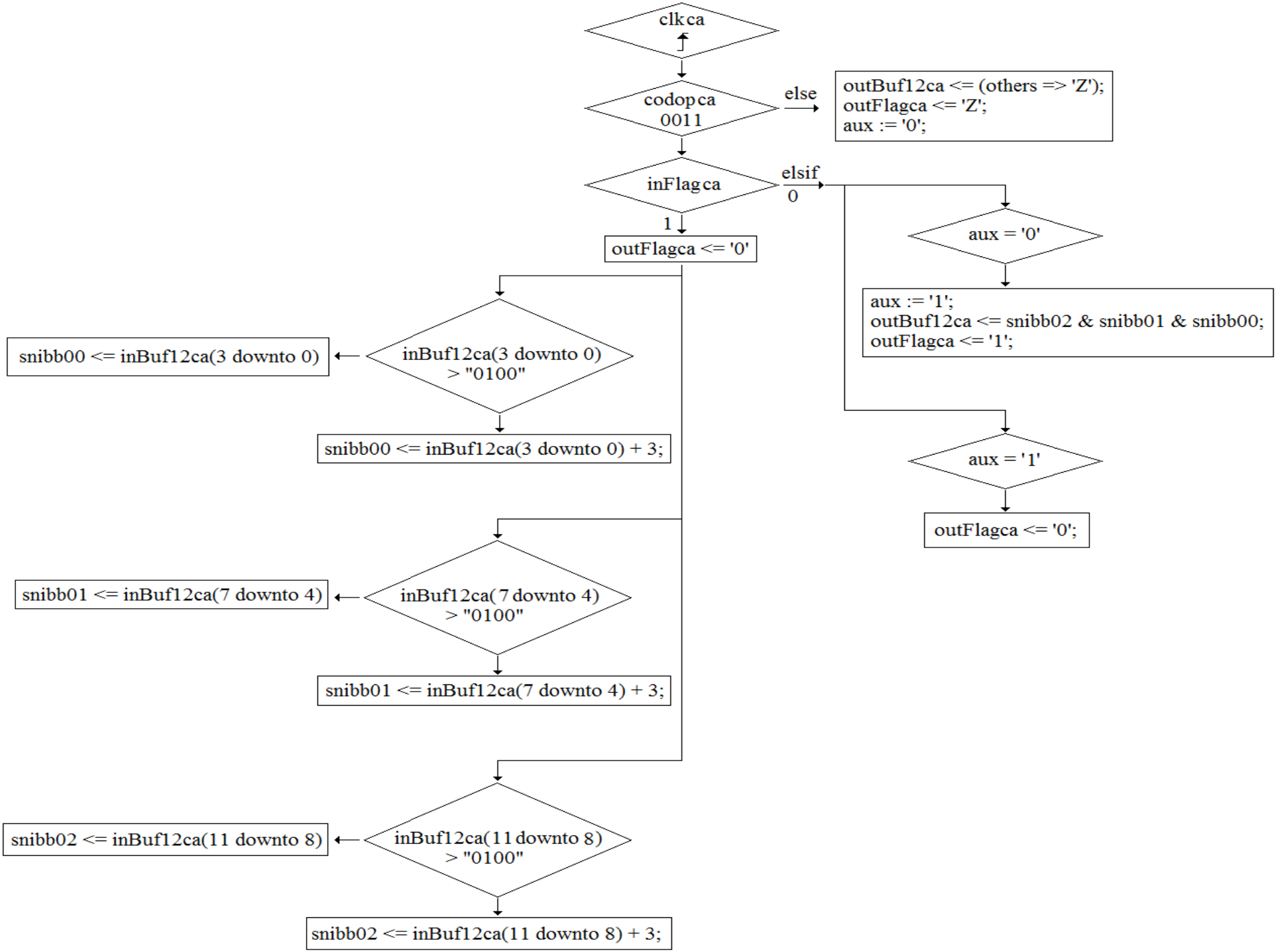
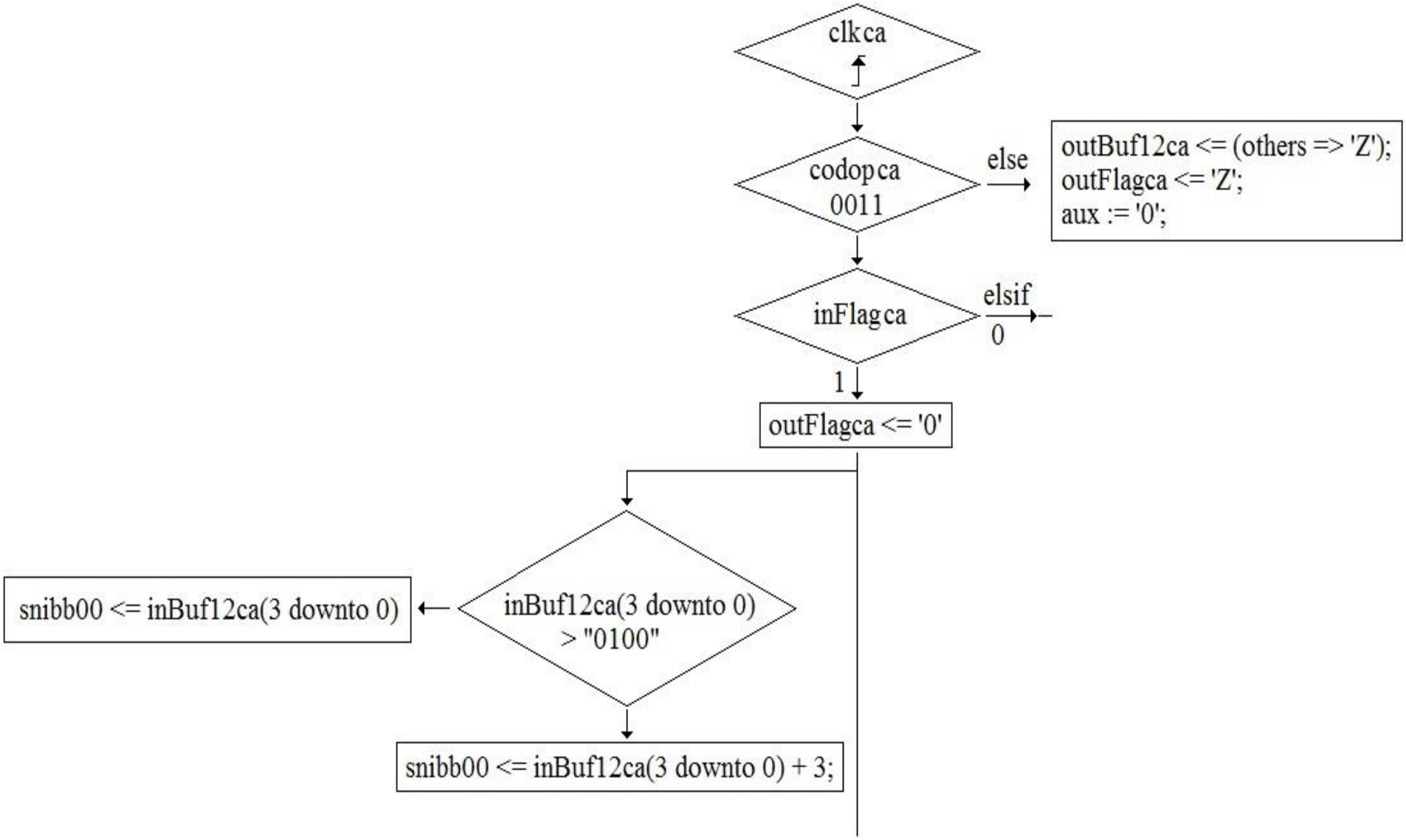
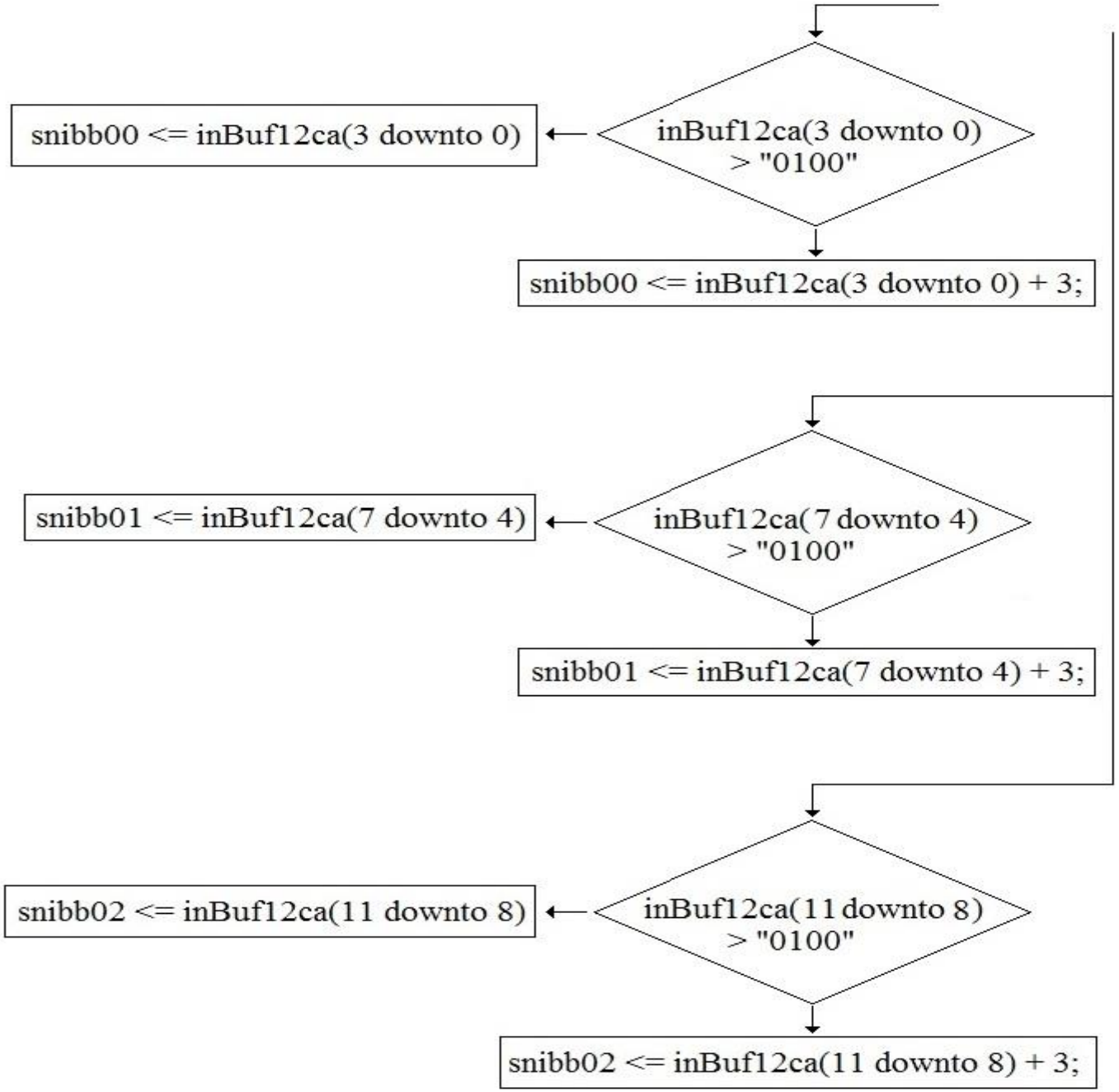
Entidad y Diagrama de Flujo para la implementación del Código VHDL del circuito correspondiente a la instrucción “compadd00”




clkca
codopca
0011
else
outBuf12ca <= (others => 'Z');
outFlagca <= 'Z';
aux := '0';
inFlagca
elsif
0
1
outFlagca <= '0'
aux = '0'
aux := '1';
outBuf12ca <= snibb02 & snibb01 & snibb00;
outFlagca <= '1';
aux = '1'
outFlagca <= '0';
inBuf12ca(3 downto 0)
> "0100"
snibb00 <= inBuf12ca(3 downto 0)
snibb00 <= inBuf12ca(3 downto 0) + 3;
inBuf12ca(7 downto 4)
> "0100"
snibb01 <= inBuf12ca(7 downto 4)
snibb01 <= inBuf12ca(7 downto 4) + 3;
inBuf12ca(11 downto 8)
> "0100"
snibb02 <= inBuf12ca(11 downto 8)
snibb02 <= inBuf12ca(11 downto 8) + 3;


clkca
codopca
0011
else
outBuf12ca <= (others => 'Z');
outFlagca <= 'Z';
aux := '0';
inFlagca
elsif
0
1
outFlagca <= '0'
inBuf12ca(3 downto 0)
> "0100"
snibb00 <= inBuf12ca(3 downto 0)
snibb00 <= inBuf12ca(3 downto 0) + 3;


inBuf12ca(3 downto 0)
> "0100"
snibb00 <= inBuf12ca(3 downto 0)
snibb00 <= inBuf12ca(3 downto 0) + 3;
inBuf12ca(7 downto 4)
> "0100"
snibb01 <= inBuf12ca(7 downto 4)
snibb01 <= inBuf12ca(7 downto 4) + 3;
inBuf12ca(11 downto 8)
> "0100"
snibb02 <= inBuf12ca(11 downto 8)
snibb02 <= inBuf12ca(11 downto 8) + 3;