SOC Design Laboratory, 2023 Fall

Report

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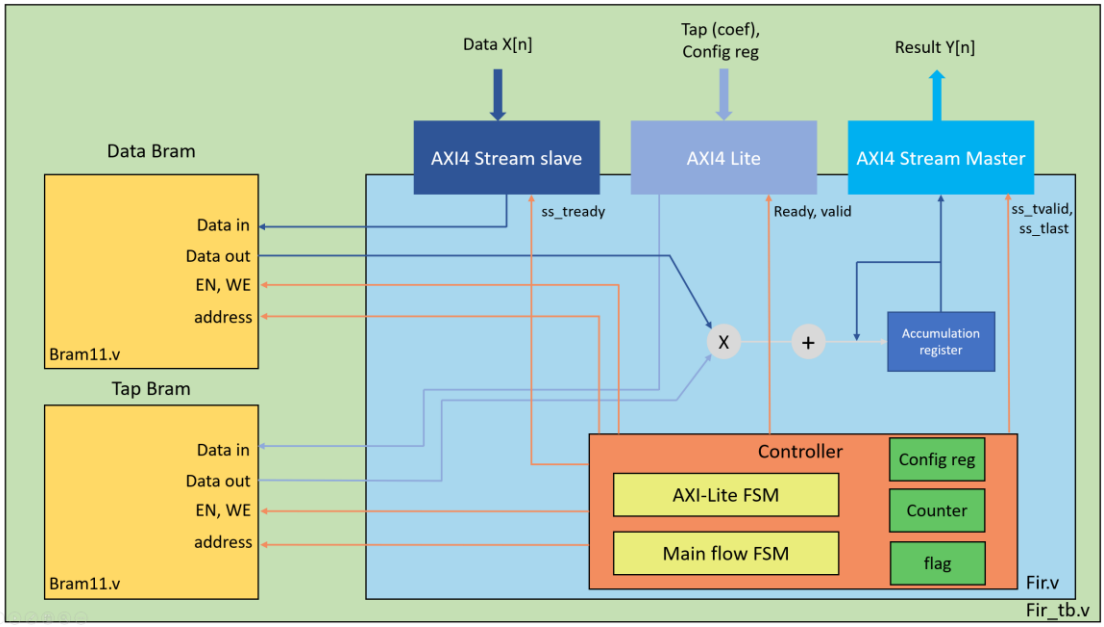
Overview

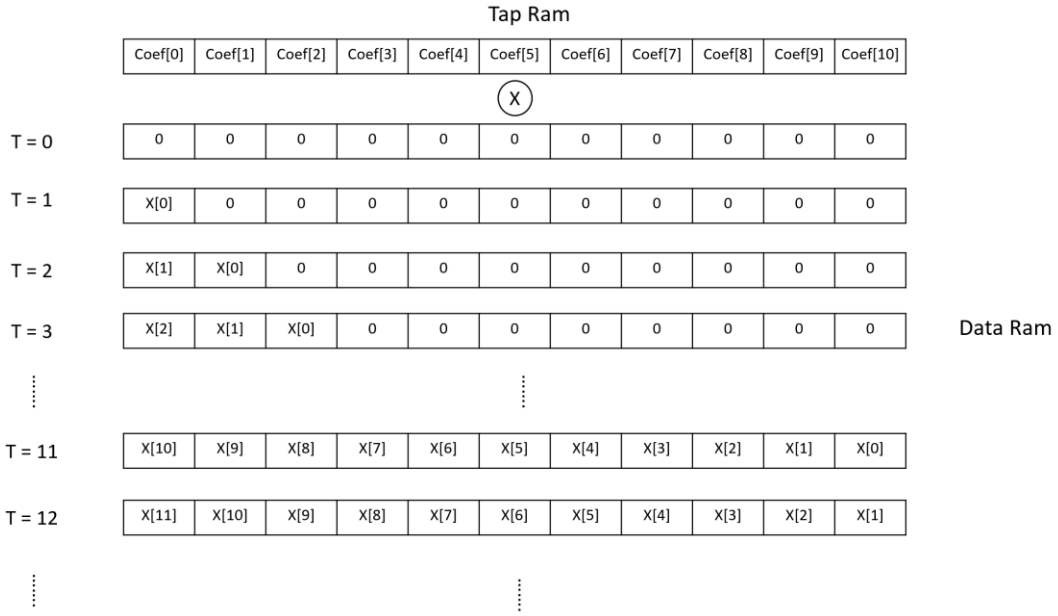
此次 Lab 需求為人工撰寫的 FIR (Finite impulse response) filter RTL design，module 所定義的 interface 為 AXI4-Lite, AXI4-Stream，另外實做細節規定使用一個乘法器和一個加法器， Shift register 則需使用 Block ram 代替。

Block diagram



FIR filter computation

此次 Lab 需要用到用 Bram implement 的 data & tap register，其中計算過程中會需要大量對 data ram 做 shift，以下詳細的運算流程。



實際計算只需將 data ram 和 tap ram 對應 address 的值相乘並累加後則可求得該 stream in x[n] 的 Y[n]。算完一個 Y[n]後依序從 data ram addr = 10 -> 0 shift in 後則可做新一輪的計算。

Resource usage

LUT and Flip Flop

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	237	0	0	53200	0.45
LUT as Logic	237	0	0	53200	0.45
LUT as Memory	0	0	0	17400	0.00
Slice Registers	136	0	0	106400	0.13
Register as Flip Flop	96	0	0	106400	0.09
Register as Latch	40	0	0	106400	0.04
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

Block RAM

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

Timing Report

合成的 cycle time 設定依序為 10->8->6->4ns，timing report 如下:

Timing summary

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.103 ns	Worst Hold Slack (WHS):	0.153 ns	Worst Pulse Width Slack (WPWS):	1.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	149	Total Number of Endpoints:	149	Total Number of Endpoints:	97

All user specified timing constraints are met.

Max delay path

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Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             0.103ns  (required time - arrival time)
  Source:                 sm_tdata_reg_reg[1]/C
                            (rising edge-triggered cell FDRE clocked by axis_clk  {rise@0.000ns fall@2.000ns period=4.000ns})
  Destination:            sm_tdata_reg_reg[31]/D
                            (rising edge-triggered cell FDRE clocked by axis_clk  {rise@0.000ns fall@2.000ns period=4.000ns})
  Path Group:             axis_clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            4.000ns  (axis_clk rise@4.000ns - axis_clk rise@0.000ns)
  Data Path Delay:        3.761ns  (logic 2.646ns (70.354%)  route 1.115ns (29.646%))
  Logic Levels:           10  (CARRY4=8 LUT2=2)
  Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    2.128ns = ( 6.128 - 4.000 )
    Source Clock Delay      (SCD):    2.456ns
    Clock Pessimism Removal (CPR):    0.184ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns
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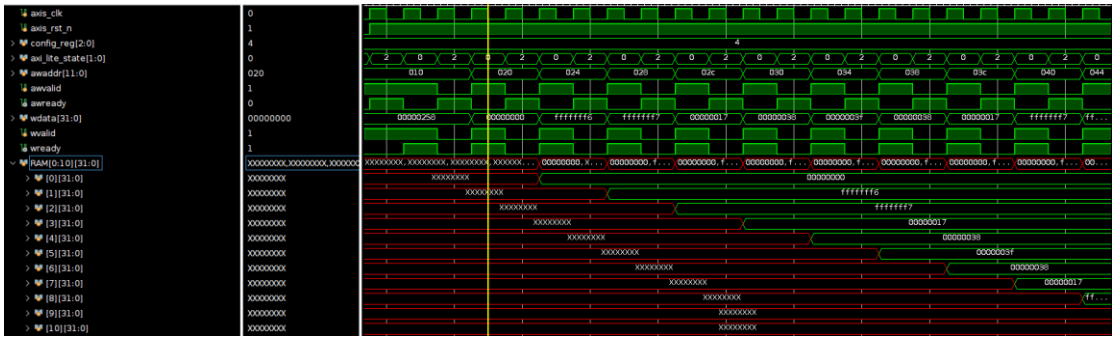
如圖中可觀察到，max delay path 為計算 FIR 結果的累加暫存器，由於需經過乘法與加法的 combinational 電路，因此相對整個 design 而言是 critical path。

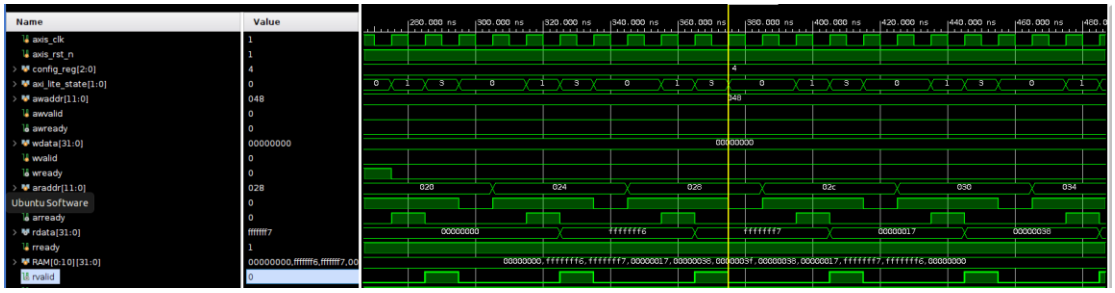
Simulation waveform

data length & Tap coefficient write



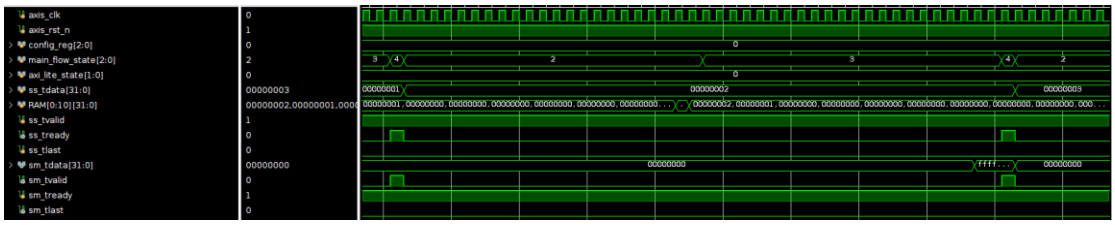
Config register 和 Tap coefficient 由 AXI-Lite interface 輸入，每當 wready = 1，Testbench 會在下個 cycle 輸入一筆新的資料。

Coefficient read check



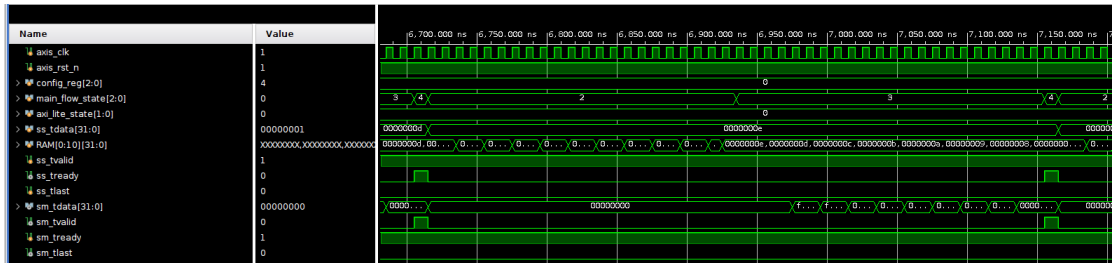
透過 FSM 控制，先從 Tap Ram 對取出對應的 coefficient 再透過 AXI Lite interface 輸出，當 rvalid = 1 時，testbench 可從 rdata 讀取出 coefficient。

Data stream in & Data Ram write



Data stream in，當 ss_tready = 時，testbench 會輸入下一筆 data 做後續 data shift。

Data stream out



Fir result stream out，當 sm_tvalid = 1 時，testbench 可將 sm_tdata 的結果和 golden value 進行比對。