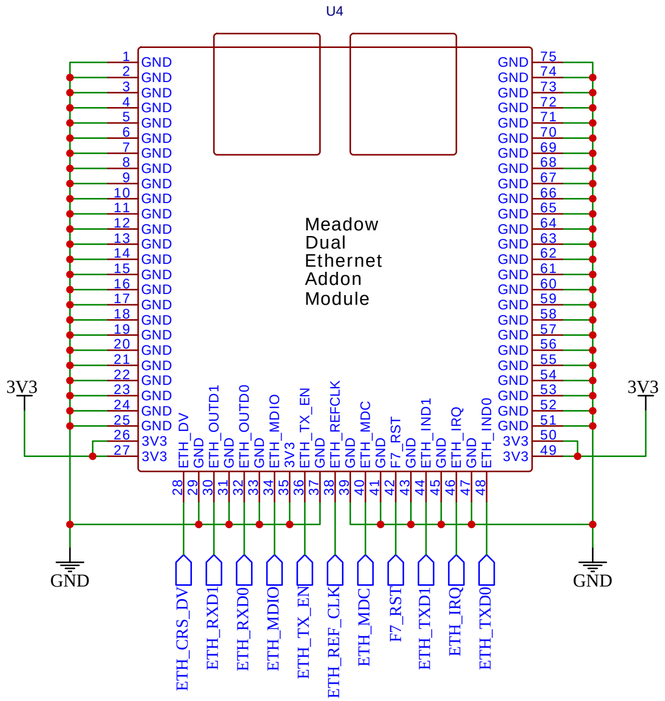

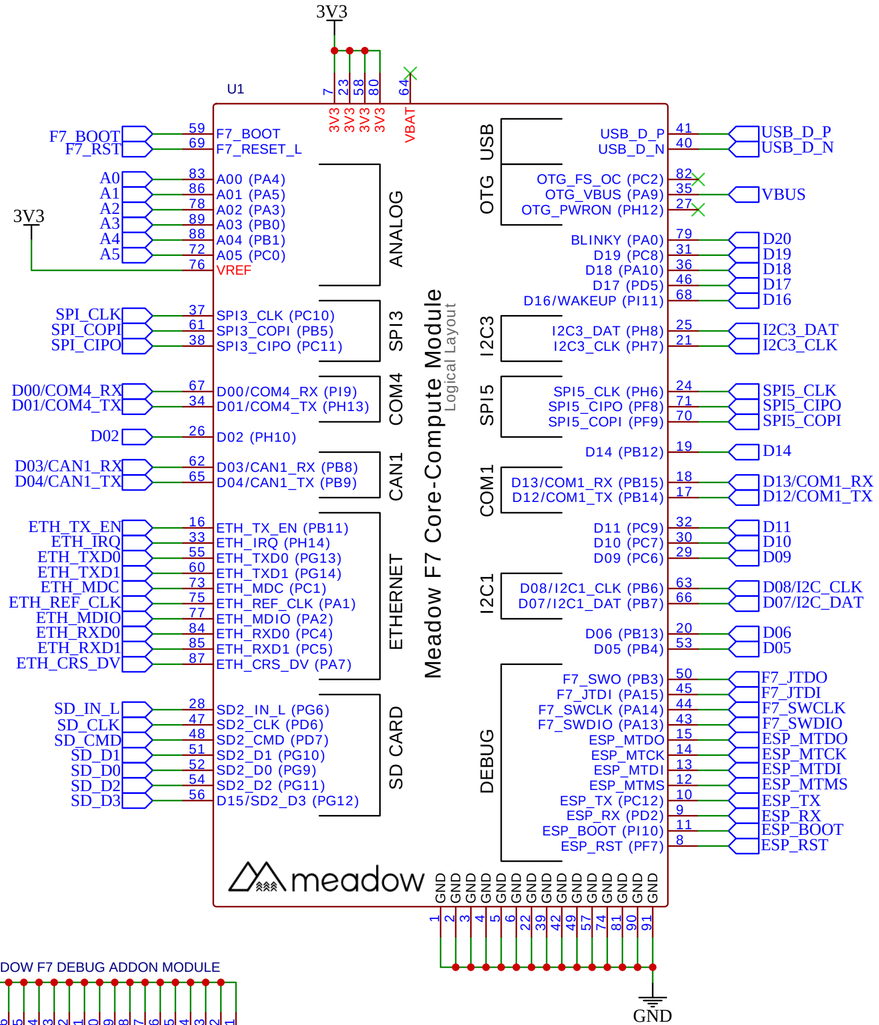

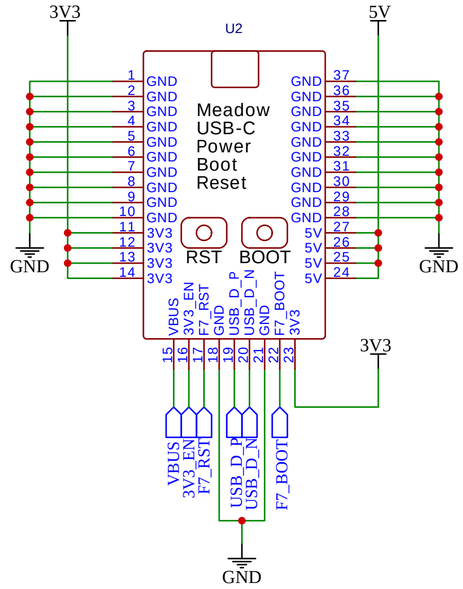

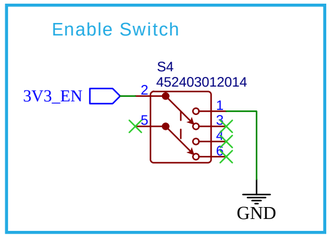

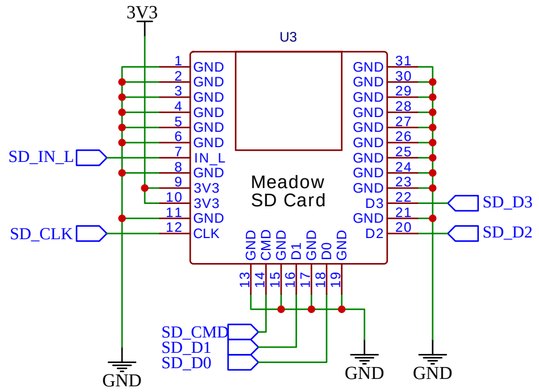

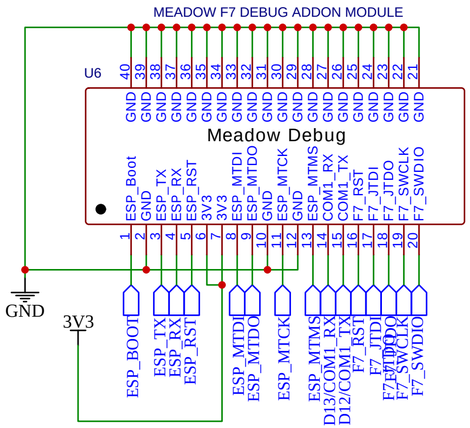

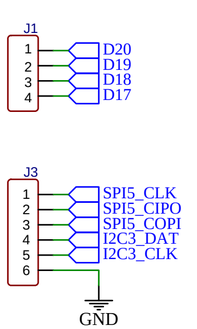

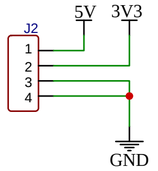

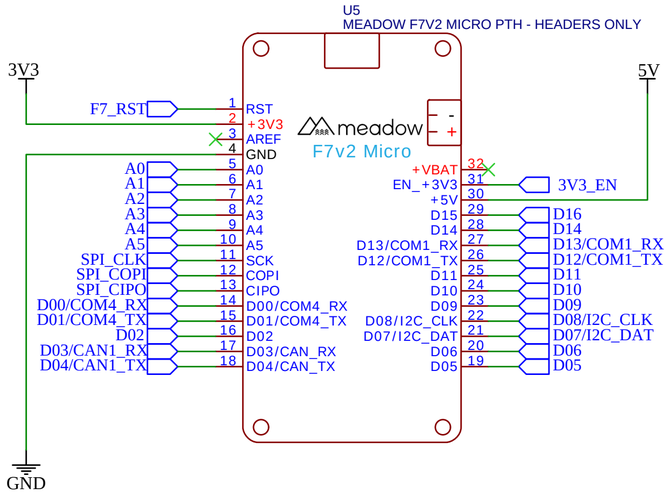


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Stackup/Controlled Impedance:
 SD Signals: 50Ω
    Outer layer: 0.29mm width
    Inner layer: 0.23mm width
 USB: 90Ω Diff Pair
    Outer layer: 0.19mm width, 0.11mm spacing
    Inner layer: 0.13mm width, 0.11mm spacing
 MCU -> PHY - 50Ω Single-Ended
    Outer layer: 0.29mm width, 0.127mm spacing
    Inner layer: 0.24mm width, 0.127mm spacing
 JLCPCB Stackup: JLC7628
```

TITLE: Core-Compute Dev Breakout w/Ethernet		REV: v1.d
	Company: Wilderness Labs	Sheet: 1/1
	Date: 2022-07 Drawn By: bryan costanich	