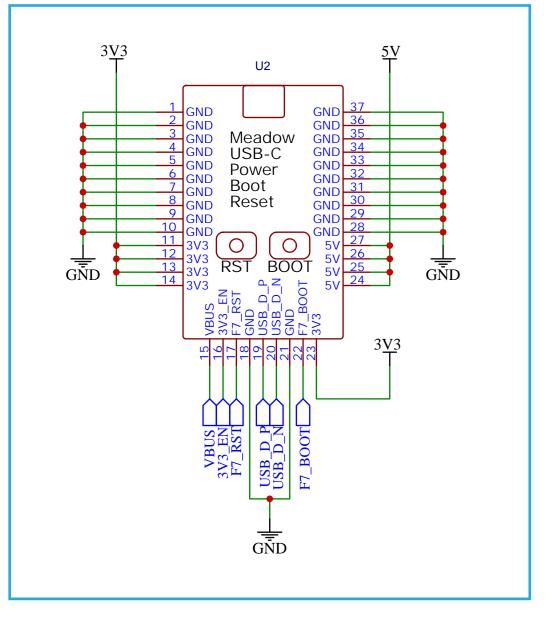
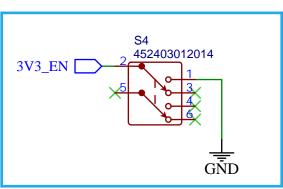


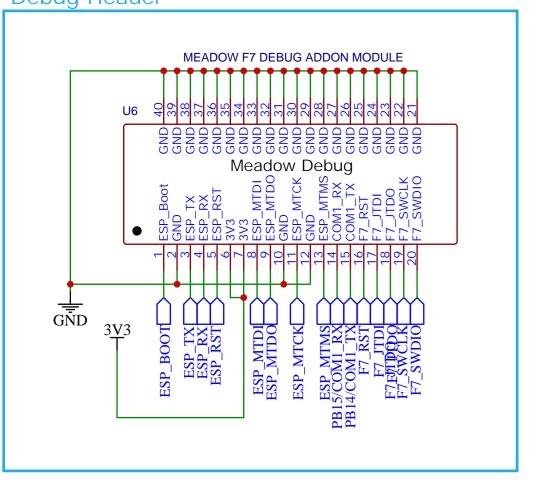
USB/Power/Reset



Enable Switch



Debug Header



Stackup/Controlled Impedance:

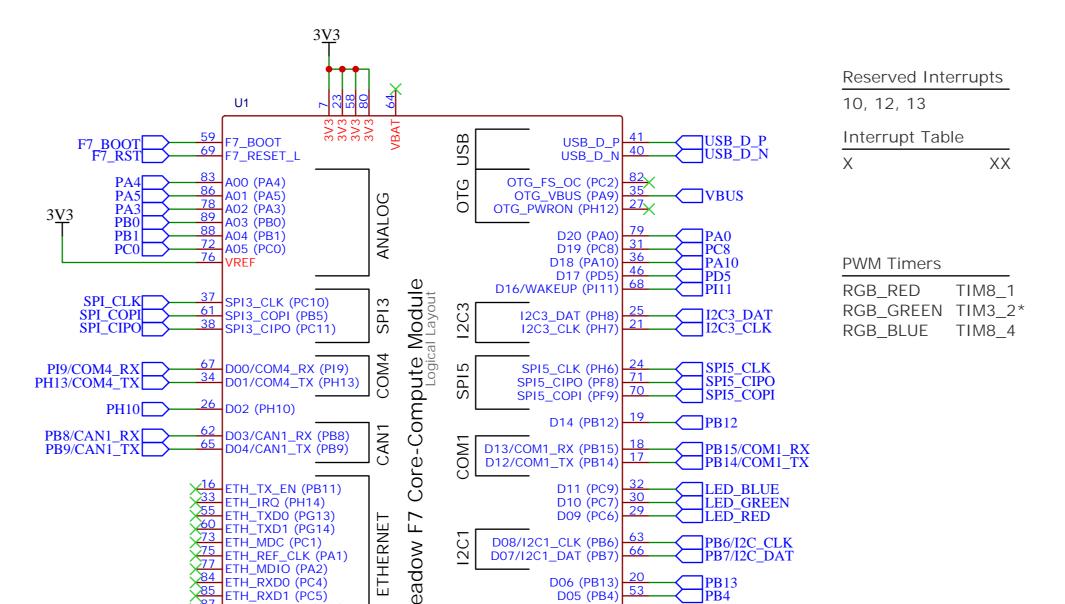
SD Signals: 50 Outer layer: 0.29mm width

Inner layer: 0.23mm width USB: 90 Diff Pair

Outer layer: 0.19mm width, 0.11mm spacing Inner layer: 0.13mm width, 0.11mm spacing MCU -> PHY - 50 Single-Ended

Outer layer: 0.29mm width, 0.127mm spacing Inner layer: 0.24mm width, 0.127mm spacing

JLCPCB Stackup: JLC7628



F7_SWO (PB3)
F7_JTDI (PA15)
F7_SWCLK (PA14)
F7_SWDIO (PA13)
ESP_MTDO
ESP_MTCK
ESP_MTDI
ESP_MTDI
ESP_MTDI
ESP_MTMS
ESP_TX (PC12)
ESP_RX (PD2)
ESP_RST (PF7)
ESP_RST
EFT_ITDO
FFT_JTDI
FFT_SWCLK
FFT_SWDIO
FFT_SWDIO
ESP_MTDI
ESP_MTCK
TSP_MTCK
TSP_MTDI
TSP_MTMS
TSP_MTMS
TSP_MTMS
TSP_TX
TSP_BOOT
TSP_RST
TSP_BOOT
TSP_RST

ETH_MDIO (PA2) 84 ETH_RXD0 (PC4)
85 ETH_RXD1 (PC5)
ETH_CRS_DV (PA7)

 SD_IN_L
 28
 SD2_IN_L (PG6)

 SD_CLK
 47
 SD2_CLK (PD6)

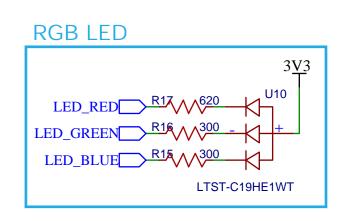
 SD_CMD
 51
 SD2_CMD (PD7)

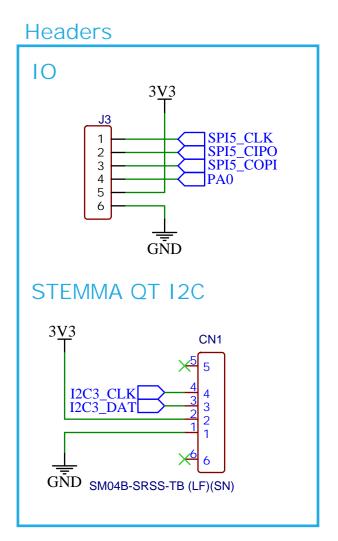
 SD_D1
 51
 SD2_D1 (PG10)

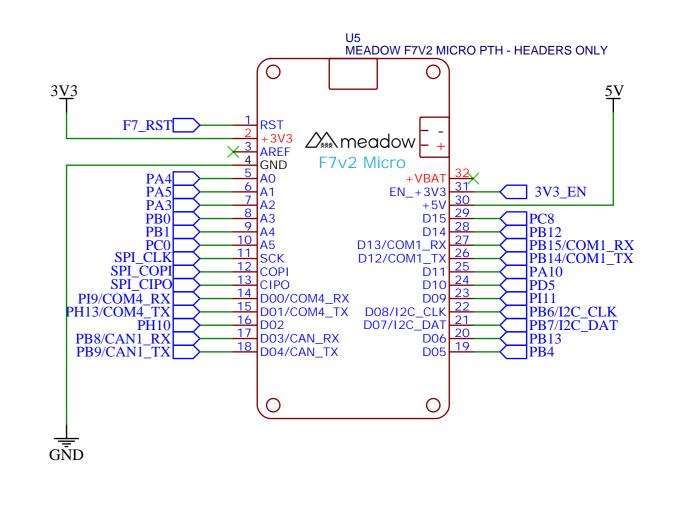
 SD_D0
 52
 SD2_D0 (PG9)

 SD_D2
 54
 SD2_D2 (PG11)

 SD_D3
 56
 D15/SD2_D3 (PG12)









Date: 2023.01

Drawn By: bryan costanich