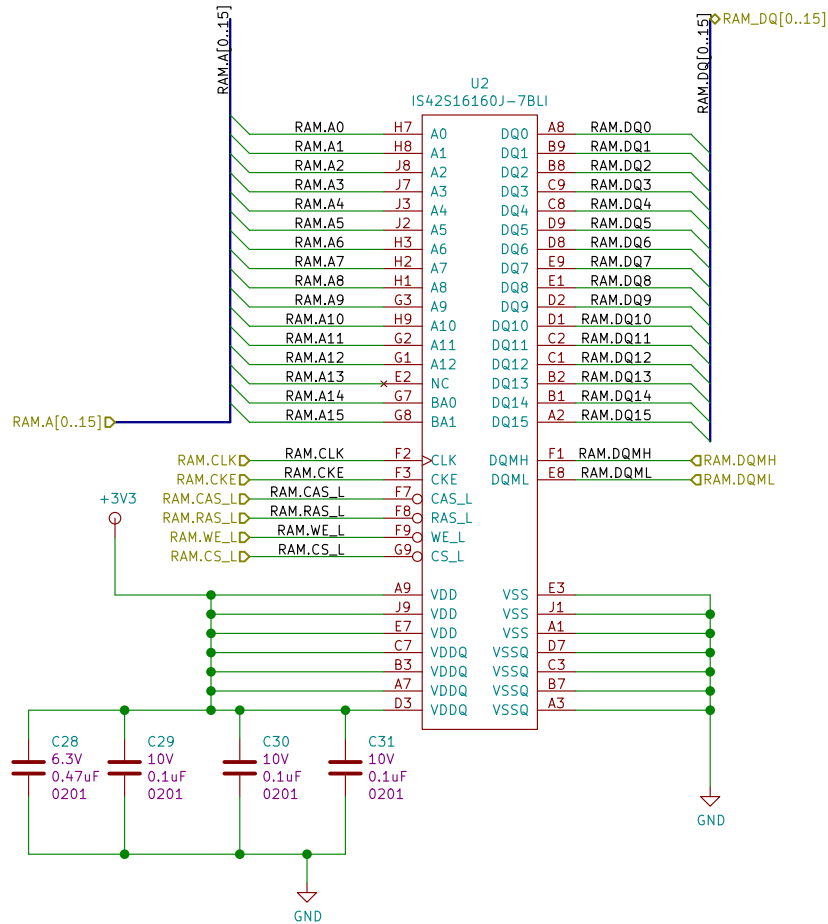
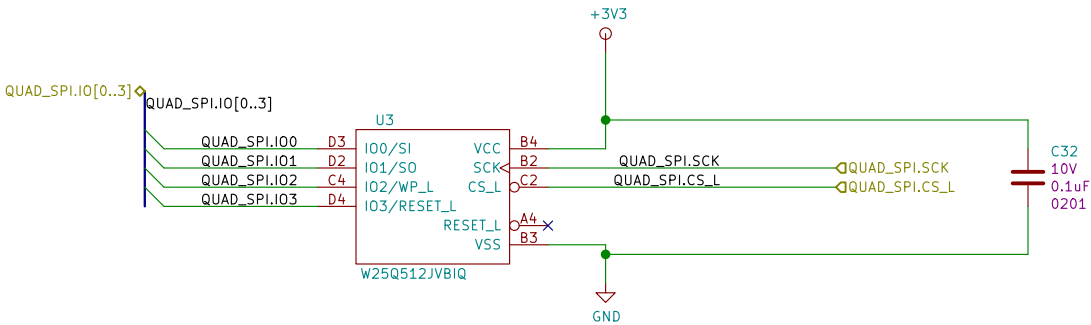


# RAM



# FLASH



## WILDERNESS LABS

Sheet: /memory/ File: Ram_Flash.sch		Designer: S.Johnson
Title: Core Compute Module V2		
Size: B	Date: 2021-08-02	Rev: A
KiCad E.D.A. kicad (5.1.10)-1		Id: 2/4

# ESP32

Table 1. SKYA21001 Signal Descriptions

Pin	Name	Description	Pin	Name	Description
1	J3	RF output <sup>1</sup>	4	V1	DC control voltage GPIO27
2	GND	Ground	5	J1	RF output <sup>1</sup>
3	J2	RF output <sup>1</sup>	6	V2	DC control voltage GPIO26

<sup>1</sup> A 100 pF blocking capacitor is required for >500 MHz operation. Use larger value capacitors for lower frequency operation.

# WILDERNESS LABS

Sheet: /ESP32/

File: ESP32.sch

Designer: S.Johnson

**Title: Core Compute Module V2**

Size: A4


Date: 2021-08-02

Rev: A

KiCad E.D.A. kicad (5.1.10)-1

Id: 3/4

Pin	Name	Description	Pin	Name	Description
1	J3	RF output <sup>1</sup> External Ant	4	V1	DC control voltage GPIO27
2	GND	Ground	5	J1	RF output <sup>1</sup>
3	J2	RF output <sup>1</sup> On Board Antenna	6	V2	DC control voltage GPIO26



# WILDERNESS LABS

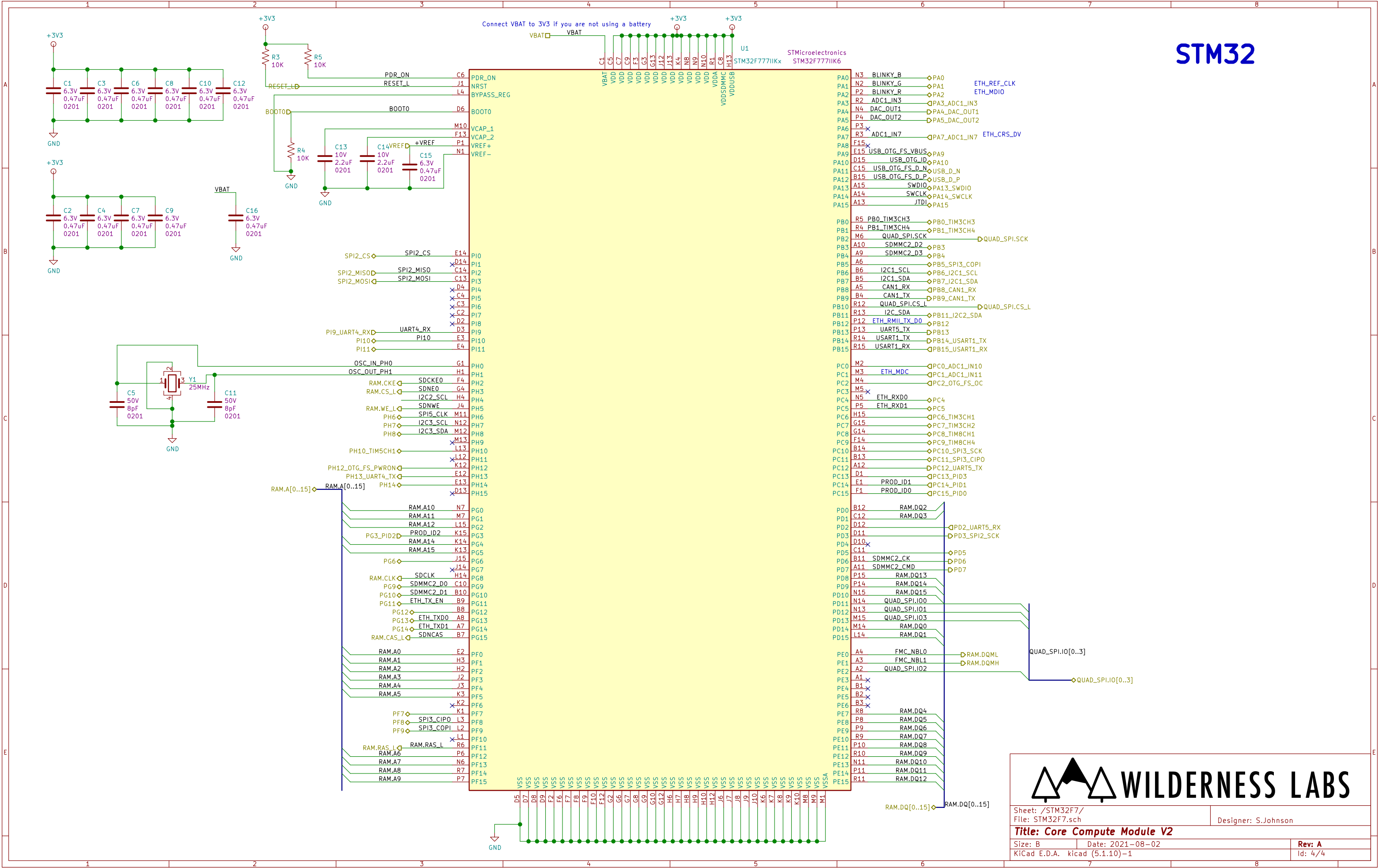
Sheet: /ESP32/
Designer: S.Johnson


**Title: Core Compute Module V2**

Size: A4
Date: 2021-08-02
**Rev: A**

KiCad E.D.A. kicad (5.1.10)-1
Id: 3/4

STM32





# WILDERNESS LABS

Sheet: /STM32F7/  
File: STM32F7.sch

Designer: S.Johnson

**Title: Core Compute Module V2**

Size: B  
KiCad E.D.A.    kicad (5.1.10)–1

Date: 2021–08–02  
Id: 4/4

Rev: A