Stability Improvement of Pulse Power Supply With Dual-Inductance Active Storage Unit Using Hysteresis Current Control

Ping Yang, *Member, IEEE*, Xi Chen, *Student Member, IEEE*, Rongqian Chen, Yusheng Peng, Songrong Wu, and Jianping Xu, *Member, IEEE*

***Abstract*— The output power of the pulsed power supply (PPS) pulsates at the pulse repetition frequency (PRF) of pulse load. The pulsating power will result in a large bus voltage ripple. To balance the instantaneous power difference, a single or dual-inductance active storage unit (ASU) is usually connected in parallel with the output terminal of the PPS. Poor compensating current tracking accuracy of ASU will lead to the output current of PPS suffered from serious current spikes, which affects the stability of the bus voltage. A hysteresis current control (HCC) is proposed to achieve an excellent pulse current compensation performance. Compared with the current mode control (CMC), the small-signal modeling of dual-inductance with HCC is established to illustrate good compensation performance. Besides, a valley voltage loop is introduced to regulate the storage capacitor voltage in dual-inductance ASU to reduce the power loss at any pulse duty cycle. An experimental prototype is built to verify the spikes in output current can be eliminated effectively, the bus voltage keeps smooth and stable, and the output capacitor of the per-stage DC/DC converter is reduced significantly.**

***Index Terms*— Dual-inductance active storage unit (ASU), hysteresis current control (HCC), pulse power supply (PPS), tracking accuracy, valley voltage control.**

I. Introduction

PULSED power supply (PPS) as a special power supply has been around for many years, which is characterized by periodic transient high power. And it has been widely applied in industrial and military fields include wastewater treatment [1], [2], metal processing [3], air purification [4], and pulsed radar system [5]. Because of the poor application environment, PPS is highly demanded for high power density, long lifetime, and stability. However, due to the difference between input power and pulse power, the bus voltage of PPS suffers from serious fluctuation because of the transient high power of pulse load. A straightforward way is to increase a bulk electrolytic capacitor to store enough power for pulse load, however, as the demand capacity of the system increases, the capacitance capacity cannot be satisfied, and the power density of the converter is low. Another way is to provide an extra power flow path for high power by increasing other converters, but the efficiency is low because instantaneous high power is transmitted by two-stage topology in [6]. The linear amplifier is introduced in [7] to parallel with a high power path, which brings power loss inevitably. Connecting a bidirectional converter named active storage unit (ASU) in parallel with the output to buffer the unbalance power became the most common practice gradually. It has been widely used in single-phase dc-ac inverters [8]–[11], single-phase power factor correction (PFC) rectifiers for light emitted diode (LED) supply without flicker-free [12], [13], and cascaded dc-dc converter to enhance the stability of cascaded system [14]. The bidirectional converter also is used in pulse load applications [15], [16], as shown in Fig. 1. In [16], the bidirectional converter is applied in an ac-dc converter, which can compensate second harmonic current and supply pulse power concurrently. Due to the inductor in bidirectional converter limits the slope of compensating current, unexpected spikes appear at the output current, which leads to the bus voltage affected severely, especially when photovoltaic (PV) module or low power generator as the main power source at the input port in Fig. 1. And if another steady-state load connects on the same DC bus, the stability of the load is also not guaranteed anymore.

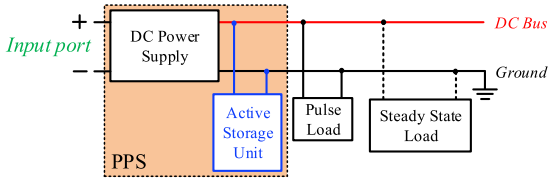

Fig. 1. Schematic of the PPS with loads.

Essentially, the control objective of the ASU is to regulate its compensating current equals to the ac component in pulse current, which is a rectangular wave. The ASU with feed-forward control strategy is proposed in [17] to enhance the tracking performance of compensating current,

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The authors are with the Key Laboratory of Magnetic Suspension Technology and Maglev Vehicle, Ministry of Education, Southwest Jiaotong University, Chengdu 610031, China (e-mail: pyang@swjtu.edu.cn).

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in which the control circuit is quite complicated to obtain instantaneous duty-cycle. The good compensation performance in [18] can be realized by one-cycle control without being affected by the tolerance or parameter deviations of the passive components. Real-time duty-cycle (RDC) calculation control strategy with the digital signal processor (DSP) is further presented in [19], [20], and the analogy circuit is greatly reduced. To ensure current tracking accuracy under different PRF, the current mode control (CMC) with a dual loop is proposed in [21], the compensating current is controlled indirectly by controlling the output current. However, the variational storage capacitor voltage results in the gain of the current loop unstable, which affects the compensation performance. So as to further improve the current control accuracy, the deadbeat current control method is proposed in [22] for switched reluctance motor (SRM), the accuracy of phase current control has improved greatly. In addition to the optimization of control methods, the structure of topology is improved to realize excellent compensation performance. The dual-inductance ASU proposed in [23] to provide two flow paths for compensating current, the compensation performance has been greatly improved but the output current spikes still exist.

Hysteresis current control (HCC) has been applied to achieve fast dynamic performance in [24]. For the sake of further eliminating the output current spikes, HCC is applied to the dual-inductance ASU to enhance compensation performance in this paper. And compared with the CMC strategy, the small-signal modeling of dual-inductance ASU with HCC is established to illustrate compensation performance.

This paper is organized as follows. The topology and operating principle of dual-inductance ASU is presented in Section II. In Section III, the cause of current spikes in the CMC is analyzed by small-signal modeling, and the HCC is proposed to achieve excellent compensation performance. Section IV proposes the small-signal modeling of dual-inductance ASU with HCC, compared with the CMC from simulation results. In Section V, the experimental results from a prototype with a peak power of 500 W and PRF of 100-500 Hz are provided to verify the compensation performance in HCC. Finally, Section VI concludes this paper.

II. Operating Principle of Dual-Inductance ASU

The application of the dual-inductance ASU is presented in detail in [23]. Here, we iterate the operating principle briefly to better understand the hysteresis control strategy.

By utilizing the quick charging and discharging characteristics of the storage capacitor in ASU, the ASU can be composed of bidirectional half-bridge topologies, including buck-type, boost-type, and buck-boost type. The inductor current as the compensating current is continuous and can be controlled easily in boost-type, so the bidirectional buck/boost converter is often chosen as ASU. As shown in Fig. 2, the dual-inductance structure is employed to replace the single inductor, which can provide independent current flow paths, so the direction of the inductor current remains the same, and the unexpected current spikes can be suppressed caused by the single inductor structure.

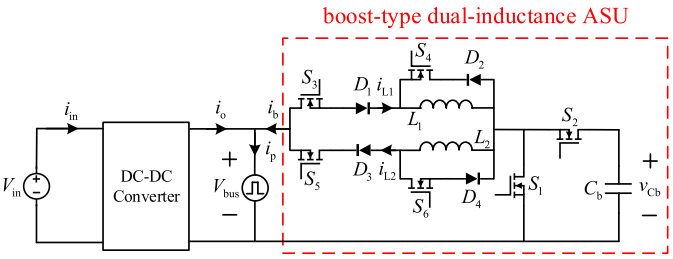

Fig. 2. Circuit configuration of PPS with dual-inductance ASU.

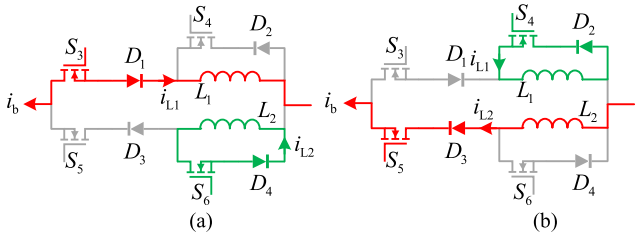

Fig. 3. The operation mode of dual-inductance structure. (a) boost mode. (b) buck mode.

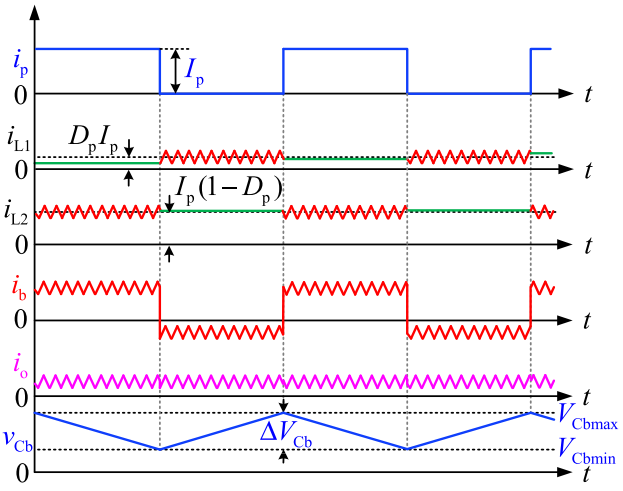

Fig. 4. Key operational waveforms of PPS with dual-inductance ASU.

Fig. 3 shows the dual-inductance structure under the boost mode and buck mode, when one of the inductors is connected to the pre-stage DC-DC converter, another one with switch and diode constitute the continuous inductor current path.

Fig. 4 shows the key waveforms of dual-inductance ASU, including the pulse load current i_p, the two inductors current i_{L1} and i_{L2}, the compensating current i_b, the output current i_o, and the voltage of storage capacitor v_{Cb}, where the I_p is the peak value of i_p, the D_p is pulse duty cycle, and the ΔV_{Cb} is the voltage variation of the storage capacitor. If the inductor loss is ignored, the inductor current remains unchanged. At the beginning of the next pulse period, the dual-inductance ASU can fully respond to the change of pulse current, the current spikes can be suppressed significantly.

III. Hysteresis Current Control Strategy of the Dual-Inductance ASU

A. Cause of Current Spikes in the Bus Port With CMC

The bidirectional buck/boost converter with two inductors is used as dual-inductance ASU to balance the instantaneous power difference. Since both inductance values are the same

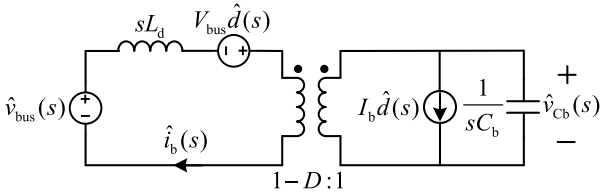

Fig. 5. Small-signal equivalent circuit of the dual-inductance ASU in CCM.

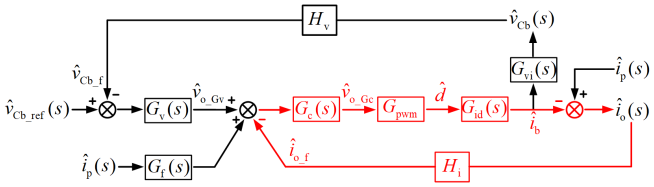

Fig. 6. Control block diagram of the dual-inductance ASU with CMC.

and only one inductor is involved in a switching cycle, by using a state-space averaging approach, the small-signal modeling of bidirectional buck/boost converter with two inductors operating in a continuous conduction mode (CCM) can be obtained, as shown in Fig. 5, where the D is the steady-state duty cycle of S_1, the inductance value L_d is equal to L_1 and L_2, and I_b is the average inductor current.

According to Fig. 5, the transfer function of the duty cycle to inductor current, and the inductor current to the voltage of the storage capacitor can be obtained separately as

$$G_{id}(s) = \left.\frac{\hat{i}_b(s)}{\hat{d}(s)}\right|_{\hat{v}_{bus}(s)=0} = \frac{C_b V_{Cb} s}{C_b L_d s^2 + (V_{bus}/V_{Cb})^2} \quad (1)$$

$$G_{vi}(s) = \frac{\hat{v}_{Cb}(s)}{\hat{i}_b(s)} = \frac{V_{bus}}{C_b V_{Cb} s} \quad (2)$$

Fig. 6 shows the control block diagram of the dual-inductance ASU with CMC mentioned above, the current loop is brought to control output current i_o equal to dc component that is filtered by a low-pass filter (LPF), the current loop is expected to have high gain at 0 Hz to ensure higher tracking accuracy of i_o. To ensure the normal operation of the bidirectional buck/boost converter, the voltage loop is introduced to keep that the minimum voltage of the storage capacitor is greater than the bus voltage. The output of voltage loop regulator v_{o_Gv} is approximately a small dc value with little PRF harmonic, so the reference for output current mainly contains the dc component. And the H_v is the senor gain of storage capacitor voltage v_{Cb}, the H_i is the senor gain of output current i_o, $G_{pwm} = 1/V_{saw}$ is the gain of a pulse width modulator, V_{saw} is the amplitude of the saw-tooth carrier, $G_f(s)$ is the transfer function of LPF.

On account of the pulse load characterized by low PRF, the small-signal of pulse current $\hat{i}_p(s)$ can be ignored, the current loop is shown in red in Fig. 6, the gain of which can be simplified as

$$T_{c\_CMC}(s) = H_i G_c(s) G_{pwm} G_{id}(s) = \frac{H_i C_b V_{Cb} G_c(s) s}{\left[C_b L_b s^2 + (V_{bus}/V_{Cb})^2\right] V_{saw}} \quad (3)$$

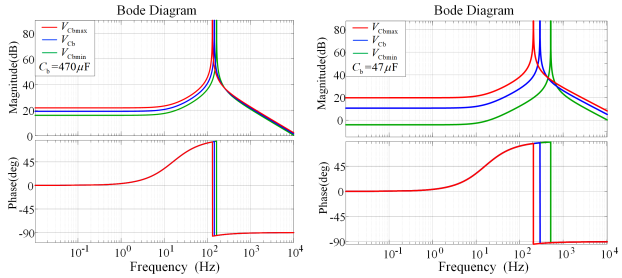

Fig. 7. Bode plots of $T_{c\_CMC}(s)$. (a) $C_b = 470\ \mu$F. (b) $C_b = 47\ \mu$F.

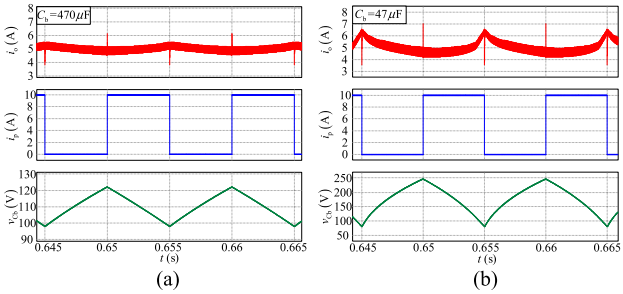

Fig. 8. Simulation results of the output current spikes with CMC. (a) $C_b = 470\ \mu$F. (b) $C_b = 47\ \mu$F.

As mentioned above, the tracking accuracy is determined by the gain of the current loop, the magnitude of $T_{c\_CMC}(s)$ is expected to be large at 0 Hz. Therefore, a type II compensator is employed to increase the loop gain magnitude by adding a pole and a zero. The transfer function of the current regulator $G_c(s)$ is designed to be $G_c(s) = G_{c0}(s)(1+\frac{\omega_z}{s})$, where the $G_{c0}(s)$ is feedback gain, ω_z is added angular frequency of zero. According to (3), $T_{c\_CMC}(s)$ is changed with the value of storage capacitor V_{Cb}, since the waveform of V_{Cb} is sawtooth waveform at PRF, which has both maximum and minimum value, the Bode plots of $T_{c\_CMC}(s)$ with maximum voltage value V_{Cbmax} and minimum voltage value V_{Cbmin} can be obtained in Fig. 7.

From Fig. 7(a), it can be known that when the capacitance of the storage capacitor is large enough, the $|T_{c\_CMC}(0)|$ is changed slightly at different V_{Cb}, which is enough for high tracking accuracy. But in the case of a small capacitance storage capacitor, as shown in Fig. 7(b), the $|T_{c\_CMC}(0)|$ is changed a lot, which results in low tracking accuracy. Fig. 8 shows the simulation results of the storage capacitor voltage, output current, and pulse current with capacitors of different capacities under the CMC. It can be known that the current spikes occur apparently when a small capacitance capacitor is used. To further reduce the current spikes and increase the stability of bus voltage, the current feedback loop base on CMC is not sufficient, and practically one-fifth of switching frequency is usually a limit in the design of the bandwidth of linear controllers.

B. Hysteresis Current Control Strategy for the Dual-Inductance ASU

In order to eliminate the current spikes completely to improve the stability of bus voltage, the excellent

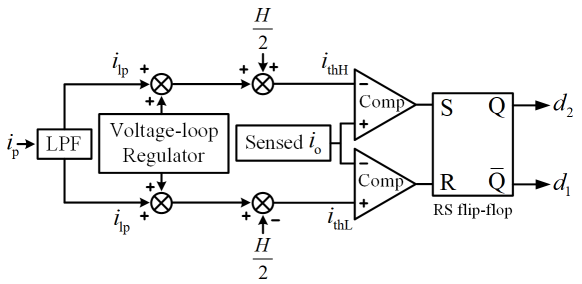

Fig. 9. The simplified control structure of the HCC.

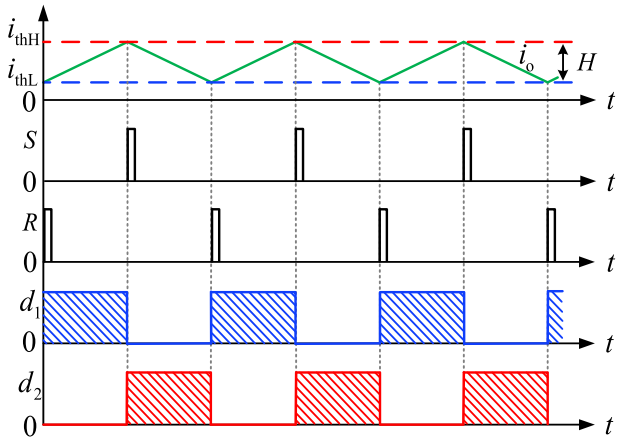

Fig. 10. Operation waveforms of the control structure for the HCC.

compensation performance of dual-inductance ASU is expected to be achieved. On account of output current contains switch periodic ripple from inductor current, so the objective is to control the output current to realize the operation of S_1 and S_2 in dual-inductance ASU. The proposed HCC method controls two current thresholds in the control circuitry, i_{thH} and i_{thL}, the output current i_o is sampled by senor, and is then compared with two thresholds. The simplified structure of the HCC controller and operations waveforms are illustrated respectively in Fig. 9 and Fig. 10, where the H is the fixed hysteretic-band. Since i_o is equal to pulse current i_p subtracts compensating current i_b according to Kirchhoff's law, i_o contains the inductor current ripple from i_b. Hence, by using two comparators, when i_o is greater than i_{thH}, the RS flip-flop is SET, corresponding high-side switch S_2 is ON and the complementary low-side switch S_1 is OFF. When i_o is below i_{thL}, S_1 and S_2 go into the opposite state. When the value of i_o is between i_{thH} and i_{thL}, both output logic of comparators are LOW, and the RS flip-flop maintains the previous state.

The two thresholds, i_{thH} and i_{thL} are generated by adder, subtractor, LPF, and voltage regulator. Since the storage capacitor voltage v_{Cb} should be guaranteed above the bus voltage V_{bus} for the boost-type bidirectional topologies, the output of voltage regulator, which is a dc value, is introduced to generate thresholds as illustrated in Fig. 9. Where the i_{lp} is dc component filtered from i_p to be used to provide a reference for output current.

According to Fig. 10, the difference values of i_{thH} and i_{thL} are fixed by hysteretic-band H, the switching frequency is

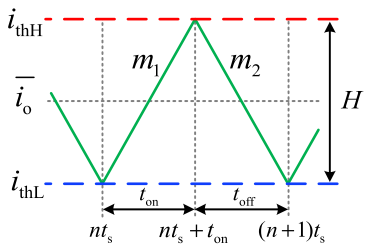

Fig. 11. Instantaneous output current with two thresholds.

given as follows

$$f_s = \frac{1}{t_{on}+t_{off}} = \frac{1}{\frac{H}{m_1}+\frac{H}{m_2}} = \frac{V_{bus}(v_{Cb}-V_{bus})}{H L_d v_{Cb}} \tag{4}$$

where m_1 and m_2 are the slopes of inductor current respectively, it is noted that the instantaneous waveform of v_{Cb} is the sawtooth waveform, so the switching frequency of the HCC is variable and related to hysteretic-band H.

IV. Modeling and Analysis of Dual-Inductance ASU Using HCC

Not only the excellent loop performance of the HCC method has but also the instability can be prevented for all duty cycle since HCC is based on bounded operation between the upper and the lower trip point. In this section, the derivation procedure of the small-signal modeling for dual-inductance ASU with HCC is presented.

Fig. 11 shows the output current with two current thresholds, the modeling approach adopted replaces the duty cycle d with the on-time t_{on} of switch S_1 and switch period t_s, which are linear even in the variable switching frequencies.

The relationship of average duty cycle $\overline{d}$, average on-time $\overline{t_{on}}$ and average switch period $\overline{t_s}$ can be obtained in (5)

$$\overline{t_{on}} = \overline{d} \times \overline{t_s} \tag{5}$$

Small signal perturbations are added to the equation (5), the relationship can be obtained as follow

$$\hat{d} = \frac{\hat{t}_{on} - D\hat{t}_s}{T_s} \tag{6}$$

Referring to [25] and [26], for the fixed hysteretic-band HCC, the small-signal relationship between switching period and on-time is as follow

$$\begin{aligned}\hat{t}_s &= \hat{t}_{on} + \frac{T_{off}}{V_{Cb}-V_{bus}}(\hat{v}_{Cb}-\hat{v}_{bus}) \\ &= \hat{t}_{on} + \frac{(1-D)T_s}{V_{Cb}-V_{bus}}(\hat{v}_{Cb}-\hat{v}_{bus})\end{aligned} \tag{7}$$

According to Fig. 11, the current threshold can be obtained as follow

$$i_{thH} = \overline{i_o} + \frac{1}{2}m_1 t_{on} = \overline{i_o} + \frac{v_{bus}}{2L_d}t_{on} \tag{8}$$

With small-signally perturbed (8), the small-signal of i_{thH} can be obtained as follow

$$\hat{i}_{thH} = \hat{i}_o + \frac{V_{bus}\hat{t}_{on} + T_{on}\hat{v}_{bus}}{2L_d} \tag{9}$$

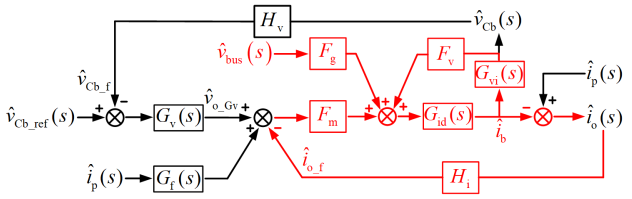

Fig. 12. Control block diagram of the dual-inductance ASU with HCC.

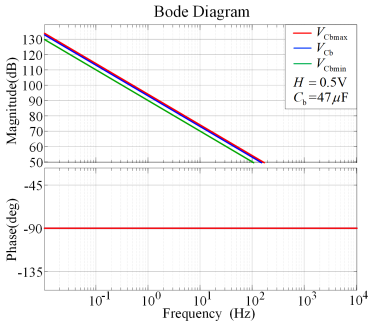

Fig. 13. Bode plots of $T_{c\_HCC}(s)$.

The following relationship can be obtained from (9)

$$\hat{t}_{on} = \frac{2L_d}{V_{bus}}\left(\hat{i}_{thH} - \hat{i}_o - \frac{DT_s}{2L_d}\hat{v}_o\right) \tag{10}$$

According to Fig. 9, the relationship between $\hat{i}_{thH}$ and $\hat{v}_{o\_Gv}$ can be represented as

$$\hat{i}_{thH} = \hat{v}_{o\_Gv} \tag{11}$$

Substituting (7) and (10) into (6), the $\hat{d}$ can be obtained

$$\hat{d} = F_m(\hat{v}_{o\_Gv} - H_i\hat{i}_o) + F_g\hat{v}_{bus} + F_v\hat{v}_{Cb} \tag{12}$$

where

$$F_m = \frac{2L_d}{V_{Cb}T_sH_i}, \quad F_g = -\frac{1}{V_{Cb}}, \quad F_v = \frac{1-D}{V_{Cb}}.$$

According to (12), the small-signal modeling diagram of dual-inductance ASU with HCC is shown in Fig. 12.

In Fig. 12, by setting $\hat{v}_{Cb\_ref}(s) = 0$, $\hat{v}_{bus}(s) = 0$, and $\hat{i}_p(s) = 0$, the current loop $T_{c\_HCC}(s)$ is presented as

$$\begin{aligned} T_{c\_HCC}(s) &= \frac{H_iF_mG_{id}(s)}{1 - F_vG_{id}(s)G_{vi}(s)} = \frac{2}{T_ss} \\ &= \frac{2V_{bus}(v_{Cb} - V_{bus})}{HL_dv_{Cb}s} \end{aligned} \tag{13}$$

According to (13), the Bode plots of $T_{c\_HCC}(s)$ with maximum voltage value V_{Cbmax} and minimum voltage value V_{Cbmin} can be obtained in Fig. 13.

From Fig. 13, it can be known that when v_{Cb} varies from the maximum to minimum value, $|T_{c\_HCC}(s)|$ is change slightly, the storage capacitor voltage has little effect on the gain of the current loop. And $|T_{c\_HCC}(0)|$ can be supposed to infinite from (13), which achieves high tracking accuracy.

Fig. 14 shows the Bode plots of $T_{c\_HCC}(s)$ with different hysteretic-band H, it can be seen that even at different H, $|T_{c\_HCC}(0)|$ has a high magnitude.

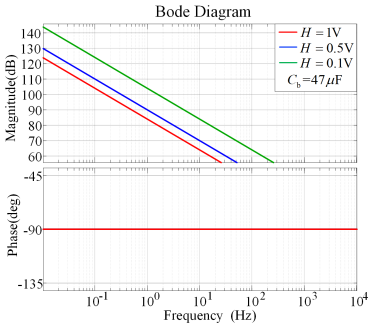

Fig. 14. Bode plots of $T_{c\_HCC}(s)$ with different hysteretic-band H.

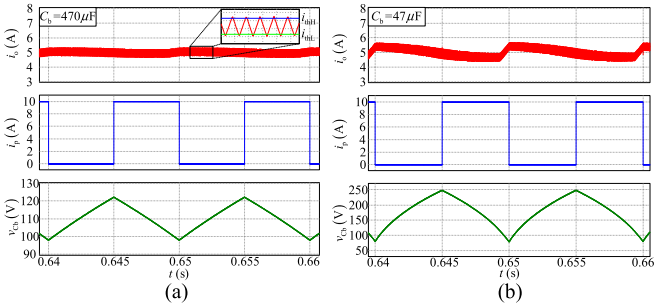

Fig. 15. Simulation results of the output current spikes with HCC. (a) $C_b = 470\ \mu$F. (b) $C_b = 47\ \mu$F.

While the inner closed-loop transfer function $A_{HCC}(s)$ is

$$\begin{aligned} A_{HCC}(s) &= \frac{1}{H_i}\frac{T_{c\_HCC}(s)}{1 + T_{c\_HCC}(s)} = \frac{1}{H_i}\frac{1}{\frac{T_s}{2}s + 1} \\ &= \frac{1}{H_i}\frac{1}{\frac{HL_d}{2V_{bus}(1 - V_{bus}/v_{Cb})}s + 1} \approx \frac{1}{H_i} \end{aligned} \tag{14}$$

From (14), it can be found that the closed-loop transfer function of dual-inductance ASU with HCC is reduced to a first-order system. Although $A_{HCC}(s)$ is relevant to the storage capacitor voltage v_{Cb}, by decreasing the hysteretic-band H, the influence can be ignored and the equivalent power stage could be regarded as a proportional component. Fig. 15 shows the simulation results of the storage capacitor voltage, output current, and pulse current with capacitors of different capacities under the HCC. It can be seen that there are no spikes in output current. Therefore, compared to the CMC, the HCC is more conducive to the improvement of compensation performance.

V. Prototype Design of the PPS With Dual-Inductance ASU Using HCC

To verify the validity of the proposed HCC strategy in improving compensation performance to eliminate current spikes and improve the stability of bus voltage, a peak power 500 W PPS is constructed, flyback converter is employed as pre-stage DC/DC converter due to its advantages of low component cost and simple control. Fig. 16 shows the main circuit of PPS with dual-inductance ASU, and the key specifications are given in Table I.

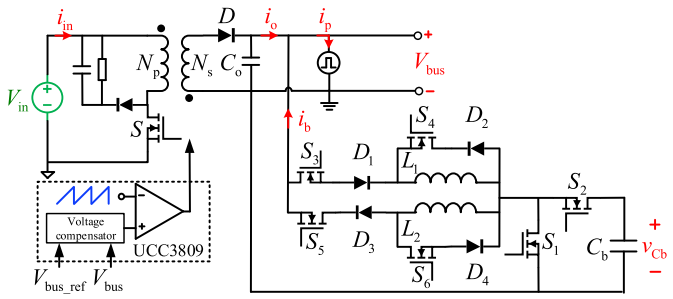

Fig. 16. The main circuit of the PPS.

TABLE I
KEY SPECIFICATIONS OF THE PPS

Parameters	Values
Input voltage V_{in}	220 V
Bus voltage V_{bus}	50 V
Valley storage capacitor voltage $V_{Cbvalley}$	100 V
Output peak current I_p	10 A
PRF f_p	100-500 Hz
Pulse duty cycle D_p	0.2-0.8

A. Parameters Design of PPS With Dual-Inductance ASU

The flyback converter is designed to operate in discontinuous current mode (DCM). As shown in Fig. 16, the average bus voltage V_{bus} is regulated by voltage mode control (VMC) to keep stable, and the controller is made up of UCC3809 and optocoupler H11AV1. The switching frequency of the flyback converter is set to 150 kHz, a 330 μF electrolytic capacitor is employed as the filter capacitor C_o to filter switching frequency ripple.

Referring to [15] and [16], the capacitance of storage capacitor in the ASU is derived as

$$C_b = \frac{V_{bus} D_p (1-D_p) I_p}{f_p \Delta V_{Cb} V_{Cb\_ave}} = \frac{V_{bus} D_p (1-D_p) I_p}{f_p \Delta V_{Cb} (V_{Cbvalley} + \frac{1}{2}\Delta V_{Cb})} \quad (15)$$

where V_{Cb_ave} is the average value of storage capacitor voltage, and $\Delta V_{Cb} = V_{Cbmax}$-$V_{Cbmin}$.

According to (15), the storage capacitor voltage ripple ΔV_{Cb} is affected by pulse duty cycle D_p directly, ΔV_{Cb} reduces to minimum at the light and heavy load and reaches maximum at the half load as shown in Fig. 17. So, the voltage difference between bus voltage and storage capacitor voltage is large when the load is heavy and light, while the V_{Cb_ave} is regulated at a fixed level by average voltage control. But this will lead to increased switching frequency at heavy and light load according to (4), and thus the efficiency of the dual-inductance ASU will be degraded [27].

To reduce the power loss no matter how D_p changes, the valley voltage of storage capacitor $V_{Cbvalley}$ is detected and controlled to greater than bus voltage V_{bus}, so the voltage difference between bus voltage and storage capacitor voltage can be narrowed compared to average voltage control, as shown in Fig. 17(b). Letting $\Delta V_{Cb} = 25$ V while the tradeoff between the efficiency and volume is considered, and substituting them together with $V_{bus} = 50$ V, $I_p = 10$ A, $f_p = 100$ Hz, and $V_{Cbvalley} = 100$ V, the minimum required capacitance in dual-inductance ASU is chosen as 470 μF.

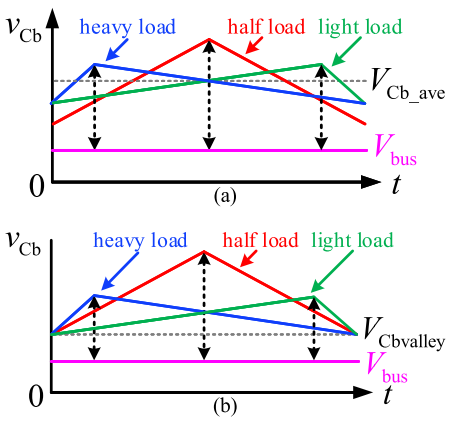

Fig. 17. Waveforms of v_{Cb} and V_{bus} under different loads. (a) With average voltage control. (b) With valley voltage control.

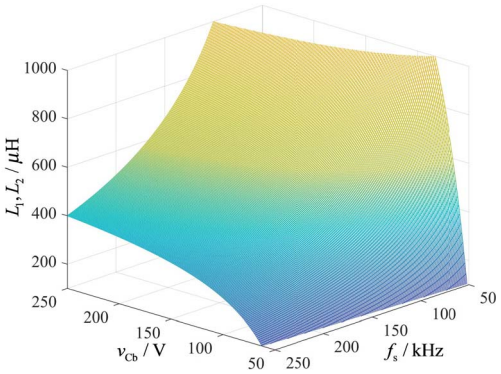

Fig. 18. Range of inductor L_1 and L_2.

TABLE II
ALL COMPONENT PARAMETERS OF THE PPS

Parameters	Values
Transformer turns ratio N_p:N_s	20:10
Switch of flyback converter S	IRF740
Diode of flyback converter D	STTH2003CT
Filter capacitor of flyback converter C_o	330 μF (NXA 80VB330)
Switches of dual inductor ASU (S_1~S_6)	KNF6140A
Diodes of dual inductor ASU (D_1~D_4)	SDURF1030
Inductors of dual inductor ASU (L_1~L_2)	600 μH (PQ3535)
Storage capacitor of dual inductor ASU C_b	470 μF (LPG471M35035FVA)

To reduce conduction loss in the dual-inductance ASU, the inductor current ripple is expected to be small. Since the inductor current ripple is only determined by hysteretic-band H and independent of inductance value, while inductor current ripple is certain, the smaller the value of H, the smaller size inductor can be used. However, too small H means higher switching frequency, which leads to more switching loss. Hence, the inductor current ripple is chosen as 20% of the minimum output current in PPS. Here, the H is chosen as 400 mV.

Since the inductance value, L_1 and L_2 are the same, while hysteretic-band H is fixed, L_1 and L_2 are determined by storage capacitor voltage v_{Cb} and switching frequency f_s, the L_1 and L_2 under different v_{Cb} and f_s can be plotted in Fig. 18, setting minimum switching frequency is 100 kHz, the required minimum inductance value are 600 μH. All component parameters are listed in Table II.

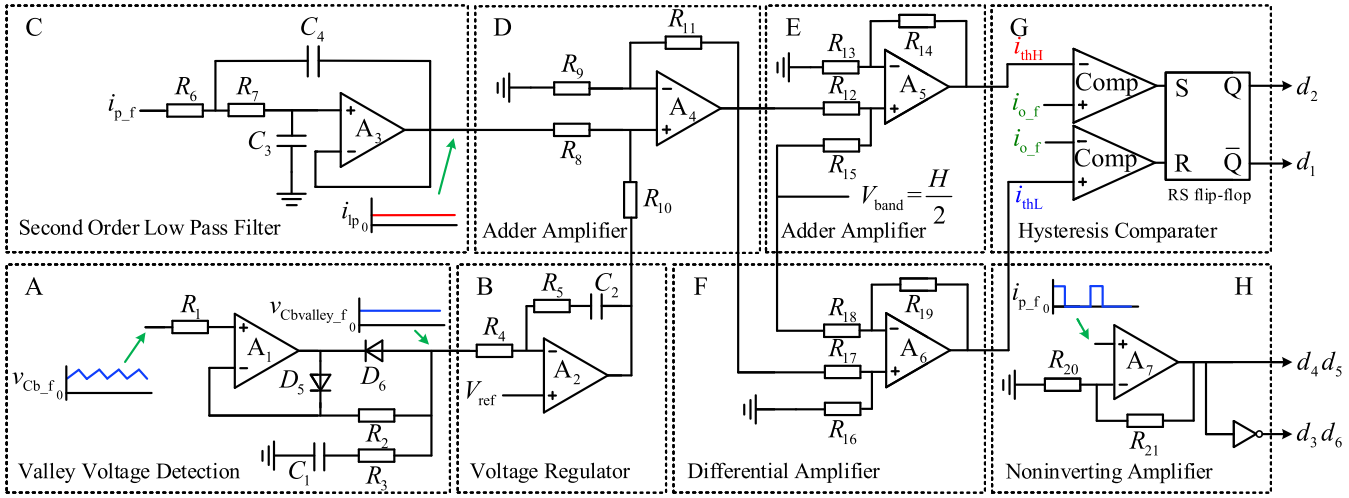

Fig. 19. The control circuit of PPS with HCC.

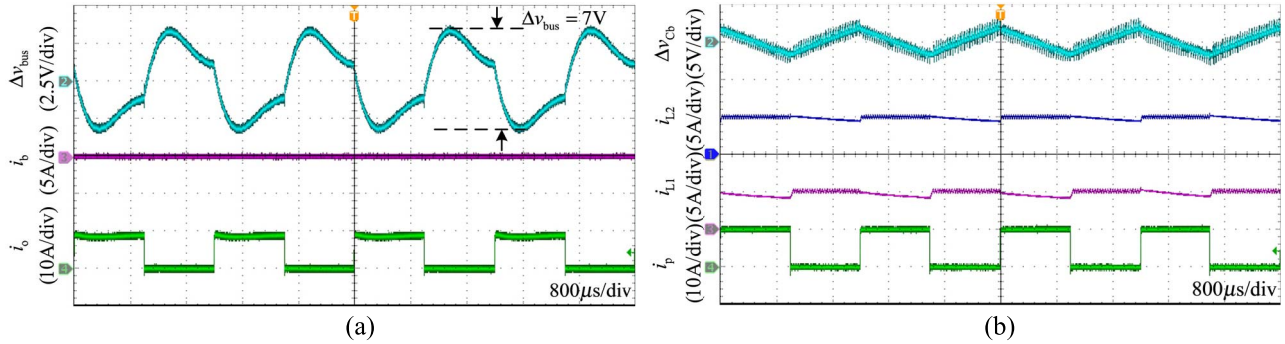

Fig. 20. Waveforms. (a) Waveforms of flyback converter without dual-inductance ASU. (b) Waveforms of dual-inductance ASU.

B. Controller Design of Dual-Inductance ASU With HCC

Based on the previous analysis, the detailed control circuit of the HCC strategy is shown in Fig. 19, which contains eight sub-circuits composed of analog components.

Sub-circuit A, which is composed of R_1, R_2, R_3, D_5, D_6, C_1, and amplifier A_1, is employed to sample valley storage capacitor voltage, and the proportional-integral voltage regulator in sub-circuit B can keep the $v_{Cbvalley\_f}$ stable at reference voltage V_{ref}. R_6, R_7, C_3, C_4, and amplifier A_3 consist the second-order LPF in sub-circuit C, the output i_{lp} (dc component in pulse current i_{p_f}) is added to the output of voltage regulator by adder amplifier in sub-circuit D to get new output current reference.

Sub-circuit E and F are adder amplifier and differential amplifier applied to generate two thresholds i_{thH} and i_{thL}. Noting that the output of sub-circuit D is added and subtracted from band voltage V_{band}, hence, the fixed hysteric-band H can be formed.

Sub-circuit G is a hysteresis comparator, composed of two comparators and an RS flip-flop, two logic signals are generated and sent to the drivers of S_1 and S_2. According to Fig. 3 and Fig. 4, driving signals of S_4, S_5 are in phase with output current, the drive signals of S_3, S_6 are in inverse phase with output current, so the noninverting amplifier is employed in sub-circuit H to generate drive signals of S_3-S_6.

C. Experimental Results

Fig. 20(a) shows the waveforms of flyback converter without dual-inductance ASU, as for the output port, the bus voltage ripple Δv_{bus} is 7 V when f_p is 500 Hz, $D_p = 0.5$, the output current i_o is the same as pulse current i_p, which is rectangle wave. Fig 20(b) shows the waveforms of the HCC employed for the PPS operates with dual-inductance ASU, where the two inductors current are continuous, even though two currents going down caused by the inductor loss.

Fig. 21(a) shows the experimental waveforms of Δv_{Cb}, v_{bus}, i_o, and i_p of the PPS with CMC, the bus voltage ripple has decreased a lot about 1.2 V, but the current spikes are up to 4 A and cannot be suppressed effectively. However, in Fig. 21(b), there are no spikes in i_o because of HCC. Thus, the proposed dual-inductance ASU with HCC has an excellent performance in improving the current tracking ability, which reduces the output current spikes significantly.

Fig. 22 and Fig 23 show experimental results for PPS at the condition of different pulse duty cycle D_p and PRF f_p, it can be also seen that bus voltage is stable, and output current spikes disappear.

Fig. 24 shows the output current i_o at the rising edge of the pulse current, because the i_o is limited to the thresholds, the current overshoot does not exist, which brings no current spikes on the output current.

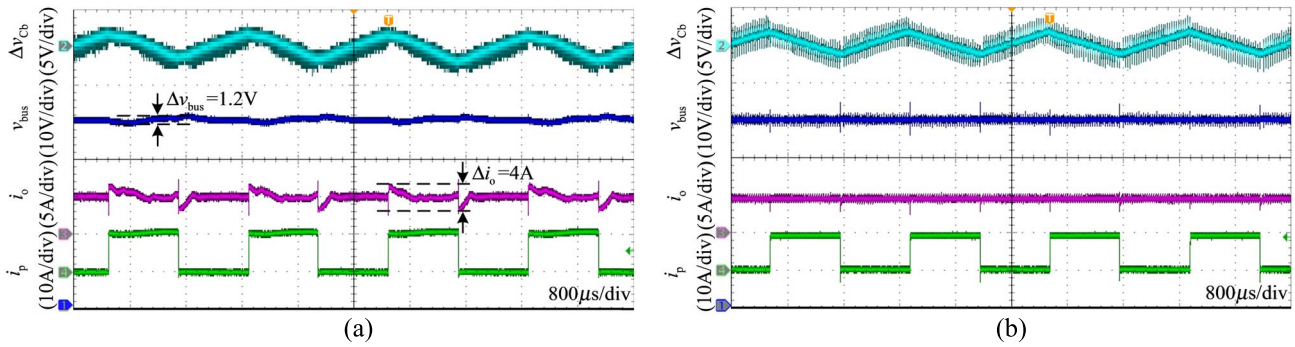

Fig. 21. Waveforms of the PSS. (a) With CMC. (b) With HCC.

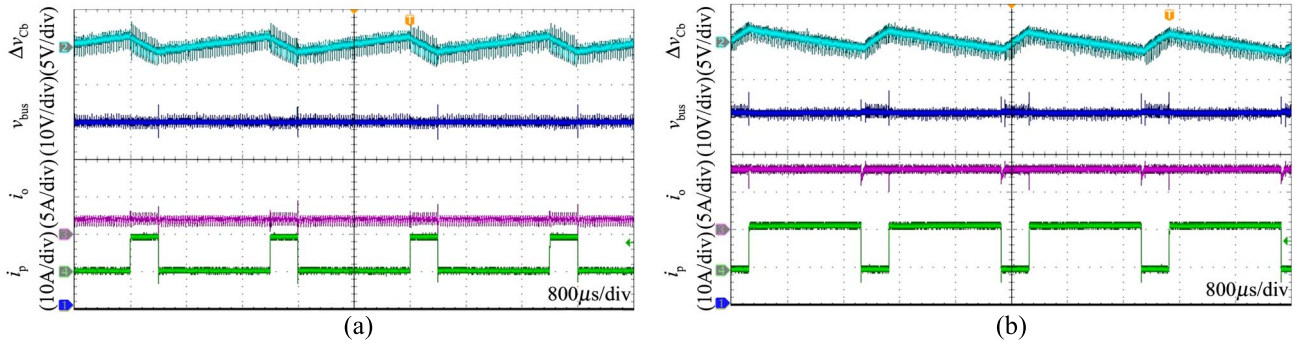

Fig. 22. Waveforms of the PPS with HCC under $f_{\mathrm{p}} = 500$ Hz and different D_{p}. (a) $D_{\mathrm{p}} = 0.2$. (b) $D_{\mathrm{p}} = 0.8$.

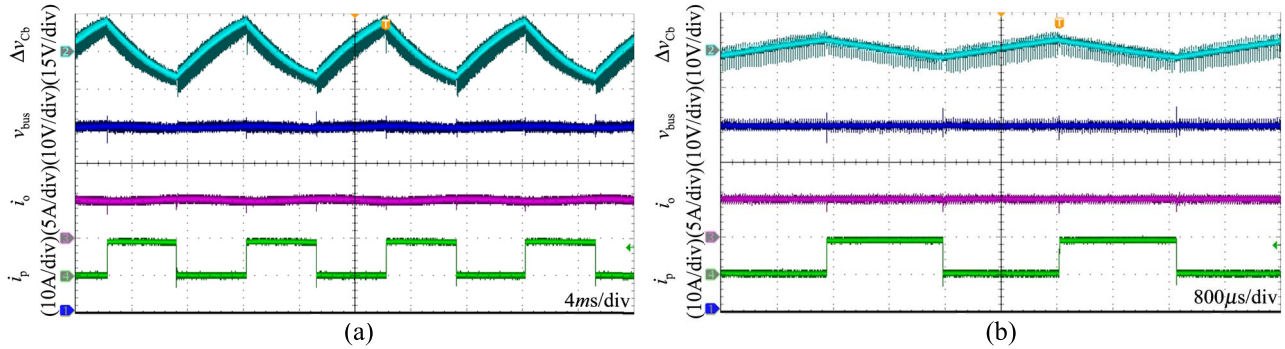

Fig. 23. Waveforms of the PPS with HCC under $D_{\mathrm{p}} = 0.5$ and different f_{p}. (a) $f_{\mathrm{p}} = 100$ Hz. (b) $f_{\mathrm{p}} = 300$ Hz.

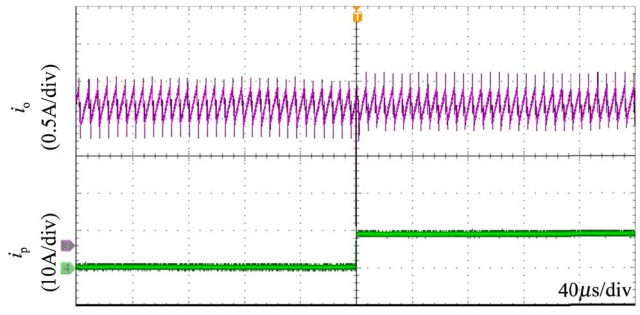

Fig. 24. Waveforms of the PPS with HCC at the rising edge of the pulse current.

TABLE III
COMPARISON OF THE PRIOR LITERATURES

	[21]	[23]	Proposed
Structure	single inductor	dual-inductance	dual-inductance
Control strategy	CMC	CMC	HCC
Peak power	500 W	500 W	500 W
Bus voltage	50 V	50 V	50 V
Maximum current spike	10 A	2.7 A	0.5 A

Table III gives the comparison of prior literatures [21], [23], and the proposed PPS with HCC. The PPS in [21] employs buck/boost bidirectional converter with CMC as ASU, but at expense of a large current spike. [23] presents the dual-inductance buck/boost bidirectional converter with CMC, the current spikes have been reduced. From Table III, it can be known that the maximum current spike in the proposed PPS with HCC is the smallest, which proves the

proposed dual-inductance ASU in HCC has better compensation performance.

VI. Conclusion

In order to eliminate the spikes in output current effectively and improve the stability of bus voltage greatly, a PPS with dual-inductance ASU in HCC is proposed for low-frequency pulse load. The output current of PPS is controlled to track the dc component of pulse current by HCC strategy to achieve an excellent compensation performance. And compared with the CMC, the small-signal modeling of dual-inductance ASU with HCC is given to illustrate the high tracking accuracy. The output capacitor of the per-stage DC/DC converter is reduced significantly, and do not provide instantaneous pulse power. Finally, a 500 W peak power with 100-500 Hz pulse load of PPS is built to verify the proposed HCC strategy. Experimental results show that the proposed dual-inductance ASU could eliminate output current spikes effectively and improve the stability of bus voltage in different pulse duty cycle and PRF.

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Ping Yang (Member, IEEE) received the Ph.D. degree in electrical engineering from Southwest Jiaotong University, China, in 2013. From 2013 to 2014, she was a Research Associate with the Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Hong Kong. She has been an Associate Professor of Electronic Engineering with Southwest Jiaotong University. Her current research interests include modulation and control strategy of power electronic systems.

Xi Chen (Student Member, IEEE) was born in Sichuan, China, in 1994. He received the B.S. degree in electronic engineering from Southwest Jiaotong University, Chengdu, China, in 2017, where he is currently pursuing the M.S. degree with the School of Electrical Engineering. His research interests include modeling and control techniques of switching dc–dc converter.

Rongqian Chen was born in Guangdong, China, in 1999. He is currently pursuing the B.S. degree in automation from Southwest Jiaotong University, Chengdu, China. His research interests include control techniques, embedded systems, machine learning, and robotics.

Yusheng Peng received the B.S. degree in electronic engineering from Southwest Jiaotong University, Chengdu, China, in 2019, where he is currently pursuing the master's degree. His research interest includes multi-port converter topologies for self-powered technology of wireless sensor networks.

Songrong Wu received the Ph.D. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2014. He has been an Associate Professor of Electronic Engineering with Southwest Jiaotong University. His current research interests include power electronics technology, high frequency switching power supply technology, railway traction, and transmission.

Jianping Xu (Member, IEEE) received the B.S. and Ph.D. degrees in electronic engineering from the University of Electronics Science and Technology of China, Chengdu, China, in 1984 and 1989, respectively. Since 1989, he has been with the School of Electrical Engineering, Southwest Jiaotong University, Chengdu, where he has been a Professor since 1995. From November 1991 to February 1993, he was with the Department of Electrical Engineering, University of Federal Defense, Munich, Germany, as a Visiting Research Fellow. From February 1993 to July 1994, he was with the Department of Electrical Engineering and Computer Science, University of Illinois at Chicago, Chicago, IL, USA, as a Visiting Scholar. His research interests include the modeling, analysis, and control of power electronic systems.