COMPENG 3DQ5: Digital Systems Design Take-Home Exercise 4
10/20/2021 - Thursday - Group 55
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For this exercise, there were 4 main steps that needed to be done. These 4 steps were the even address write forward, even address read backwards, odd address write backwards and odd address read forward. Since this exercise involves reading the SRAM from the largest address (18'h3FFFF) to 0, there were some modifications that needed to be made from experiment 4. Firstly, our logic variable for BIST_expected_data needed to be modified, since it would not work if we are reading from the largest address to the smallest. For this, we made two variables, BIST_expected_data_fw and BIST_expected_data_bw (fw and bw are for forwards and backwards, respectively) that is the value of BIST_address - 4 and BIST_address + 4. A difference of 4 between BIST_address and the BIST_expected_data variables is necessary here, as the SRAM is delayed by 2 clock cycles and we are incrementing / decrementing by 2 since we are only reading / writing on even or odd addresses at any given time. These variables ensure that we can check for mismatches when reading in either the forwards or backwards direction. In addition to these changes, more states were added, since we are making more cycles than experiment 4.

The states that were added were S_WRITE_EVEN_CYCLE, S_READ_EVEN_CYCLE, S_WRITE_ODD_CYCLE and S_READ_ODD_CYCLE, as well as more delay states, S_DELAY_1 through S_DELAY_8. When cycling through states, our design first writes on the even addresses from 0 to 3FFFE (S_WRITE_EVEN_CYCLE), then reads from even addresses 3FFFE to 0 (S_READ_EVEN_CYCLE). Then it writes on odd addresses 3FFFF to 1 (S_WRITE_ODD_CYCLE), then it reads from odd addresses 1 to 3FFFF (S_READ_ODD_CYCLE). In between read and write states, we have 2 delay states present per cycle (S_DELAY_1 through S_DELAY_8), and the delay states ensure the BIST_address variable is correctly set, so that the next cycle starts on the correct address. Finally, at the end, our design goes from address 3FFFF in S_READ_ODD_CYCLE to address 3 in S_DELAY_8, as the last 2 delay states are for the last 2 clock cycles of the SRAM, to verify the last addresses in the SRAM are correct.