Yueqiao Wang

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**Computer Architecture & OS New Grad with hands-on RISC-V microkernel (OpenSBI/PLIC), kernel-level programming/debug (QEMU/GDB), and architecture-level simulation (gem5/Ramulator/uPIMulator);   
delivers reproducible performance analyses (Roofline, Omniperf/MFMA) in C/C++ on Linux**

**Education**

Bachelor of Science, Computer Engineering 05/2026

**Rose-Hulman Institute of Technology | Terre Haute, IN GPA:3.28/4.00**

* Honors: RHIT Dean’s List, Rose-Hulman Merit Scholarship
* Minor: Computer Science & Economics (in progress)
* Certificate: Semiconductor Materials and Devices (in progress)
* Related Courses: Computer Architecture I & II; Advanced Computer Architecture; High Performance Computing & AI; Semiconductor Physics; Signal Processing; Signals & Systems; Circuit and System; Control System; Electronic Device Modeling; Digital System; High-Speed Digital Design; Embedded Systems; Operating Systems; Communication Networks; Object-Oriented Software/Web Development; Competitive Programming; Data Structures & Algorithm; Principles of Design; Technical Communication

**Skills**

**Language**: Native Chinese, Professional English

**Programming & System**: Assembly, Verilog, bash, shell, linker script, C, C++, CMake, GCC, Java, Python, HTML, JavaScript, CSS, React, MATLAB & Simulink, Unix System Operation, Linux, Debian, Ubuntu, MacOS

**Software Development**: Git, GitHub, GitHub Action, GitLab, Docker, AI-Assisted Development

**General Hardware**: Finite State Machines (FSM), FPGA, Quartus Prime, ModelSim Simulation; Instrumentation, Programmable Power Supply & Load, Oscilloscope, Multimeter, Function Generator

**Computer Architecture**: Verilog, Micro Architecture,Instruction Set Architecture, Silicon Platforms, RTL Simulation, Cycle-Accurate Simulators, Gem5, Ramulator, ZSim, uPIMulator; Performance & Power Analysis; Research & Experimental Design; Microcontroller Programming, Embedded C Development, Driver Development, Communication Protocol (UART, I2C, SPI, JTAG)

**High-Performance Computing:** Performance Metrics, Roofline Analysis, Analytical Modeling, HPC Profiling,

**Parallel Computing**: Multi-GPU Processing, Matrix-Fused Multiply Accumulate (MFMA)

**Signals & Systems:** Fourier Series & Transform, Frequency Domain Analysis, Filter Design, Feedback Control Systems, Z-Transform & Discrete-Time Systems, Digital Signal Processing Implementation

**Networking:** TCP/IP, OSI Model, Signal Encoding, Error Detection, ARQ Protocols, Sliding Window Protocols, Network Switching & Routing, Multiplexing, Subnetting, Ethernet, Wireless Networks, Medium Access Control (MAC)

**Operating System:** Kernel-Level Programming & Debug, Multi-Thread/Process Programming, System Call, Interrupt, Process Creation & Scheduling, Memory Virtualization, Virtual Memory Management, File System, Concurrency & Synchronization, Low-Level System Security & Access Control, Drivers & Bring-up, interrupts, PLIC, linker scripts, board-level validation; CI via reproducible scripts (Bash/Python/Docker)

**System Engineering:** System Validation & Verification, Unit Test, Functional Architecture Modeling, Test-Driven Development, Agile Development

**AI & Machine Learning:** Transformer-Based Neural Networks (TNN), Attention Mechanisms, Multilayer Perceptron, AI Model Training & Inference, Running AI Workloads on HPC Systems, Local Model Deployment

**Engineering Design & Ethics:** Open-Ended Project Management, Team Collaboration & Conflict Management, Stakeholder-Requirement Analysis, Technical Report Writing & Poster Presentation, Ethical Decision-Making

**Other**: Data Analysis, Problem-Solving, Analytical Skills, SolidWorks, 3D Modeling & Printing, Teamwork, Adaptability

**Research Experiences**

**MorpheOS: Teaching-Focused RISC-V Microkernel, Operating System 06/2025 – Present***Rose-Hulman Institute of Technology, Terre Haute, IN*

* Designed and implemented core microkernel components (boot process, board bring-up, trap/exception handling, timer-driven preemption, and PLIC-based external interrupts) on a RISC-V SoC platform; Integrated OpenSBI (FW\_DYNAMIC) and verified the system on QEMU with GDB; Developed unit tests into the pipeline; Authored extensive documentation, lab exercises, and code comments to support an educational OS stack; Maintained reproducible build tooling (Makefiles, scripts) for student use; Collaborated remotely under faculty mentorship
* Practiced low-level debugging and development skills (RISC-V assembly, QEMU, OpenSBI, GDB, linker scripts, interrupt controller configuration) while contributing to a teaching-focused open-source project
* Researching & Designing memory and page table layout, Hypervisors Potential, and context switch speed-up method

**Open-Source Educational Robotics, Robotics,** [***LINK***](https://merl-rose-hulman.github.io/) **05/2024–Present***Rose-Hulman Institute of Technology, Terre Haute, IN*

* Designed and programmed human-interactive robot frameworks using various microcontrollers (Arduino, Raspberry Pi, etc.); Implemented software architectures using C, JavaScript, and Python; Used Cadence OrCAD for Printed Circuit Board design; Designed 3D models and mechanical components in SolidWorks
* As the Student Researcher Manager, elevated team throughput by introducing a Git branching model, an online TODO tracker, a shared team calendar, and an internal wiki system; Mentored 5 new student researchers in a multidisciplinary team under faculty supervision, improving onboarding time by 20%; Maintained Daily Operations
* Built end-to-end embedded systems (circuit design & soldering, HW–SW integration, product design); Deepened proficiency with microcontroller, embedded C programming, CAD workflows, and technical documentation through iterative development cycles

**Processing-In-Memory DPU Scaling Analysis, Computer Architecture 11/2024 – 03/2025**

* Conducted simulation and analysis on Data Processing Unit (DPU) configurations in UPMEM Processing-In-Memory (PIM) systems; Simulated various DPU scaling configurations (1–16 DPUs per rank) using uPIMulator, a cycle-accurate simulator; Evaluated performance metrics from benchmark simulation results such as execution latency, throughput, and memory bandwidth utilization
* Automated batch simulations & data reduction with Bash/Python, producing reproducible configs and CSV summaries [4 configs × 6 runs]; Documented trade-offs and configuration guidelines for computational-memory systems
* Explored Gem5, Ramulator, ZSim, uPIMulator, and other simulation tools; Gained hands-on experience in computer architecture research, experimentation, and performance modeling; Applied Linux/Unix-based system command line operation

**Project Experiences**

**Performance Metrics & Optimizer Study, HPC 04/2025 – 05/2025**

* Built a reproducible performance-metrics pipeline to profile matrix- and memory-intensive workloads; Implemented MATLAB/Python search script to find near-optimal configurations under power/cost constraints (grid + heuristic local search); Produced comparison reports based on throughput/latency/energy to guide design decisions
* Worked in a team of 2; Focused on High-Performance Computing (HPC) performance profiling and script creation; Increased the search efficiency by over 100% from hand calculation
* Delivered our design to the class and professor; Authored post-mortem and teaching notes that dissected modeling, scaling limits, and “memory-wall” sensitivity; Strengthened skills in profiling, metric design, optimization algorithms, and experiment reproducibility; Familiarized with real-world HPC tasks operation, Unix System operation on AMD HPC

**Socket Chat Program, Network Programming 09/2024 – 11/2024**

* Developed an IP-based two-person chat application using TCP sockets in C; Implemented custom network protocols over UDP (with additional messaging features over UDP)
* Collaborated in a 2-person team, splitting the workload 50/50; Took primary responsibility for designing and implementing a custom, reliable UDP messaging protocol on top of sockets, ensuring message ordering and integrity
* Strengthened skills in Networking Protocol, low-level network programming (sockets API), protocol design, and error handling in C; Improved debugging techniques, packet capturing for networked systems; Honed teamwork through pair programming and testing

**LazyPlant, Embedded System,** [***LINK***](https://github.com/WillWYQ/LazyPlant) **11/2023 – 03/2024**

* Created an automated plant care system with embedded C software on a TI MSP432 microcontroller; Optimized plant conditions through water pump, grow light, and fan control based on soil moisture, light, and temperature monitoring, and configurable profiles; Developed driver for sensors and NeoPixel LED; Utilized interrupt routing, ADC sensor reading; Instrumented oscilloscope-based validation
* Led a team of two as the main designer and software contributor; Collaborated effectively to integrate mechanical and hardware components and enhance system performance
* Practiced embedded system firmware development, low-power mode control, data protocol (SPI, UART, I2C), and real-time clock scheduling; Improved skills in embedded system design, hardware automation, and hardware debugging (Oscilloscope and other equipment), as well as project leadership and documentation

**Leadership & Teaching Experience**

**Marker Lab – Archivist 03/2023 – Present**

**International Student Association – Treasurer 03/2023 – 06/2025**

**Embedded Systems Development – Teaching Assistant 11/2024 – 03/2025**

**Direct Current Circuits – Lab Assistant 03/2024 – 05/2024**

**Object-Oriented Software Development – Teaching Assistant 09/2023 – 11/2023**