

Compare Results

Old File:

USB_PD_R3_1 V1.8 2023-04_Ch7.pdf

88 pages (2.57 MB)

13/10/2023 19:36:07

versus

New File:

USB_PD_R3_2 V1.0 2023-10_Ch 7.pdf

100 pages (2.47 MB)

31/10/2023 18:09:01

Total Changes

1897

Text only comparison

Content

856
564
477

Replacements
Insertions
Deletions

Styling and Annotations

0 Styling
0 Annotations

[Go to First Change \(page 1\)](#)

7. Power Supply

7.1 Source Requirements

7.1.1 Behavioral Aspects

A USB PD Source exhibits the following behaviors:

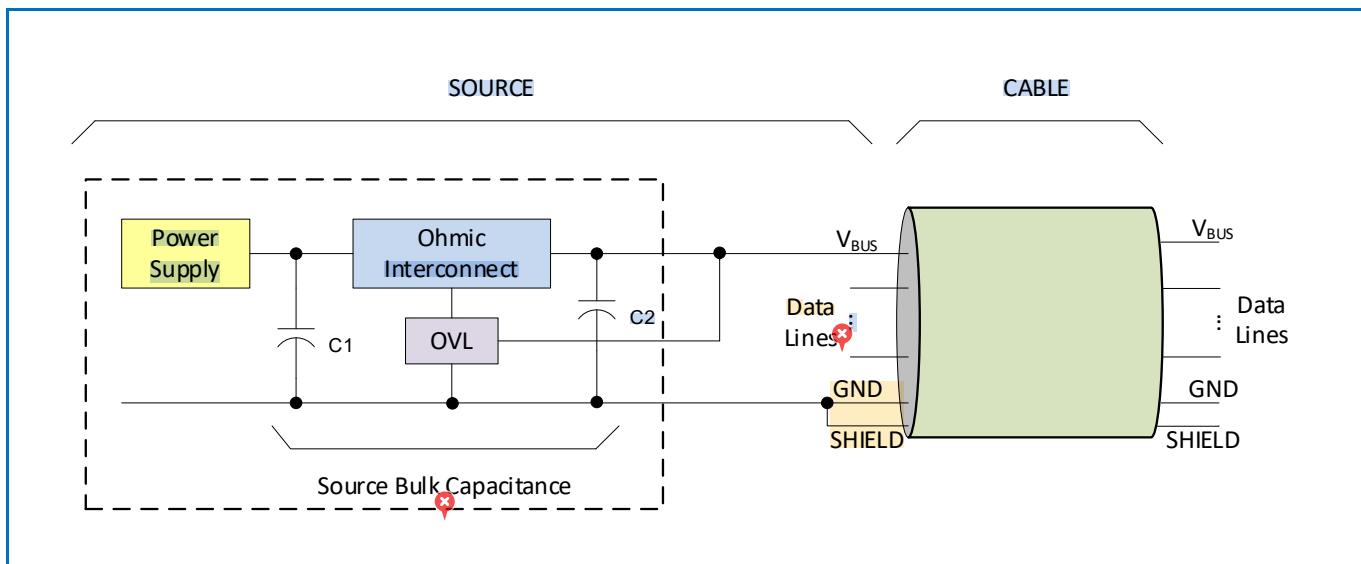
- **Shall** supply [\[USB Type-C 2.3\]](#) USB Type-C® Current method to V_{BUS} while in a Default Contract or Implicit Contract.
- **Shall** follow the requirements as specified in [Section 7.1.5 “Response to Hard Resets”](#) when **Hard Reset** Signaling is received.
- **Shall** control V_{BUS} Voltage transitions as bound by undershoot, overshoot and transition time requirements.

7.1.2 Source Bulk Capacitance

The Source bulk capacitance **Shall Not** be placed between the transceiver isolation impedance and the USB receptacle. The Source bulk capacitance consists of C1 and C2 as shown in [Figure 7-1 “Placement of Source Bulk Capacitance”](#). The Ohmic Interconnect might consist of PCB traces for power distribution or power switching devices. The Ohmic Interconnect might also be part of the circuit implemented by the Source to limit its V_{BUS} output Voltage (OVL) as described in [Section 7.1.7.5 “Output Voltage Limit”](#). Though a Source **Shall** limit its output Voltage, a Sink **Shall** implement Sink OVP as described in [Section 7.2.9.2 “Input Over Voltage Protection”](#) to protect against excessive V_{BUS} input Voltage. The capacitance might be a single capacitor, a capacitor bank or distributed capacitance. If the power supply is shared across multiple ports, the bulk capacitance is defined as [cSrcBulkShared](#). If the power supply is dedicated to a single Port, the minimum bulk capacitance is defined as [cSrcBulk](#).

The Source bulk capacitance is allowed to change for a newly negotiated power level. The capacitance change **Shall** occur before the Source is ready to operate at the new power level. During a Power Role Swap, the Default Source **Shall** transition to Swap Standby before operating as the new Sink. Any change in bulk capacitance required to complete the Power Role Swap **Shall** occur during Swap Standby.

Figure 7-1 “Placement of Source Bulk Capacitance”



7.1.3 Types of Sources

Consistent with the Power Data Objects discussed in [Section 6.4.1 “Capabilities Message”](#), the power supply types that are available as Sources in a USB Power Delivery System are:

- The Fixed Supply PDO exposes well-regulated fixed Voltage power supplies. Sources **Shall** support at least one Fixed Supply capable of supplying **vSafe5V**. The output Voltage of a Fixed Supply **Shall** remain within the range defined by the relative tolerance **vSrcNew** and the absolute band **vSrcValid** as listed in [Table 7.25 “Source Electrical Parameters”](#) and described in [Section 7.1.8 “Output Voltage Tolerance and Range”](#).
- The Variable Supply (non-Battery) PDO exposes less well-regulated Sources. The output Voltage of a Variable Supply (non-Battery) **Shall** remain within the absolute maximum output Voltage and the absolute minimum output Voltage exposed in the Variable Supply PDO.
- The Battery Supply PDO exposes Batteries than can be connected directly as a Source to V_{BUS}. The output Voltage of a Battery Supply **Shall** remain within the absolute maximum output Voltage and the absolute minimum output exposed in the Battery Supply PDO.
- The Programmable Power Supply (PPS) Augmented PDO (APDO) exposes a Source with an output Voltage that can be adjusted programmatically over a defined range. The output Voltage of the Programmable Power Supply **Shall** remain within a range defined by the relative tolerance **vPpsNew** and the absolute band **vPpsValid**.
- The Adjustable Voltage Supply (AVS) Augmented PDO (APDO) exposes a Source with an output Voltage that can be adjusted programmatically over a defined range. The output Voltage of the Adjustable Voltage Source **Shall** remain within a range defined by the relative tolerance **vAvsNew** and the absolute band **vAvsValid**.

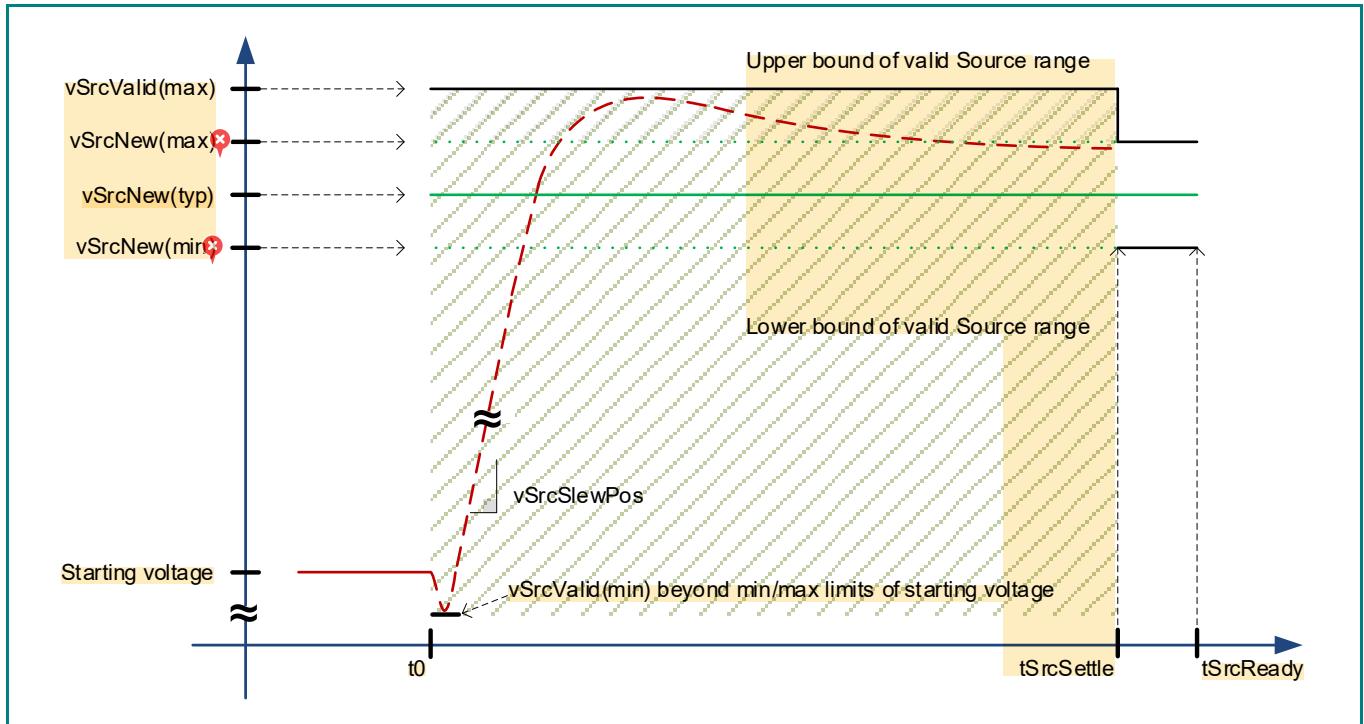
7.1.4 Source Transitions

7.1.4.1 Fixed Supply

7.1.4.1.1 Fixed Supply Positive Voltage Transitions

The Source **Shall** transition V_{BUS} from the starting Voltage to the higher new Voltage in a controlled manner. The negotiated new Voltage (e.g., 5V, 9V, 15V, ...) defines the nominal value for $vSrcNew$. During the positive transition the Source **Should** be able to supply the Sink standby current and the transient current to charge the total bulk capacitance on V_{BUS} . The slew rate of the positive transition **Shall Not** exceed $vSrcSlewPos$. The transitioning Source output Voltage **Shall** settle within $vSrcNew$ by $tSrcSettle$. The Source **Shall** be able to supply the negotiated power level at the new Voltage by $tSrcReady$. The positive Voltage transition **Shall** remain above $vSrcValid$ min of the previous contract and below $vSrcValid$ max of the new contract ([Figure 7-2 "Transition Envelope for Positive Voltage Transitions"](#)). The voltage **Shall** settle to $vSrcNew$ within $tSrcSettle$. The starting time, t_0 , in [Figure 7-2 "Transition Envelope for Positive Voltage Transitions"](#) starts $tSrcTransition$ after the last bit of the EOP of the $GoodCRC$ Message has been received by the Source.

[Figure 7-2 "Transition Envelope for Positive Voltage Transitions"](#)



At the start of the positive Voltage transition the V_{BUS} Voltage level **Shall Not** droop $vSrcValid$ min below either $vSrcNew$ (i.e., if the starting V_{BUS} Voltage level is not $vSafe5V$) or $vSafe5V$ as applicable.

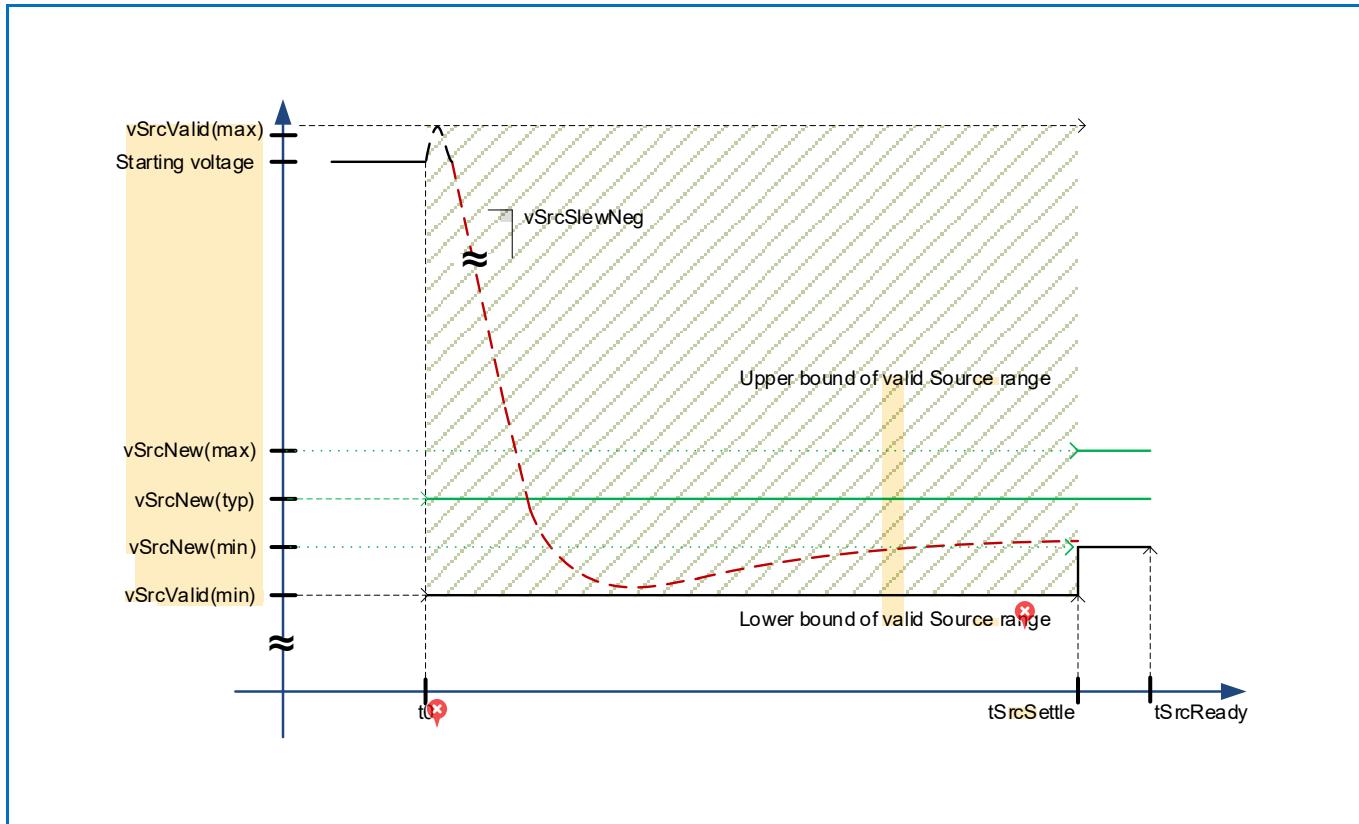
[Section 7.1.14 "Non-application of VBUS Slew Rate Limits"](#) lists transitions that are exempt from the $vSrcSlewPos$ limit.

7.1.4.1.2 Fixed Supply Negative Voltage Transitions

Negative Voltage transitions are defined as shown in [Figure 7-3 "Transition Envelope for Negative Voltage Transitions"](#) and are specified in a similar manner to positive Voltage transitions. [Figure 7-3 "Transition Envelope for Negative Voltage Transitions"](#) does not apply to $vSafe0V$ transitions. The slew rate of the negative transition **Shall Not** exceed $vSrcSlewNeg$. The negative Voltage transition **Shall** remain below $vSrcValid$ max of the previous

contract and above $vSrcValid$ min of the new contract, as shown in [Figure 7-3 “Transition Envelope for Negative Voltage Transitions”](#). The transitioning Source output Voltage **Shall** settle to $vSrcNew$ within $tSrcSettle$. The starting time, t_0 , in [Figure 7-3 “Transition Envelope for Negative Voltage Transitions”](#) starts $tSrcTransition$ after the last bit of the **EOP** of the **GoodCRC** Message has been received by the Source.

[Figure 7-3 “Transition Envelope for Negative Voltage Transitions”](#)



If the newly negotiated Voltage is $vSafe5V$, then the $vSrcValid$ limits **Shall** determine the transition window and the transitioning Source **Shall** settle within the $vSafe5V$ limits by $tSrcSettle$.

[Section 7.1.14 “Non-application of VBUS Slew Rate Limits”](#) lists transitions that are exempt from the $vSrcSlewNeg$ limit.

7.1.4.2 SPR Programmable Power Supply (PPS)

7.1.4.2.1 SPR Programmable Power Supply Voltage Transitions

The Programmable Power Supply (PPS) **Shall** transition V_{BUS} over the defined Voltage range in a controlled manner. The Output Voltage value in the Programmable RDO defines the nominal value of the PPS output Voltage after completing a Voltage change and **Shall** settle within the limits defined by $vPpsNew$ by $tPpsSrcTransSmall$ for steps smaller than or equal to $vPpsSmallStep$, or else, within the limits defined by $vPpsNew$ by $tPpsSrcTransLarge$, but only in case the Programmable Power Supply is not in CL mode. Any overshoot beyond $vPpsNew$ **Shall Not** exceed $vPpsValid$ at any time. Any undershoot beyond $vPpsNew$ **Shall Not** exceed $vPpsValid$ for currents not resulting in CL mode. The PPS output Voltage **May** change in a step-wise or linear manner and the slew rate of either type of change **Shall Not** exceed $vPpsSlewPos$ for Voltage increases or $vPpsSlewNeg$ for Voltage decreases. The nominal requested Voltage of all linear Voltage changes **Shall** equate to an integer number of LSB changes. An LSB change of the PPS output Voltage is defined as $vPpsStep$. A PPS **Shall** be able to supply the negotiated current level as it changes its output Voltage to the requested level. All PPS Voltage increases **Shall** result in a Voltage that is greater than or equal to the previous PPS output Voltage. Likewise, all PPS Voltage decreases **Shall** result in a Voltage that is less than or equal to the previous PPS output Voltage.

Since a Sink can draw current up to the negotiated APDO current level in case of a Voltage step, the Voltage might not increase to the requested level due to the power supply operating in CL mode. Likewise, since a Sink can have a battery connected to V_{BUS} , the Voltage might not decrease to the requested level due to the battery Voltage being higher than the output Voltage set point the Source is transitioning to. Were the Source to rely on checking the Voltage on V_{BUS} , in either case, to determine when its power supply is ready a PS_RDY would never be sent.

When the PPS Voltage steps up or down, a **PS_RDY** Message **Shall** be sent within:

- $tPpsSrcTransLarge$ after the last bit of the **GoodCRC** Message following the **Accept** Message for steps larger than $vPpsSmallStep$.
- $tPpsSrcTransSmall$ after the last bit of the **GoodCRC** Message following the **Accept** Message for steps less than or equal to $vPpsSmallStep$ provided that either the Voltage on V_{BUS} has reached $vPpsNew$ or the power supply is in CL mode.

When $vPpsNew$ is lower than the battery Voltage, or the Source's primary power is cut off the Sink **Shall** immediately disconnect its battery from V_{BUS} . In these situations, the output current could reverse polarity and the Sink is not allowed to source current (see [Section 7.2.1 "Behavioral Aspects"](#) and [Section 7.2.9 "Robust Sink Operation"](#)).

[Figure 7-4 "PPS Positive Voltage Transitions"](#) and [Figure 7-5 "PPS Negative Voltage Transitions"](#) below show the output Voltage behavior of a Programmable Power Supply in response to positive and negative Voltage change requests. The parameters $vPpsMinVoltage$ and $vPpsMaxVoltage$ define the lower and upper limits of the PPS range respectively (see [Table 10.11 SPR "Programmable Power Supply Voltage Ranges"](#) for required ranges).

$vPpsMinVoltage$ corresponds to Minimum Voltage field in the PPS APDO and $vPpsMaxVoltage$ corresponds to Maximum Voltage field in the PPS APDO. If the Sink negotiates for a new PPS APDO, then the transition between the two PPS APDOs **Shall** occur as described in [Section 7.3.1 "Transitions caused by a Request Message"](#).

Figure 7-4 “PPS Positive Voltage Transitions”

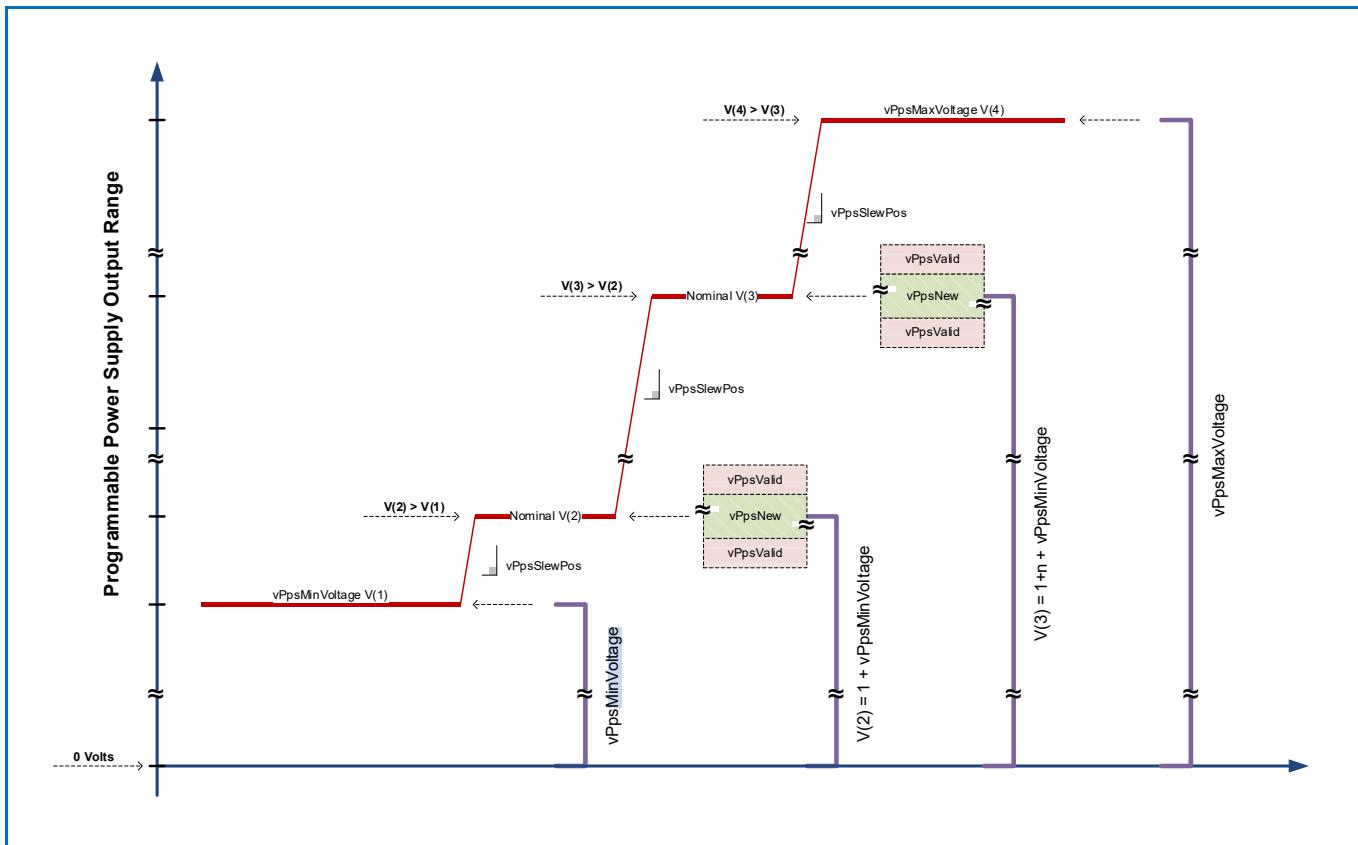
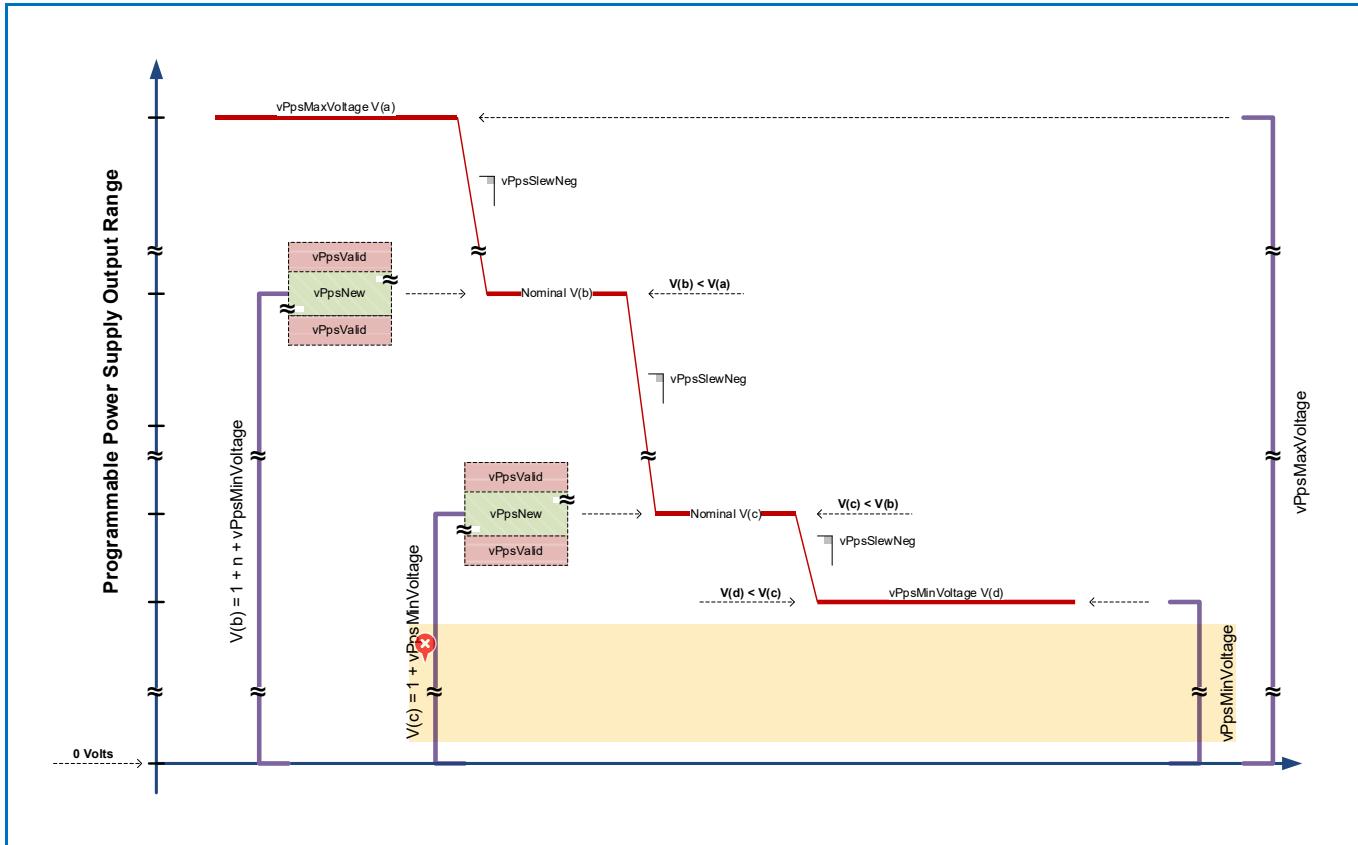
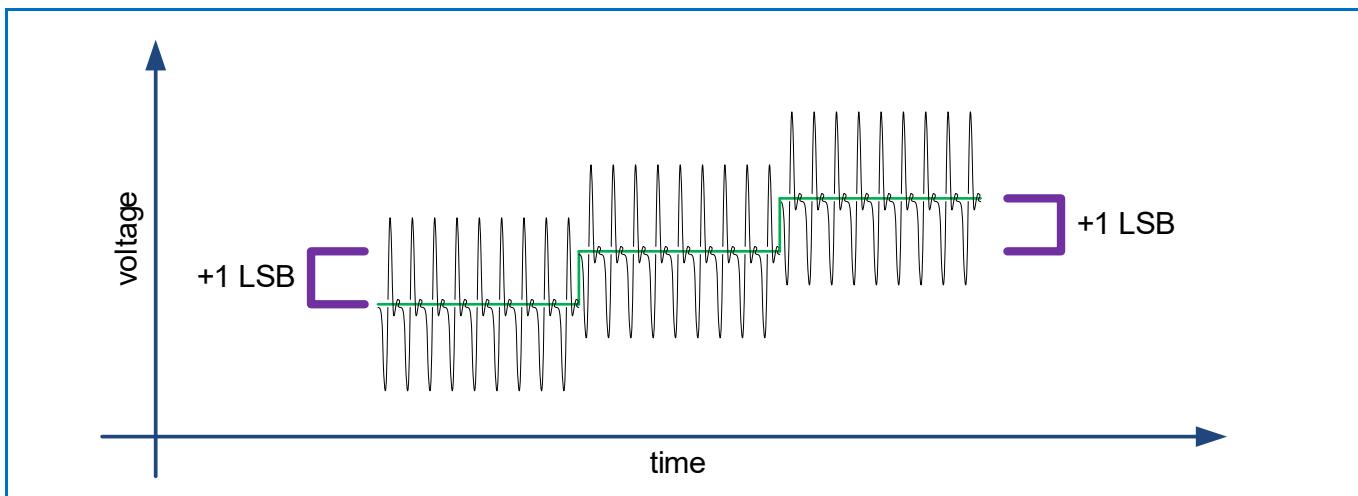


Figure 7-5 “PPS Negative Voltage Transitions”



✖ The PPS output Voltage ripple is expected to exceed the magnitude of one or more LSB as show in the [Figure 7-6 “Expected PPS Ripple Relative to an LSB”](#).

Figure 7-6 “Expected PPS Ripple Relative to an LSB”



[Section 7.1.14 “Non-application of VBUS Slew Rate Limits”](#) lists transitions that are exempt from the **vPpsSlewNeg** and **vPpsSlewPos** limits.

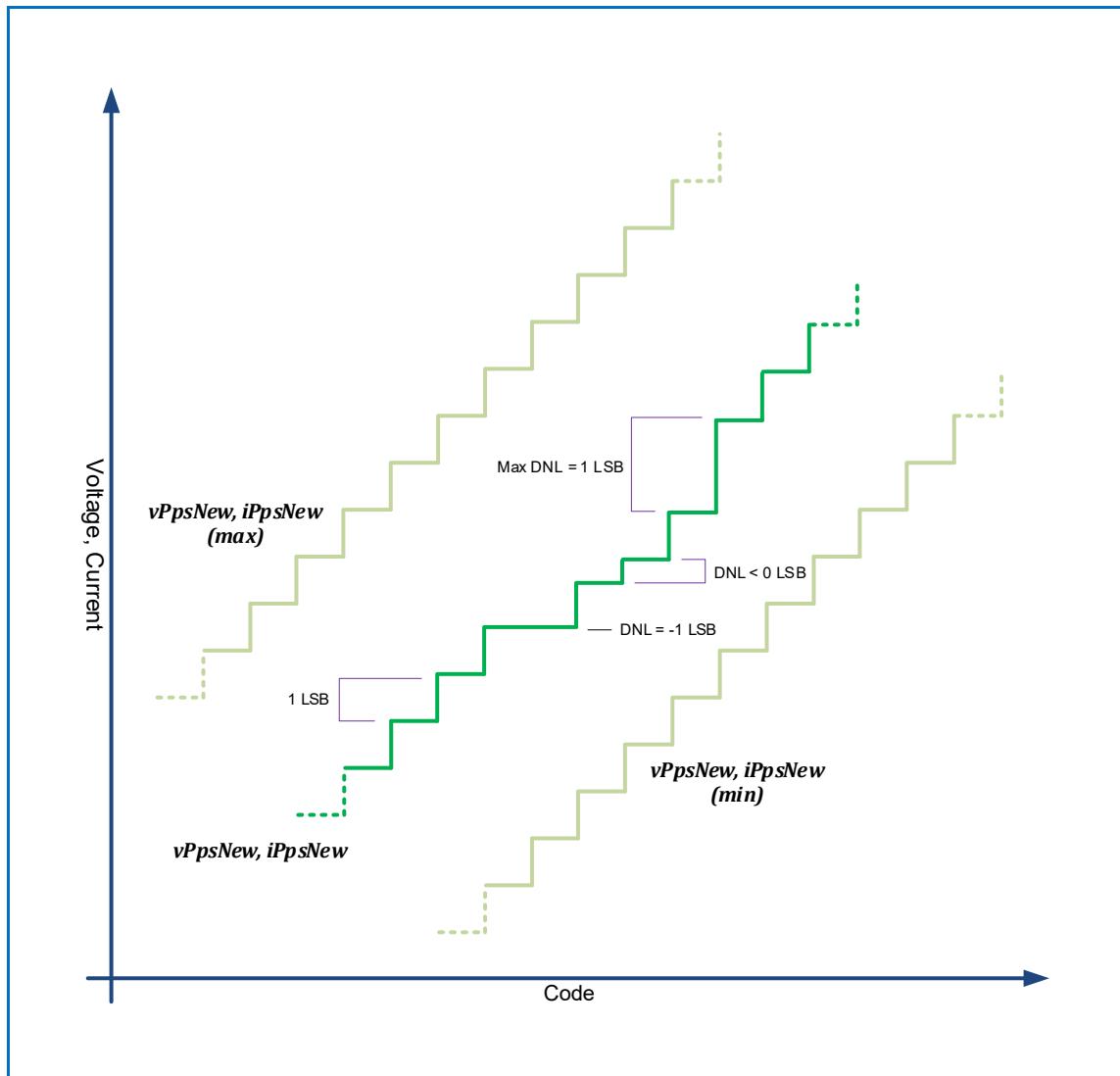
The PPS voltage and current discrete LSB steps have a **DNL** tolerance as shown in [Figure 7-7 "Allowed DNL errors and tolerance of Voltage and Current in PPS mode"](#) below. In absolute terms the step size of the LSB for both voltage and current is defined by **vPpsStep**, and **iPpsCLStep**, for voltage and current, respectively. Several examples of **Valid** LSB steps are shown in [Figure 7-7 "Allowed DNL errors and tolerance of Voltage and Current in PPS mode"](#):

- The upper end of the **DNL** error (+1 LSB) shows the case where one step is effectively skipped.
- The lower end of the **DNL** error (-1 LSB) shows the case where the voltage or current setpoint remained the same.

The ideal scenario for the **DNL** error (=0) matches the typical step size for the voltage or current.

The intent of **DNL** is to guarantee that changes to the voltage/current have the correct directionality, and that the maximum step size is clearly defined. Please note that the Source **Should** avoid scenarios where multiple consecutive steps have errors close to the Maximum and Minimum **DNL**.

Figure 7-7 "Allowed DNL errors and tolerance of Voltage and Current in PPS mode"



7.1.4.2.2

SPR Programmable Power Supply Current Limit

The Programmable Power Supply operating in SPR PPS Mode **Shall** limit its output current to the Operating Current value in the Programmable RDO when the Sink attempts to draw more current than the Output Current level. The programming step size for the Output Current is **iPpsCLStep**. All programming changes of the Operating Current **Shall** settle to the new Operating Current value within **tPpsCLProgramSettle**. The SPR PPS Operating Current regulation accuracy during Current Limit is defined as **iPpsCLNew**. The minimum programmable Current Limit level is **iPpsCLMin**. A Source that supports SPR PPS **Shall** support Current Limit programmability between **iPpsCLMin** and the Maximum Current value in the SPR PPS APDO. A Source which receives a request for current below **iPpsCLMin** **Should** reject the request. A Source that accepts a request for current below **iPpsCLMin** **Shall** set its current limit at 1A.

The response of an SPR PPS to a load change depends on the Operating mode of the SPR PPS and the magnitude of the load change. These dependencies lead to one of four possible responses of an SPR PPS to any load change. They are differentiated by the value of the PPS Status OMF before and after the load change:

- If the PPS Status OMF is cleared both before and after the load change, the SPR PPS responds solely by maintaining the output Voltage. The SPR PPS output Voltage **Shall** remain within **vPpsValid** range. The SPR PPS response to the load change **Shall** settle within the **vPpsNew** tolerance band by the time **tPpsTransient**. The Operating Mode Flag **Shall** remain cleared during the load change response of the SPR PPS.
- If the PPS Status OMF is cleared before the load change and set after the load change, the SPR PPS responds by reducing its output Voltage to limit the SPR PPS output current. The SPR PPS output current **Shall** stay within the **iPpsCVCTransient** range once it reaches the **iPpsCVCTransient** range. The SPR PPS response to the load change **Shall** settle within the **iPpsCLNew** tolerance band by the time **tPpsCVCTransient**. The Operating Mode Flag **Shall** be set when the SPR PPS load change response settles.
- If the PPS Status OMF is set both before and after the load change, the SPR PPS responds by adjusting its output Voltage to maintain the output current. The SPR PPS output current **Shall** stay within the **iPpsCLTransient** range. The SPR PPS response to the load change **Shall** settle within the **iPpsCLNew** tolerance band by the time **tPpsCLSettle**. The Operating Mode Flag **Shall** remain set during the load change response of the SPR PPS.
- If the PPS Status OMF is set before the load change and cleared after the load change, the PPS responds to the load change by increasing its output Voltage to **vPpsNew** and then maintaining it. The SPR PPS output Voltage **Shall** stay within the **vPpsCLCVTransient** range. The SPR PPS response to the load change **Shall** settle within the **vPpsNew** tolerance band by the time **tPpsCLCVTransient**. The Operating Mode Flag **Shall** be cleared when the PPS load change response settles.

The SPR PPS Source **Shall** maintain its output Voltage at the value requested in the PPS RDO for all static and dynamic load conditions except when in Current Limit operation. In response to any static or dynamic load condition during Current Limit operation that causes the SPR PPS output Voltage to drop below **vPpsShutdown** the Source **May** send **Hard Reset** Signaling and **Shall** discharge V_{BUS} to **vSafeOV** then resumes USB Default Operation at **vSafe5V**.

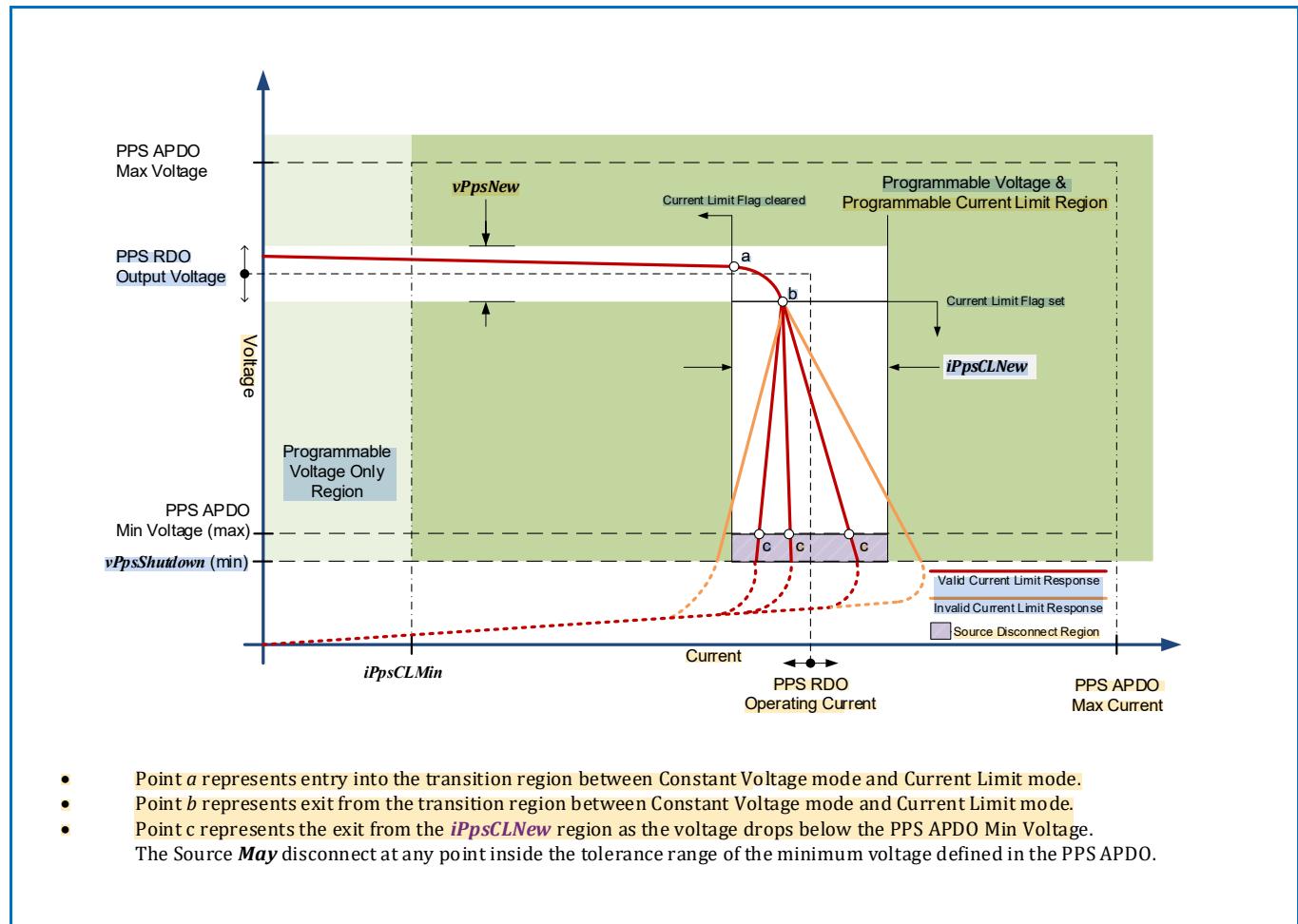
When the Sink attempts to draw more current than the Operating Current in the RDO, the Source **Shall** limit its output current. The current available from the Source during Current Limit mode **Shall** meet **iPpsCLNew**. The Sink **May Not** reduce its Operating Current request in the RDO when the PPS Status OMF is set.

Current limiting **Shall** be performed by the SPR PPS Source. Sinks that rely on PPS Current Limiting **Shall** meet the requirements of **Section 7.2.9 “Robust Sink Operation”**. The Source **Shall Not** shutdown or otherwise disrupt the available output power while in Current Limit mode unless another protection mechanism as outlined in **Section 7.1.7 “Robust Source Operation”** is engaged to protect the Source from damage.

An SPR PPS Source that is operating in Current Limit **Shall Not** change its setpoint in a manner that exceeds **iPpsCLLoadStepRate** or **iPpsCLLoadReleaseRate**.

The relationship between SPR PPS programmable output Voltage and SPR PPS programmable Current Limit **Shall** be as shown in [Figure 7-8 “SPR PPS Programmable Voltage and Current Limit”](#). The transition between the Constant Voltage mode and the Current Limit mode occurs between points *a* and *b*. The PPS Status OMF **Shall** be set or cleared within this region. In Current Limit mode when the load resistance changes, the output current of the Source **Shall** stay within *iPpsCLNew*. The proper behavior is represented by point *c*.

 [Figure 7-8 “SPR PPS Programmable Voltage and Current Limit”](#)

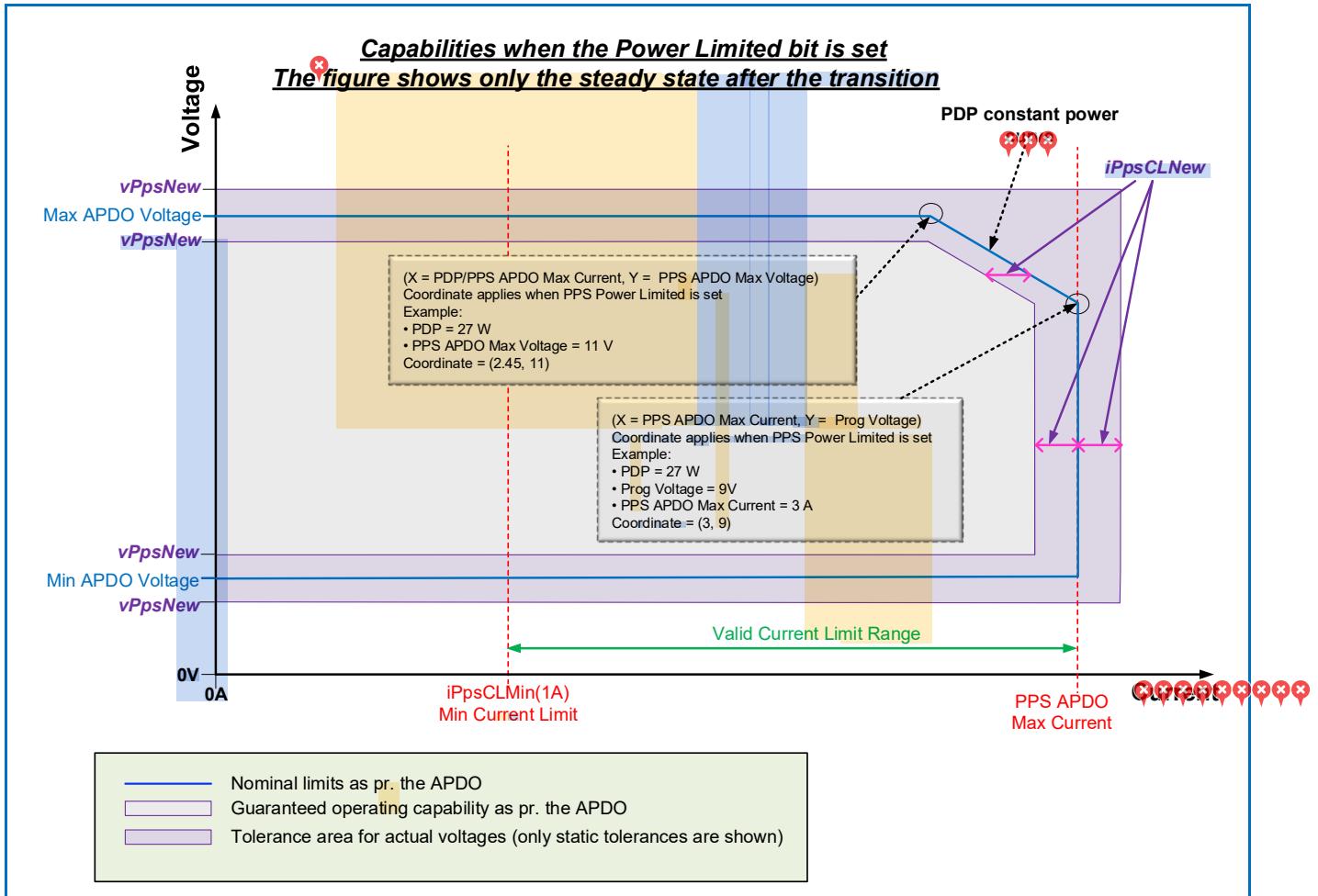


7.1.4.2.3 SPR PPS Constant Power Mode

In Constant Power mode (when the PPS Power Limited bit is set) the Source **May** supply power that exceeds the Source's rated PDP. Sinks **May** limit their Operating Current request in the RDO and **Shall** meet the requirements of [Section 7.2.9 “Robust Sink Operation”](#).

The tolerances along the Constant Power Curve **Shall Not** extend into the Guaranteed Capability Area of [Figure 7-9 “SPR PPS Constant Power”](#).

Figure 7-9 “SPR PPS Constant Power”



7.1.4.3 Adjustable Voltage Supply (AVS)

7.1.4.3.1 Adjustable Voltage Supply Voltage Transitions

⚠️ The Adjustable Voltage Supply (AVS) **Shall** transition V_{BUS} over the defined Voltage range in a controlled manner. The Output Voltage value in the AVS RDO defines the nominal value of the AVS output Voltage after completing a Voltage change and **Shall** settle within the limits defined by **vAvsNew** by **tAvsSrcTransSmall** for steps smaller than or equal to **vAvsSmallStep**, or else, within the limits defined by **vAvsNew** by **tAvsSrcTransLarge** for steps larger than **vAvsSmallStep**. Any overshoot beyond **vAvsNew Shall Not** exceed **vAvsValid** at any time. Any undershoot beyond **vAvsNew Shall Not** exceed **vAvsValid** at any time. The AVS output Voltage **May** change in a stepwise or linear manner and the slew rate of either type of change **Shall Not** exceed **vAvsSlewPos** for Voltage increases or **vAvsSlewNeg** for Voltage decreases. The nominal requested Voltage of all linear Voltage changes **Shall** equate to an integer number of LSB changes. An LSB change of the AVS output Voltage is defined as **vAvsStep**. An AVS **Shall** be able to supply the negotiated current level as it changes its output Voltage to the requested level if the change of output Voltage is less than or equal to **vAvsSmallStep** relative to **vAvsNew**. All AVS Voltage increases **Shall** result in a Voltage that is greater than or equal to the previous AVS output Voltage. Likewise, all AVS Voltage decreases **Shall** result in a Voltage that is less than or equal to the previous AVS output Voltage. Any time the Source enters the AVS range of operation that Voltage transition is considered a Voltage step larger than **vAvsSmallStep**.

When the AVS Voltage steps up or down, a PS_RDY Message **Shall** be sent within:

- **tAvsSrcTransLarge** after the last bit of the **GoodCRC** Message following the **Accept** Message for steps larger than **vAvsSmallStep**.
- **tAvsSrcTransSmall** after the last bit of the **GoodCRC** Message following the **Accept** Message for steps less than or equal to **vAvsSmallStep** provided the Voltage on V_{BUS} has reached **vAvsNew**.

Figure 7-10 “AVS Positive Voltage Transitions” and **Figure 7-11 “AVS Negative Voltage Transitions”** below show the output Voltage behavior of an Adjustable Voltage Supply in response to positive and negative Voltage change requests. The parameters **vAvsMinVoltage** and **vAvsMaxVoltage** define the lower and upper limits of the AVS range respectively (see **Table 10.9 “SPR Adjustable Voltage Supply (AVS) Voltage Ranges”** and **Table 10.15 “EPR Adjustable Voltage Supply (AVS) Voltage Ranges”** for required ranges). **vAvsMinVoltage** corresponds to Minimum Voltage field in the AVS APDO and **vAvsMaxVoltage** corresponds to Maximum Voltage field in the AVS APDO.

Figure 7-10 “AVS Positive Voltage Transitions”

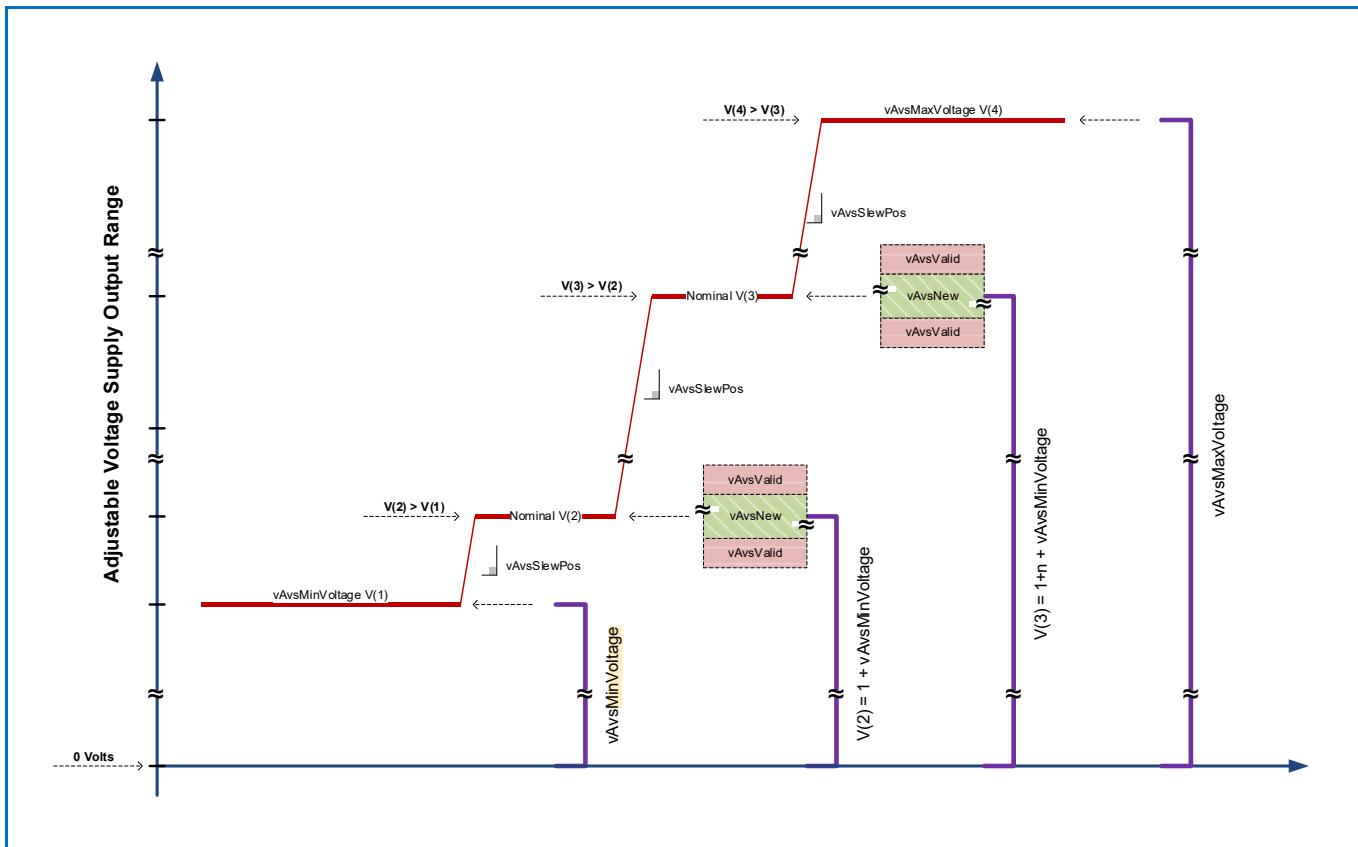
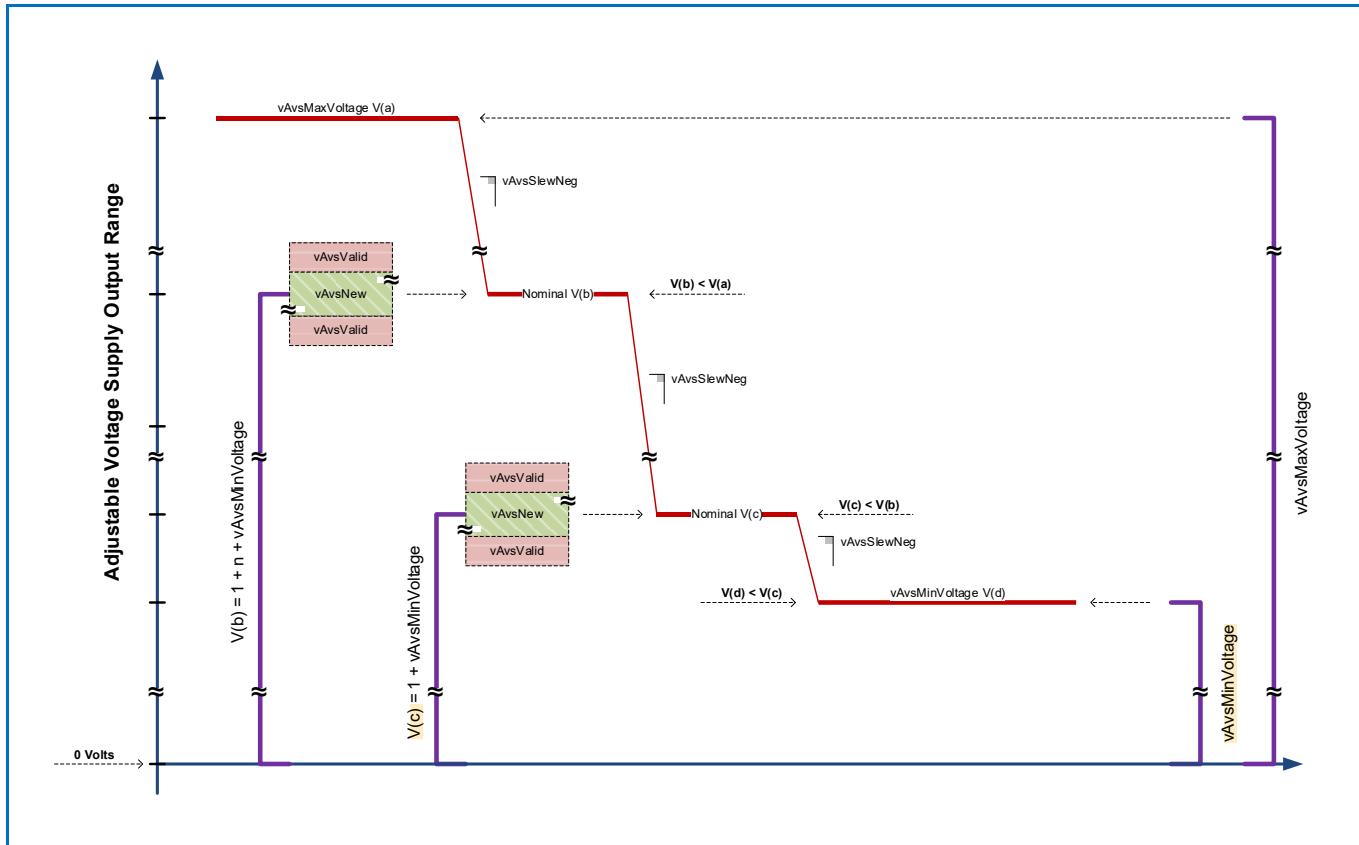
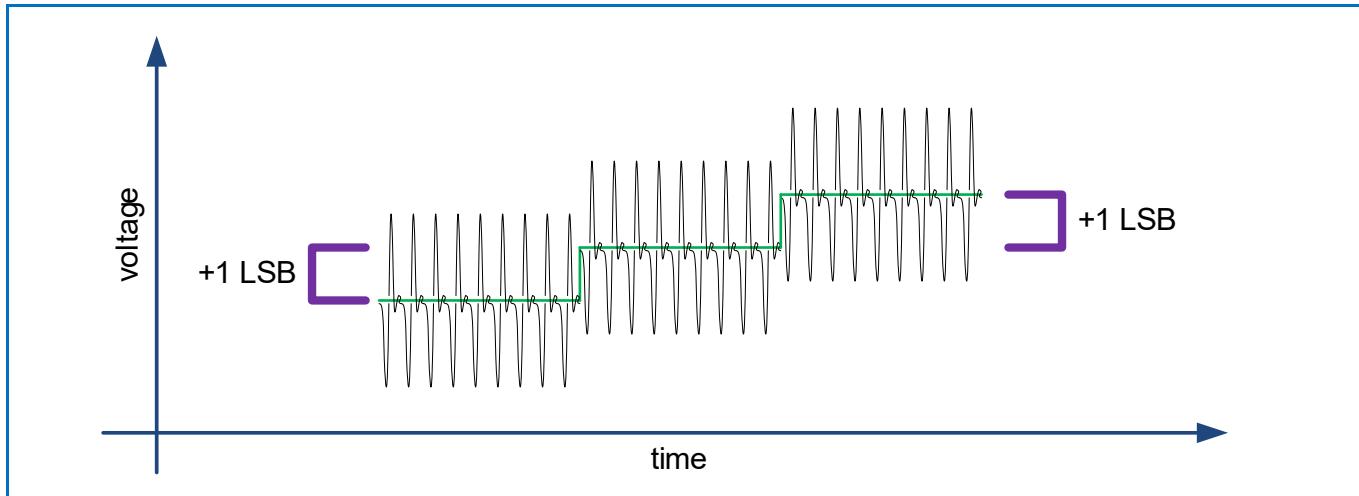


Figure 7-11 “AVS Negative Voltage Transitions”



The AVS output Voltage ripple is expected to exceed the magnitude of one or more LSB as show in the [Figure 7-12 “Expected AVS Ripple Relative to an LSB”](#).

Figure 7-12 “Expected AVS Ripple Relative to an LSB”



7.1.4.3.2

Adjustable Voltage Supply Current

The AVS **Shall** maintain its output Voltage at the value requested in the AVS RDO for all static and dynamic load conditions that do not exceed the Operating Current in the RDO. Unlike the SPR PPS programmable current, the AVS programmable power **May** range from zero to the PDP field value in the APDO.

7.1.5 Response to Hard Resets

Hard Reset Signaling indicates a communication failure has occurred and the Source **Shall** stop driving VCONN, **Shall** remove R_p from the VCONN pin and **Shall** drive V_{BUS} to **vSafe0V** as shown in [Figure 7-13 “Source V_{BUS} and Vconn Response to Hard Reset”](#). The USB connection **May** reset during a Hard Reset since the V_{BUS} Voltage will be less than **vSafe5V** for an extended period of time. After establishing the **vSafe0V** Voltage condition on V_{BUS}, the Source **Shall** wait **tSrcRecover** before re-applying VCONN and restoring V_{BUS} to **vSafe5V**. A Source **Shall** conform to the VCONN timing as specified in [\[USB Type-C 2.3\]](#).

Note: A Sink that enters Hard Reset can have **cSnkBulkPd** present until V_{BUS} drops below **vSafe0V**. The Source **Shall** take this into consideration.

Device operation during and after a Hard Reset is defined as follows:

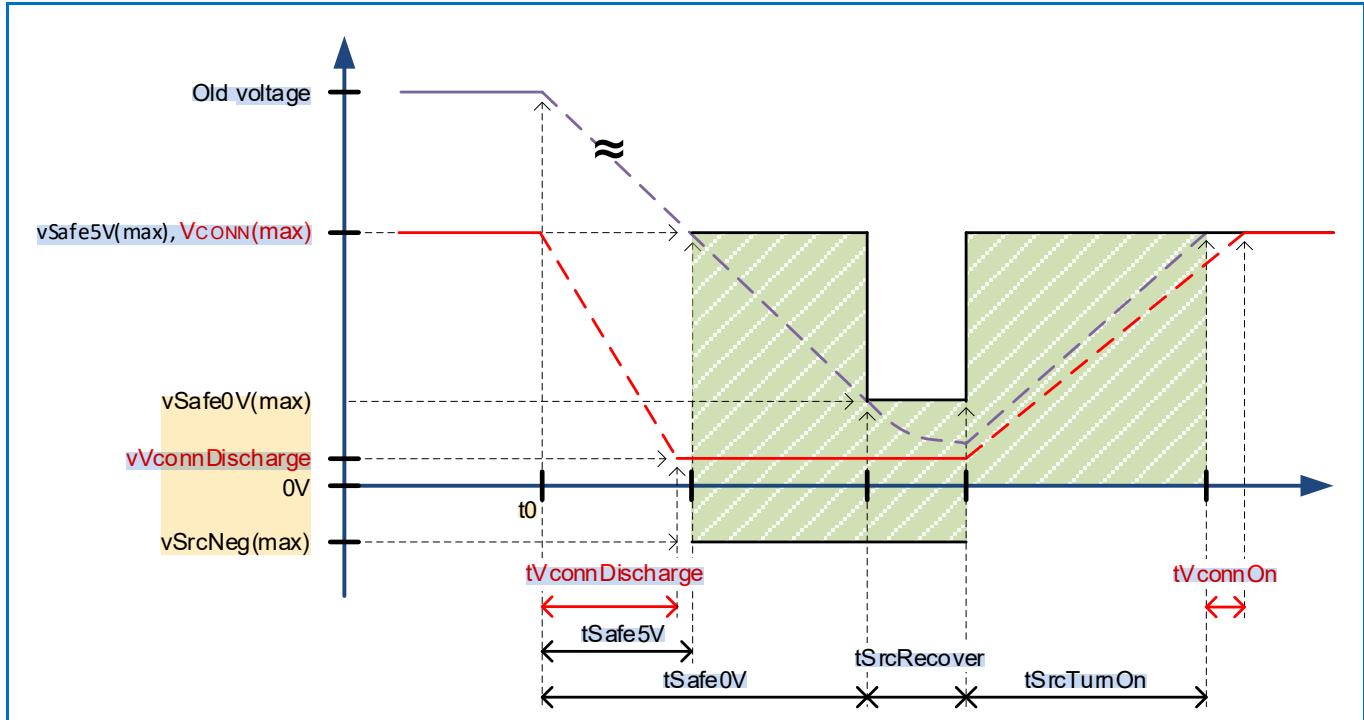
- Self-powered devices **Should Not** disconnect from USB during a Hard Reset (see [Section 9.1.2 “Mapping to USB Device States”](#)).
- Self-powered devices operating at more than **vSafe5V** **May Not** maintain full functionality after a **Hard Reset**.
- Bus powered devices will disconnect from USB during a Hard Reset due to the loss of their power source.

When a Hard Reset occurs the Source **Shall** stop driving VCONN, **Shall** remove R_p from the VCONN pin and **Shall** start to transition the V_{BUS} Voltage to **vSafe0V** either:

- **tPSHardReset** after the last bit of the **Hard Reset** Signaling has been received from the Sink or
- **tPSHardReset** after the last bit of the **Hard Reset** Signaling has been sent by the Source.

The Source **Shall** meet both **tSafe5V** and **tSafe0V** relative to the start of the Voltage transition as shown in [Figure 7-13 “Source V_{BUS} and Vconn Response to Hard Reset”](#).

Figure 7-13 “Source V_{BUS} and Vconn Response to Hard Reset”



VCONN will meet $tVconnDischarge$ relative to the start of the Voltage transition as shown in [Figure 7-13 “Source VBUS and Vconn Response to Hard Reset”](#) due to the discharge circuitry in the Cable Plug. VCONN **Shall** meet $tVconnOn$ relative to V_{BUS} reaching $vSafe5V$. Note $tVconnOn$ and $tVconnDischarge$ are defined in [\[USB Type-C 2.3\]](#).

7.1.6 Changing the Output Power Capability

Some USB Power Delivery negotiations will require the Source to adjust its output power capability without changing the output Voltage. In this case the Source **Shall** be able to supply a higher or lower load current within $tSrcReady$.

7.1.7 Robust Source Operation

7.1.7.1 Output Over Current Protection

Sources operating in SPR mode **Shall** implement over current protection to prevent damage from output current that exceeds the current handling capability of the Source. The definition of current handling capability is left to the discretion of the Source implementation and **Shall** take into consideration the current handling capability of the connector contacts. If the over current protection implementation does not use a Hard Reset or Error Recovery, it **Shall Not** interfere with the negotiated V_{BUS} current level.

After three consecutive over current events Source **Shall** go to *ErrorRecovery*.

Sources **Should** attempt to send *Hard Reset* signaling when over current protection engages followed by an *Alert* Message indicating an OCP event once an Explicit Contract has been established. The over current protection response **May** engage at either the port or system level. Systems or ports that have engaged over current protection **Should** attempt to resume *USB Default Operation* after determining that the cause of over current is no longer present and **May** latch off to protect the port or system. The definition of how to detect if the cause of over current is still present is left to the discretion of the Source implementation.

The Source **Shall** renegotiate with the Sink (or Sinks) after choosing to resume *USB Default Operation*. The decision of how to renegotiate after an over current event is left to the discretion of the Source implementation.

The Source **Shall** prevent continual system or port cycling if over current protection continues to engage after initially resuming either *USB Default Operation* or renegotiation. Latching off the port or system is an acceptable response to recurring over current.

During the over current response and subsequent system or port shutdown, all affected Source ports operating with V_{BUS} greater than *vSafe5V* **Shall** discharge V_{BUS} to *vSafe5V* by the time *tSafe5V* and *vSafe0V* by the time *tSafe0V*.

7.1.7.2 Over Temperature Protection

Sources **Shall** implement Over Temperature Protection (OTP) to prevent damage from temperature that exceeds the thermal capability of the Source. The definition of thermal capability and the monitoring locations used to trigger the over temperature protection are left to the discretion of the Source implementation.

In order to avoid reaching an OTP event, Sources **May** proactively reduce the available power being offered to the Sink, even though these offers might be lower than the Source would be expected to offer during normal thermal operating conditions. Prior to reducing power, the Source **Should** generate *Alert* Message indicating an Operating Condition Change and set the Temperature Status bit in the SOP *Status* Message to Warning (10b).

Sources **Should** attempt to send a *Hard Reset* message when OTP engages followed by an *Alert* Message indicating an OTP event once an Explicit Contract has been established. The OTP response **May** engage at either the port or system level. Systems or ports that have engaged OTP **Should** attempt to resume *USB Default Operation* and **May** latch off to protect the port or system.

The Source **Shall** renegotiate with the Sink (or Sinks) after choosing to resume *USB Default Operation*. The decision of how to renegotiate after an over temperature event is left to the discretion of the Source implementation.

The Source **Shall** prevent continual system or port cycling if over temperature protection continues to engage after initially resuming either *USB Default Operation* or renegotiation. Latching off the port or system is an acceptable response to recurring over temperature.

During the OTP and subsequent system or port shutdown, all affected Source ports operating with V_{BUS} greater than *vSafe5V* **Shall** discharge V_{BUS} to *vSafe5V* by the time *tSafe5V* and *vSafe0V* by the time *tSafe0V*.

7.1.7.3 vSafe5V Externally Applied to Ports Supplying vSafe5V

Safe operation mandates that Power Delivery Sources **Shall** be tolerant of **vSafe5V** being present on V_{BUS} when simultaneously applying power to V_{BUS}. Normal USB PD communication **Shall** be supported when this **vSafe5V** to **vSafe5V** connection exists.

7.1.7.4 Detach

A USB Detach is detected electrically using CC detection on the USB Type-C® connector. When the Source is Detached the Source **Shall** transition to **vSafe0V** by **tSafe0V** relative to when the Detach event occurred. During the transition to **vSafe0V** the V_{BUS} Voltage **Shall** be below **vSafe5V** max by **tSafe5V** relative to when the Detach event occurred and **Shall Not** exceed **vSafe5V** max after this time.

Sources operating in EPR mode need to avoid creating large differential Voltages at the connector. See Appendix H in the [\[USB Type-C 2.3\]](#) specification for background information. To achieve this, Sources operating in EPR mode, upon detecting a disconnect, **Shall** stop sourcing current and minimize V_{BUS} capacitance. There **May** continue to be current sourced from the Source Bulk Capacitance, but that **Should** also be minimized by disconnecting as much of the Source Bulk Capacitance as possible. For example, the Source can stop sourcing from the Power Supply and the C1 portion of the Source Bulk Capacitance in [Figure 7-1 “Placement of Source Bulk Capacitance”](#) by disabling the Ohmic Interconnect switch.

The Source **Should** detect the disconnect, stop sourcing current, and minimize the V_{BUS} capacitance as quickly as practical. If this is done after the CC contacts disconnect and before the V_{BUS} contacts disconnect there is less risk of large differential Voltages at the connector. Note that a USB-PD transmission by the Source during a disconnect event will delay disconnect detection by the Source.

7.1.7.5 Output Voltage Limit

The output Voltage of Sources **Shall** account for **vSrcNew, vSrcValid** or **vPpsNew, vPpsValid** or **vAvsNew, vAvsValid** as determined by the negotiated V_{BUS} value. Sources **Shall** meet applicable safety and regulatory requirements.

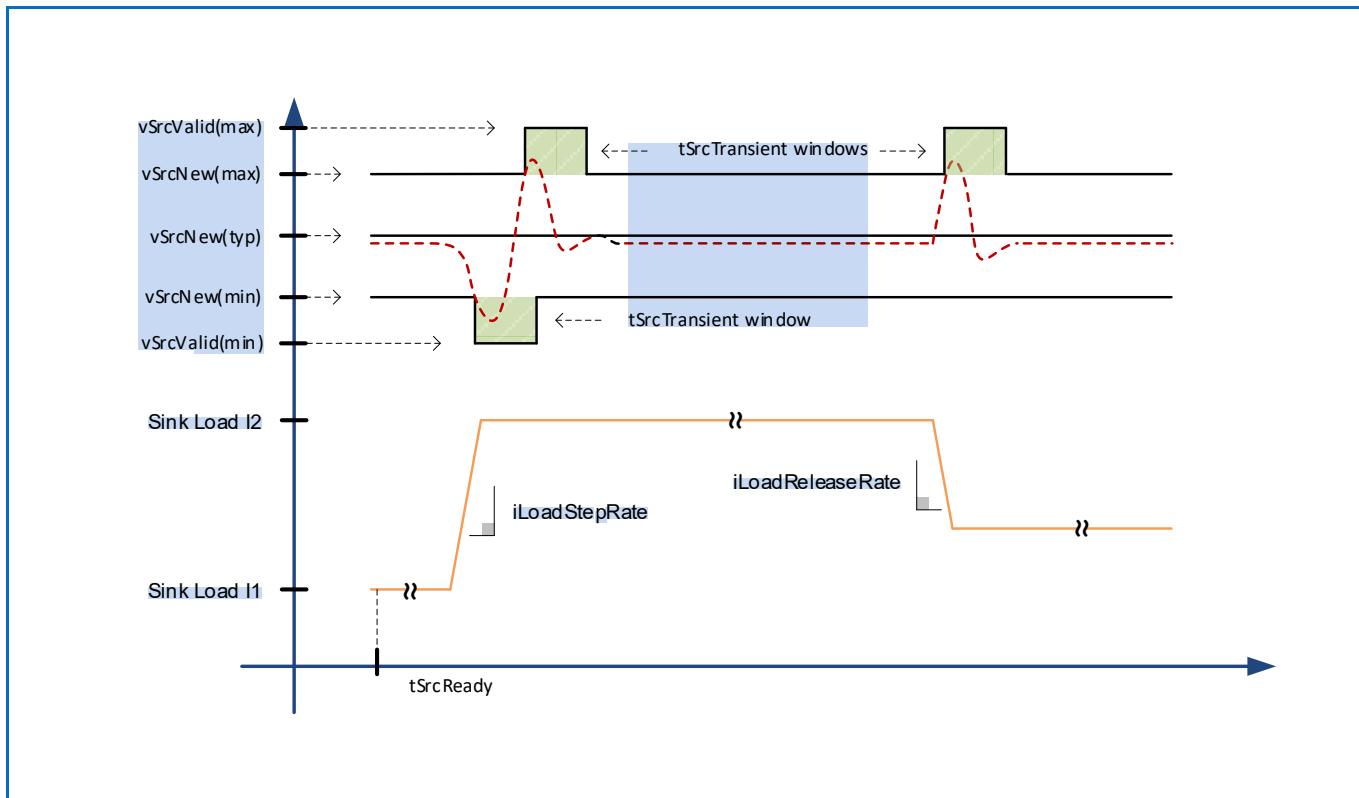


7.1.8 Output Voltage Tolerance and Range

After a Voltage transition is complete (i.e. after $t_{SrcReady}$) and during static load conditions the Source output Voltage **Shall** remain within the v_{SrcNew} or v_{Safe5V} limits as applicable. The ranges defined by v_{SrcNew} and v_{Safe5V} account for DC regulation accuracy, line regulation, load regulation and output ripple. After a Voltage transition is complete (i.e., after $t_{SrcReady}$) and during transient load conditions the Source output Voltage **Shall Not** go beyond the range specified by $v_{SrcValid}$. The amount of time the Source output Voltage can be in the band between either v_{SrcNew} or v_{Safe5V} and $v_{SrcValid}$ **Shall Not** exceed $t_{SrcTransient}$. Refer to [Table 7.25 "Source Electrical Parameters"](#) for the output Voltage tolerance specifications. [Figure 7-14 "Application of vSrcNew and vSrcValid limits after tSrcReady"](#) illustrates the application of v_{SrcNew} and $v_{SrcValid}$ after the Voltage transition is complete.

The v_{SrcNew} and $v_{SrcValid}$ limits **Shall Not** apply to V_{BUS} during the V_{BUS} discharge and switchover that occurs during a Fast Role Swap as described in [Section 7.1.13 "Fast Role Swap"](#).

Figure 7-14 "Application of vSrcNew and vSrcValid limits after tSrcReady"



The Source output Voltage **Shall** be measured at the connector receptacle. The stability of the Source **Shall** be tested in 25% load step increments from minimum load to maximum load and also from maximum load to minimum load. The transient behavior of the load current is defined in [Section 7.2.6 "Transient Load Behavior"](#). The time between each step **Shall** be sufficient to allow for the output Voltage to settle between load steps. In some systems it might be necessary to design the Source to compensate for the Voltage drop between the output stage of the power supply electronics and the receptacle contact. The determination of whether compensation is necessary is left to the discretion of the Source implementation.

7.1.8.1 Programmable Power Supply Output Voltage Tolerance and Range

After a Voltage transition of a Programmable Power Supply is complete (i.e. after *tPpsSrcTransSmall* or *tPpsSrcTransLarge*) and during static load conditions the Source output Voltage **Shall** remain within the *vPpsNew* limits. The range defined by *vPpsNew* accounts for DC regulation accuracy, line regulation, load regulation and output ripple. After a Voltage transition is complete (i.e. after *tPpsSrcTransSmall* or *tPpsSrcTransLarge*) and during transient load conditions the Source output Voltage **Shall Not** go beyond the range specified by *vPpsValid*. The amount of time the Source output Voltage can be in the band between *vPpsNew* and *vPpsValid* **Shall Not** exceed *tPpsTransient*.

7.1.8.2 Adjustable Voltage Supply Output Voltage tolerance and Range

After a Voltage transition of an Adjustable Voltage Supply is complete (i.e. after *tAvsSrcTransSmall* or *tAvsSrcTransLarge*) and during static load conditions the Source output Voltage **Shall** remain within the *vAvsNew* limits. The range defined by *vAvsNew* accounts for DC regulation accuracy, line regulation, load regulation and output ripple. After a Voltage transition is complete (i.e. after *tAvsSrcTransSmall* or *tAvsSrcTransLarge*) and during transient load conditions the Source output Voltage **Shall Not** go beyond the range specified by *vAvsValid*. The amount of time the Source output Voltage can be in the band between *vAvsNew* and *vAvsValid* **Shall Not** exceed *tAvsTransient*.

7.1.9 Charging and Discharging the Bulk Capacitance on V_{BUS}

The Source **Shall** charge and discharge the bulk capacitance on V_{BUS} whenever the Source Voltage is negotiated to a different value. The charging or discharging occurs during the Voltage transition and **Shall Not** interfere with the Source's ability to meet *tSrcReady*.

7.1.10 Swap Standby for Sources

Sources and Sinks of a Dual-Role Power Port **Shall** support Swap Standby. Swap Standby occurs for the Source after the Source power supply has discharged the bulk capacitance on V_{BUS} to *vSafe0V* as part of the Power Role Swap transition.

While in Swap Standby:

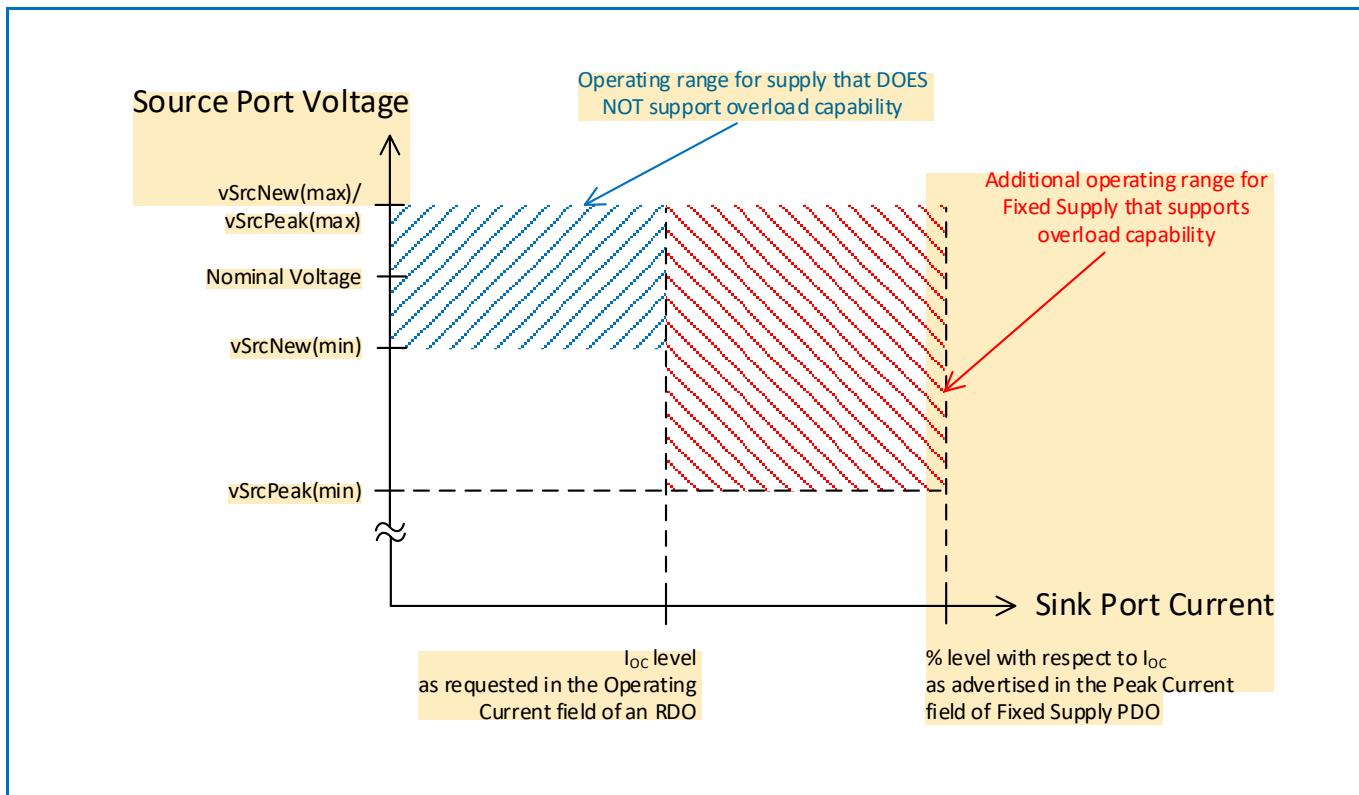
- The Source **Shall Not** drive V_{BUS} that is therefore expected to remain at *vSafe0V*.
- Any discharge circuitry that was used to achieve *vSafe0V* **Shall** be removed from V_{BUS}.
- The Dual-Role Power Port **Shall** be configured as a Sink.
- The USB connection **Shall Not** reset even though *vSafe5V* is no longer present on V_{BUS} (see [Section 9.1.2 "Mapping to USB Device States"](#)).

The *PS_RDY* Message associated with the Source being in Swap Standby **Shall** be sent after the V_{BUS} drive is removed. The time for the Source to transition to Swap Standby **Shall Not** exceed *tSrcSwapStdby*. Upon entering Swap Standby, the Source has relinquished its role as Source and is ready to become the new Sink. The transition time from Swap Standby to being the new Sink **Shall** be no more than *tNewSnk*. The new Sink **May** start using power after the new Source sends the *PS_RDY* Message.

7.1.11 Source Peak Current Operation

A Source that has the Fixed Supply PDO or AVS APDO Peak Current bits set to 01b, 10b and 11b **Shall** be designed to support one of the overload capabilities defined in [Table 6.10 “Fixed Power Source Peak Current Capability”](#) or [Table 6.15 “EPR AVS Power Source Peak Current Capability”](#) respectively. The overload conditions are bound in magnitude, duration and duty cycle as listed in [Table 6.10 “Fixed Power Source Peak Current Capability”](#) or [Table 6.15 “EPR AVS Power Source Peak Current Capability”](#). Sources are not required to support continuous overload operation. When overload conditions occur, the Source is allowed the range of $v_{SrcPeak}$ (instead of v_{SrcNew}) relative to the nominal value (see [Figure 7-15 “Source Peak Current Overload”](#)). When the overload capability is exceeded, the Source is expected take whatever action is necessary to prevent electrical or thermal damage to the Source. The Source **May** send a new **Source_Capabilities** Message with the Fixed Supply PDO or AVS APDO Peak Current bits set to 00b to prohibit overload operation even if an overload capability was previously negotiated with the Sink.

Figure 7-15 “Source Peak Current Overload”



7.1.12 Source Capabilities Extended Parameters

Implementers can choose to make available certain characteristics of a USB PD Source as a set of static and/or dynamic parameters to improve interoperability between external power sources and portable computing devices. The complete list of reportable static parameters is described in full in [Section 6.5.1 “Source_Capabilities_Extended_Message”](#) and listed in [Figure 6-36 “Source_Capabilities_Extended_Message”](#). The subset of parameters listed below directly represent Source capabilities and are described in the rest of this section.

- Voltage Regulation.
- Holdup Time.
- Compliance.
- Peak Current.
- Source Inputs.
- Batteries.

7.1.12.1 Voltage Regulation Field

The power consumption of a device can change dynamically. The ability of the Source to regulate its Voltage output might be important if the device is sensitive to fluctuations in Voltage. The Voltage Regulation bit field is used to convey information about the Sources output regulation and tolerance to various load steps.

7.1.12.1.1 Load Step Slew Rate

The default load step slew rate is established at 150mA/ μ s. A Source **Shall** meet the following requirements under the load step reported in the Extended Source Capabilities:

- The Source **Shall** maintain V_{BUS} regulation within the **vSrcValid** range.
- The noise on the CC line **Shall** remain below **vNoiseIdle** and **vNoiseActive**.

Test conditions require a change in both positive and negative load steps from 1Hz to 5000Hz, up to the Advertised Load Step Magnitude of the full load output including from both 10 mA and 10% initial load. The Source **Shall** ensure that PD Communications meet the transmit and receive masks as specified in [Section 5.8.2 “Transmit and Receive Masks”](#) under all load conditions.

7.1.12.1.2 Load Step Magnitude

The default load step magnitude rate **Shall** be 25% of IoC. The Source **May** report higher capability tolerating a load step of 90% of IoC.

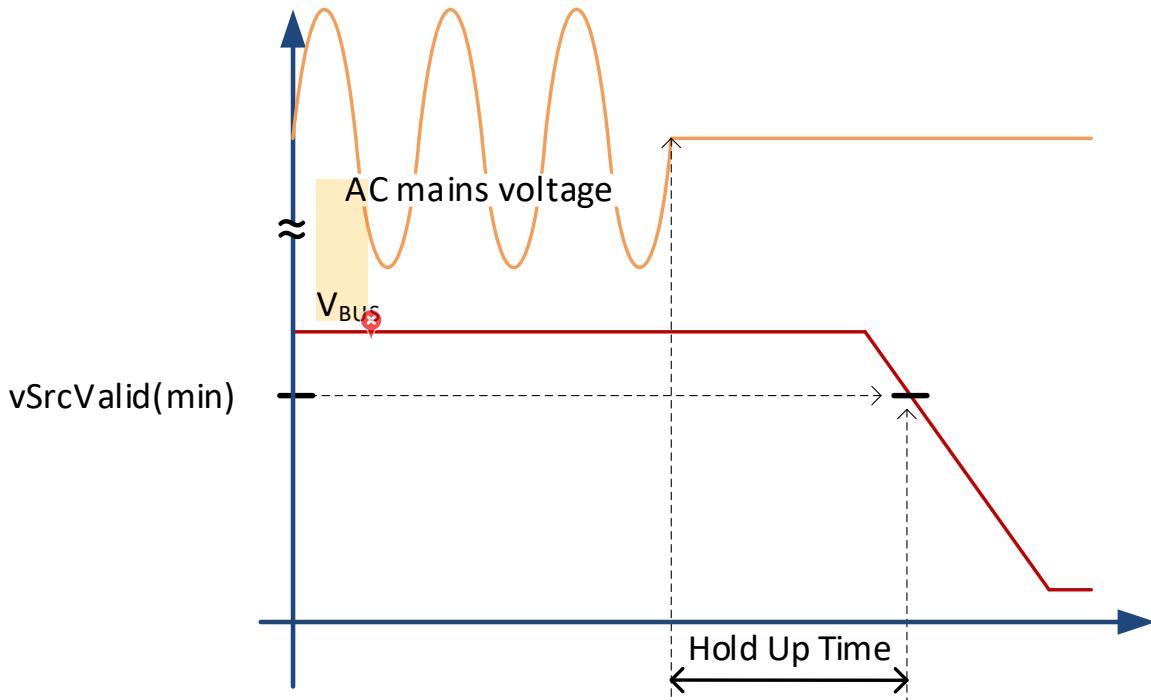
7.1.12.2 Holdup Time Field

The Holdup Time field **Shall** return a numeric value of the number of milliseconds the output Voltage stays in regulation upon a short interruption of AC mains.

A mains supplied Source **Shall** report its holdup time in this field. The holdup time is measured with the load at rated maximum, with AC mains at 115VAC rms and 60Hz (or at 230VAC rms and 50Hz for a Source that does not support 115VAC mains). The reported time describes the minimum length of time from the last completed AC mains input cycle (zero-degree phase angle) until when the output Voltage decays below **vSrcValid** (min). Power sources are recommended to support a minimum of 3ms and are preferred to support over 10 milliseconds holdup time (equivalent to a half cycle drop from the AC Mains). See [Figure 7-16 “Holdup Time Measurement”](#).



Figure 7-16 “Holdup Time Measurement”



7.1.12.3 Compliance Field

An SPR Source claiming LPS, PS1 or PS2 compliance (see [\[IEC 62368-1\]](#)) **Shall** report its capabilities in the Compliance field. Since the SPR Source **May** have several potential output Voltage and current settings, every SPR Source supply (indicated by a PDO) **Shall** be compliant to LPS requirements.

Note: according to the requirements of [\[IEC 60950-1\]](#) and/or [\[IEC 62368-3\]](#), a device tested and certified with an LPS Source (SPR Source or EPR Source operating in SPR Mode) is prohibited from using a non-LPS Source (EPR Source operating in EPR Mode). Alternatively, [\[IEC 62368-1\]](#), classifies power sources according to their maximum, constrained power output (15watts or 100watts).

7.1.12.4 Peak Current

The Source reports its ability to source peak current delivery in excess of the negotiated amount in the Peak Current field. The duration of peak current **Shall** be followed by a current consumption below the Operating Current (IoC) in order to maintain average power delivery below the IoC current.

A Source **May** have greater capability to source peak current than can be reported using the Peak Current field in the Fixed Supply PDO or AVS APDO. In this case the Source **Shall** report its additional capability in the Peak Current field in the [Source_Capabilities_Extended](#) Message.

Each overload period ***Shall*** be followed by a period of reduced current draw such that the rolling average current over the Overload Period field value with the specified Duty Cycle field value (see [Section 6.5.1.10 “Peak Current Field”](#)) ***Shall Not*** exceed the negotiated current. This is calculated as:

Period of reduced current = $(1 - \text{value in Duty Cycle field}/100) * \text{value in Overload Period field}$

7.1.12.5 Source Inputs

The Source Inputs field identifies the possible inputs that provide power to the Source. Note some Sources are only powered by a Battery (e.g., an automobile) rather than the more common mains.

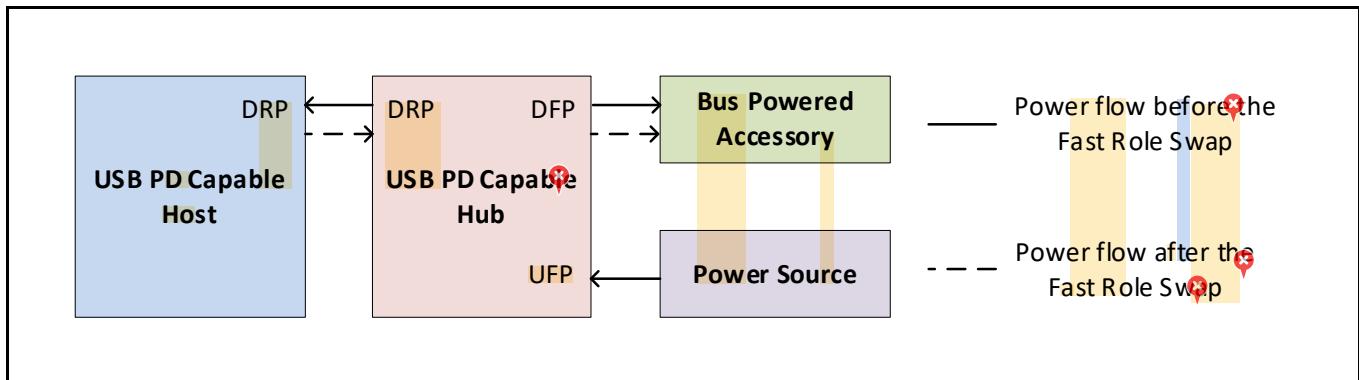
7.1.12.6 Batteries

The Batteries field ***Shall*** report the number of Batteries the Source supports. The Source ***Shall*** independently report the number of Hot Swappable Batteries and the number of Fixed batteries.

7.1.13 Fast Role Swap

A Fast Role Swap limits the interruption of V_{BUS} power to a bus powered accessory connected to a Hub DFP that has a UFP attached to a power source and a DRP attached to a Host port supporting DRP as shown in [Figure 7-17 “VBUS Power during Fast Role Swap”](#).

[Figure 7-17 “VBUS Power during Fast Role Swap”](#)



When the power source connected to the Hub UFP stops sourcing power and V_{BUS} at the Hub DRP connector discharges below $v_{SrcValid}(\min)$, if V_{BUS} has been negotiated to a higher Voltage than $vSafe5V$, or $vSafe5V(\min)$ the Fast Role Swap signal **Shall** be sent from the Hub DRP to the Host DRP and the Hub DRP **Shall Sink** power. In the Fast Role Swap use case, the Hub DRP behaves like a bidirectional power path. The Hub DRP **Shall Not** enable V_{BUS} discharge circuitry when changing operation from initial Source to new Sink. The Hub DFP Port(s) **Shall** support default USB Type-C® Current (see [\[USB Type-C 2.3\]](#)) until a new Explicit Contract is negotiated.

After sending the FRS signal and while $V_{BUS} > vSafe5V(\min)$, the new Sink **Shall Not** draw more than $i_{NewFrsSink}$ until the new Source has applied its R_p . The new Sink **Shall Not** draw more than $i_{SnkStdby}$ from V_{BUS} until $t_{SnkFRSwap}$ after it has started sending the FRS signal or V_{BUS} has fallen below $vSafe5V(\min)$. The $t_{SnkFRSwap}$ time **Shall** start at the beginning of the FRS signal or when V_{BUS} falls below $vSafe5V(\min)$, whichever comes later. After waiting for $t_{SnkFRSwap}$, the new Sink **Shall Not** draw more than $i_{NewFrsSink}$ until the new Source has applied its R_p . After the new Source has applied its R_p , the new Sink **Shall** be limited to USB Type-C® Current (see [\[USB Type-C 2.3\]](#)) in an Implicit Contract until a new Explicit Contract is negotiated. All Sink requirements **Shall** apply to the new Sink after the Fast Role Swap is complete. The Fast Role Swap response of the Host DRP is described in [Section 7.2.10 “Fast Role Swap”](#) since the Host DRP is operating as the initial Sink prior to the Fast Role Swap.

After the V_{BUS} Voltage level at the Hub DRP connector drops below $vSafe5V$ a **PS_RDY** Message **Shall** be sent to the Host DRP as shown in the Fast Role Swap transition diagram of [Section 7.3.5 “Transitions Caused by Fast Role Swap”](#).

[Figure 7-18 “VBUS detection and timing during Fast Role Swap, initial VBUS \(at new source\) > vSafe5V\(min\)”](#) and [Figure 7-19 “VBUS detection and timing during Fast Role Swap, initial VBUS \(at new source\) < vSafe5V\(min\)”](#) show the V_{BUS} detection and timing for the new Source during a Fast Role Swap after the Fast Role Swap signal has been received. The new Source **May** turn on the V_{BUS} output switch once V_{BUS} is below $vSafe5V(\max)$. In this case, the new Source prevents V_{BUS} from falling below $vSafe5V(\min)$. The new source **Shall** turn on the V_{BUS} output switch within $t_{SrcFRSwap}$ of falling below $vSafe5V(\min)$.

V_{BUS} might have started at $vSafe5V$ or at higher Voltage. When the Fast Role Swap Signal is detected, V_{BUS} could therefore be either above $vSafe5V(\max)$, within the $vSafe5V$ range, or below $vSafe5V(\min)$. If the Fast Role Swap Signal is detected when V_{BUS} is below $vSafe5V(\min)$, then the new source **Shall** turn on the V_{BUS} output switch within

$tSrcFRSwap$ of detecting the Fast Role Swap Signal. In this case, the maximum time from the beginning of the Fast Role Swap signal to V_{BUS} being sourced *May* be $tSrcFRSwap$ (max) + $tFRSwapRx$ (max).

Figure 7-18 “V_{BUS} detection and timing during Fast Role Swap, initial V_{BUS} (at new source) > vSafe5V(min)”

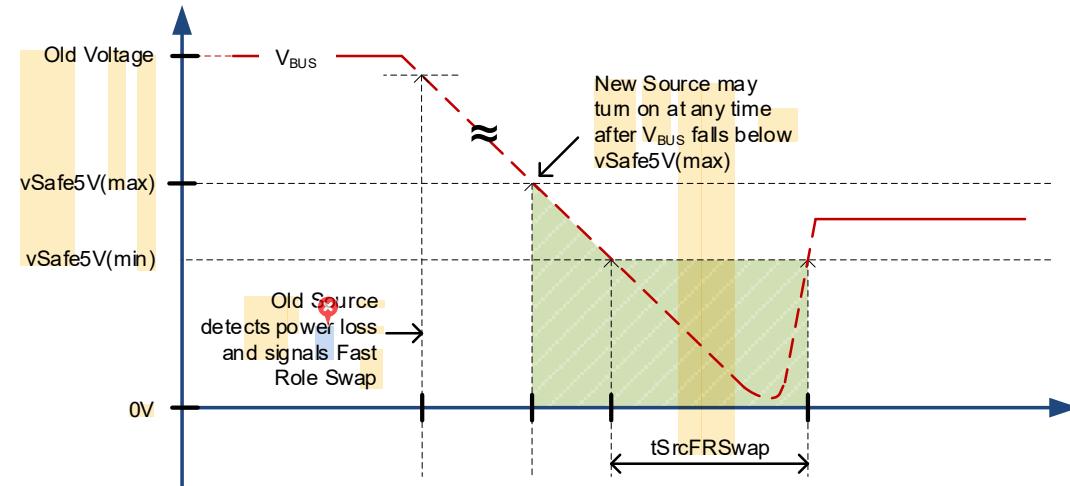
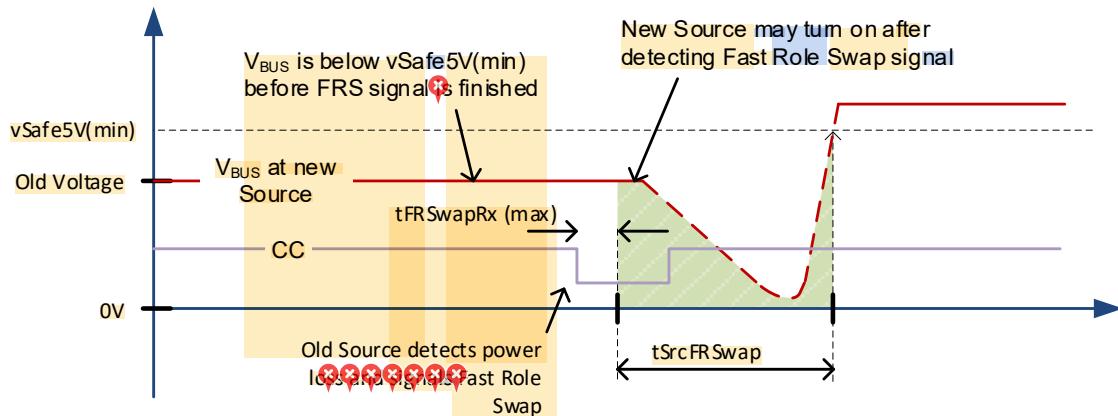


Figure 7-19 “V_{BUS} detection and timing during Fast Role Swap, initial V_{BUS} (at new source) < vSafe5V(min)”

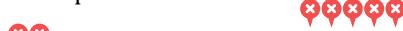


7.1.14 Non-application of V_{BUS} Slew Rate Limits

Scenarios where **vSrcSlewPos** and **vPpsSlewPos** V_{BUS} slew rate limits do not apply and V_{BUS} **May** transition faster than specified are as follows:

- When first applying V_{BUS} after an Attach.
- When applying V_{BUS} as part of a Power Role Swap to Source Role.
- When increasing V_{BUS} from **vSafe0V** to **vSafe5V** during a Hard Reset.
- During a Fast Role Swap when the initial Sink applies V_{BUS}.

Scenarios where **vSrcSlewNeg** and **vPpsSlewNeg** V_{BUS} slew rate limits do not apply and V_{BUS} **May** transition faster than specified are as follows:



- When discharging V_{BUS} to **vSafe0V** during a Hard Reset.
- When discharging V_{BUS} to **vSafe0V** as part of a Power Role Swap to Sink Role.
- When discharging V_{BUS} to **vSafe0V** after a Detach.
- During a Fast Role Swap when the V_{BUS} power source connected to the Hub UFP stops sourcing power.

7.1.15 VCONN Power Cycle

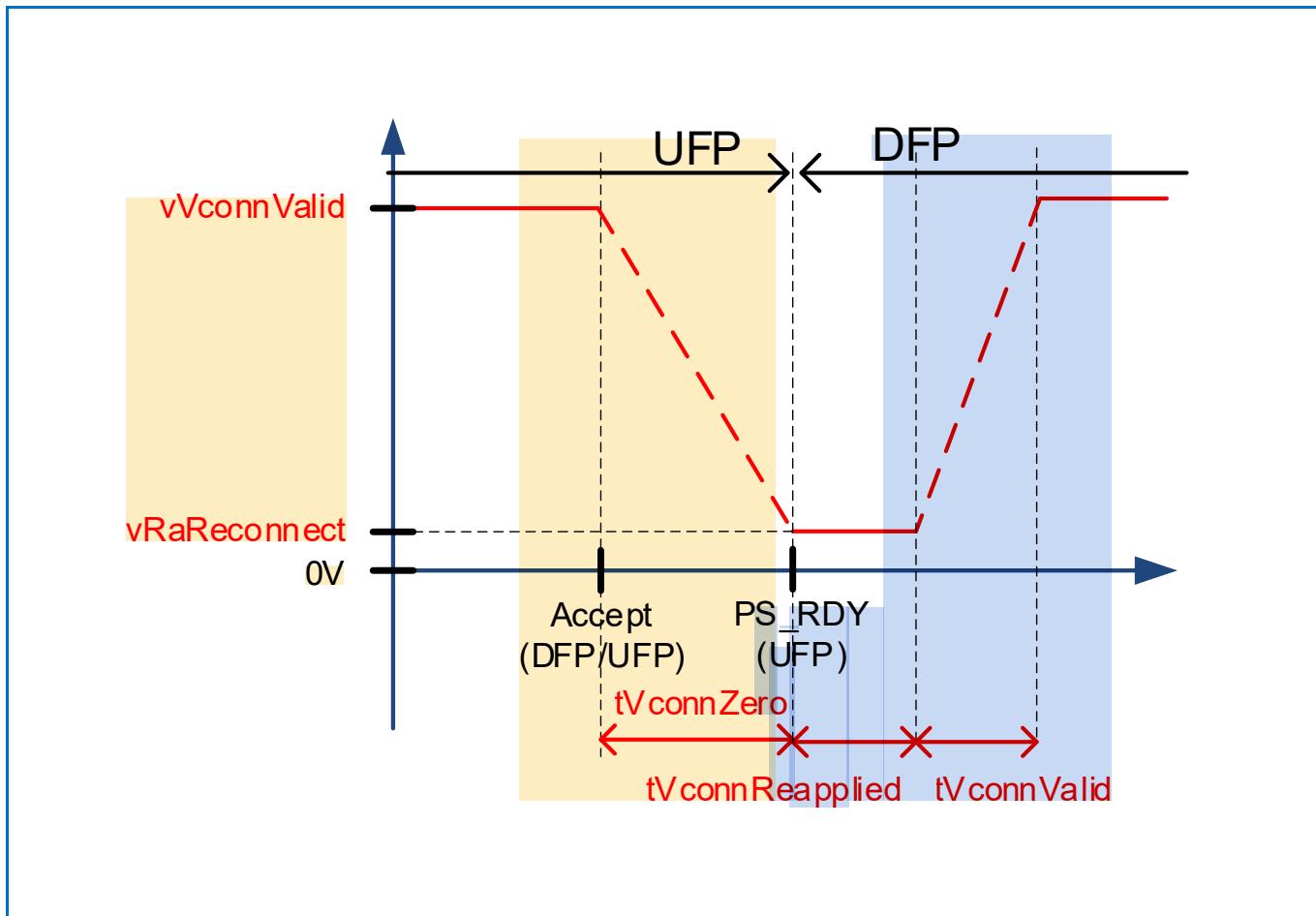
7.1.15.1 UFP VCONN Power Cycle

The Data Reset process requires the DFP to be the VCONN source by the end of the process. In the case where the UFP is the VCONN source, the following steps **Shall** be followed:

- Following the last bit of the **GoodCRC** acknowledging the **Accept** Message in response to the **Data_Reset** Message, the UFP **Shall** turn off VCONN and ensure it is below vRaReconnect (see [USB Type-C 2.3]) within **tVconnZero**.
- When VCONN is below vRaReconnect, the UFP **Shall** send a **PS_RDY** Message. Note if the UFP was not sourcing VCONN, it still sends the **PS_RDY** Message.
- The DFP **Shall** wait **tVconnReapplied** following the last bit of the **GoodCRC** acknowledging the **PS_RDY** Message before sourcing VCONN. The DFP **Shall** ensure VCONN is within vVconnValid (see [USB Type-C 2.3]) within **tVconnValid**.

Figure 7-20 "Data Reset UFP Vconn Power Cycle" below illustrates the UFP VCONN Power Cycle process.

Figure 7-20 "Data Reset UFP Vconn Power Cycle"



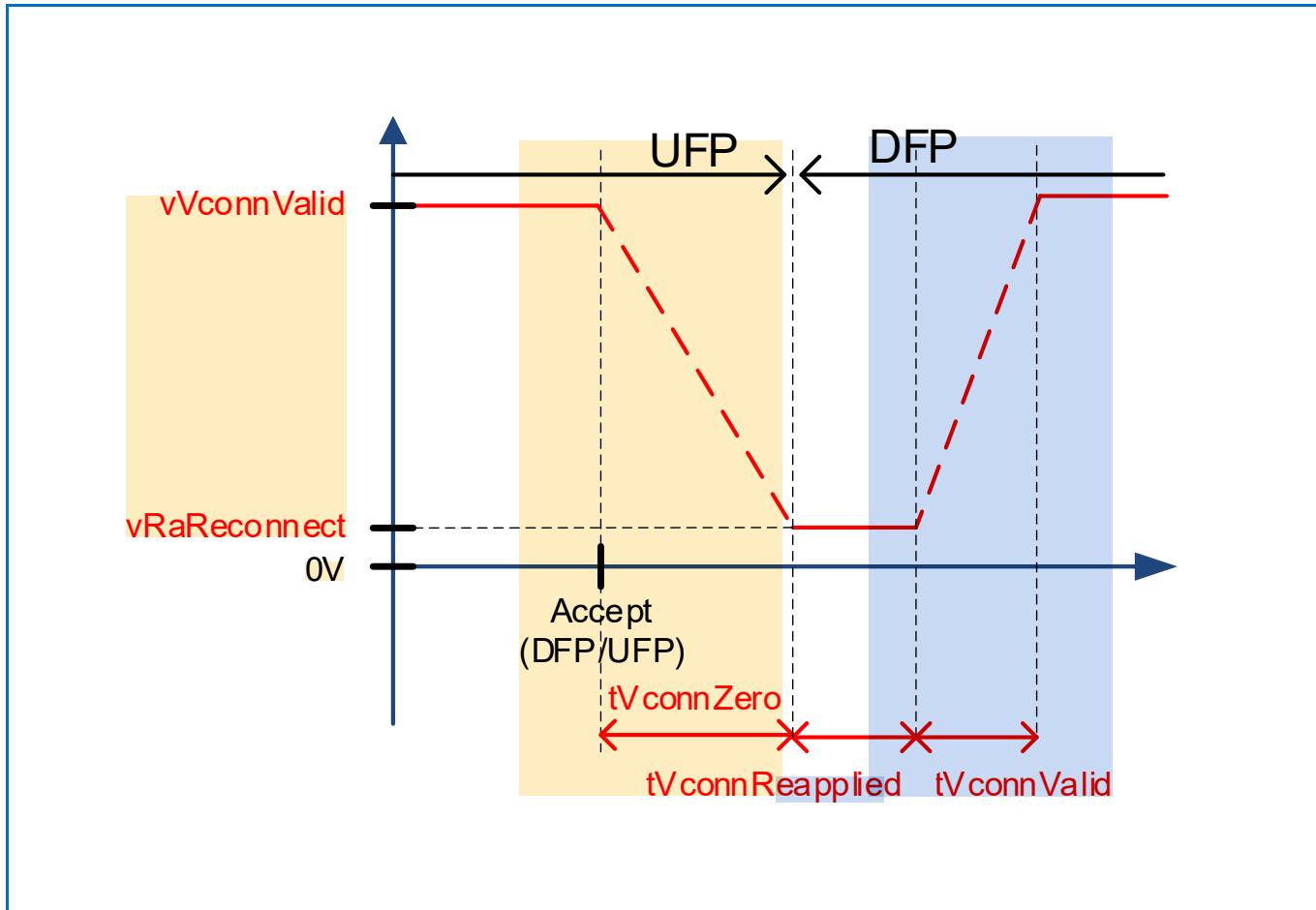
7.1.15.2 DFP VCONN Power Cycle

The Data Reset process requires the DFP to be the VCONN source by the end of the process. In the case where the DFP is the VCONN source, the following steps *Shall* be followed:

- 1) If the DFP sent the **Data_Reset** Message and is sourcing VCONN then it *Shall* turn off VCONN and ensure it is below vRaReconnect (see [USB Type-C 2.3]) within **tVconnZero** of the last bit of the **GoodCRC** acknowledging the **Accept** message in response to the **Data_Reset** Message.
- 2) If the UFP sent the **Data_Reset** Message then the DFP *Shall* turn off VCONN and ensure it is below vRaReconnect (see [USB Type-C 2.3]) within **tVconnZero** following the last bit of the **GoodCRC** acknowledging the **Accept** Message in response to the **Data_Reset** Message.
- 3) When VCONN is below vRaReconnect, the DFP *Shall* wait **tVconnReapplied** before sourcing VCONN.
- 4) The DFP *Shall* ensure VCONN is within vVconnValid (see [USB Type-C 2.3]) within **tVconnValid**.

Figure 7-21 “Data Reset DFP Vconn Power Cycle” below illustrates the DFP VCONN Power Cycle process.

Figure 7-21 “Data Reset DFP Vconn Power Cycle”



7.2 Sink Requirements

7.2.1 Behavioral Aspects

A USB PD Sink exhibits the following behaviors.

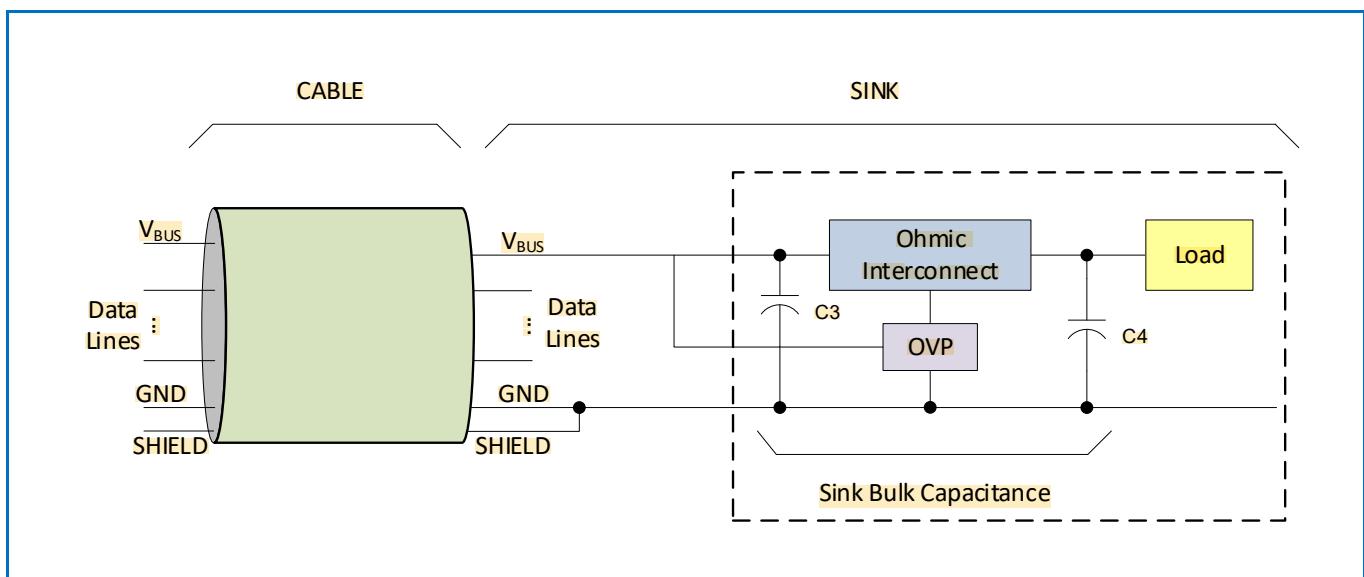
- **Shall** not draw more than [USB Type-C 2.3] USB Type-C® Current from V_{BUS} while in a Default Contract or Implicit Contract.
- Shall follow the requirements as specified in [Section 7.1.5 “Response to Hard Resets”](#) when **Hard Reset** Signaling is received.
- **Shall** control V_{BUS} in-rush current when increasing current consumption.

7.2.2 Sink Bulk Capacitance

The Sink bulk capacitance consists of C3 and C4 as shown in [Figure 7-22 “Placement of Sink Bulk Capacitance”](#). The Ohmic Interconnect might consist of PCB traces for power distribution or power switching devices. The Ohmic Interconnect is expected to be part of an input over Voltage protection (Sink OVP) circuit implemented by the Sink as described in [Section 7.2.9.2 “Input Over Voltage Protection”](#) to protect against excessive V_{BUS} input Voltage. A Sink **Shall** implement OVP. The Sink **Shall Not** rely on the Source output Voltage limit for its input over Voltage protection. The capacitance might be a single capacitor, a capacitor bank or distributed capacitance. An upper bound of **cSnkBulkPd** **Shall Not** be exceeded so that the transient charging, or discharging, of the total bulk capacitance on V_{BUS} can be accounted for during Voltage transitions.

The Sink bulk capacitance that is within the **cSnkBulk** max or **cSnkBulkPd** max limits is allowed to change to support a newly negotiated power level. The capacitance can be changed when the Sink enters Sink Standby or during a Voltage transition or when the Sink begins to operate at the new power level. Changing the Sink bulk capacitance **Shall Not** cause a transient current on V_{BUS} that violates the present Contract. During a Power Role Swap the Default Sink **Shall** transition to Swap Standby before operating as the new Source. Any change in bulk capacitance required to complete the Power Role Swap **Shall** occur during Swap Standby.

[Figure 7-22 “Placement of Sink Bulk Capacitance”](#)



7.2.3 Sink Standby

The Sink **Shall** transition to Sink Standby before a positive or negative Voltage transition of V_{BUS}. During Sink Standby the Sink **Shall** reduce the current drawn to **iSnkStdby**. This allows the Source to manage the Voltage transition as well as supply sufficient operating current to the Sink to maintain PD operation during the transition. The Sink **Shall** complete this transition to Sink Standby within **tSnkStdby** after evaluating the **Accept** Message from the Source. The transition when returning to Sink operation from Sink Standby **Shall** be completed within **tSnkNewPower**. The **iSnkStdby** requirement **Shall** only apply if the Sink current draw is higher than this level.

See [Section 7.3 "Transitions"](#) for details of when **iSnkStdby** **Shall** be applied for any given transition.

7.2.3.1 Programmable Power Supply Sink Standby

A Sink is not required to transition to Sink Standby when operating within the negotiated PPS APDO. A Sink **May** consume the Operating Current value in the PPS RDO during PPS output Voltage changes. However, prior to operating the SPR PPS in Current Limit, the Sink **Shall** program the PPS Operating Voltage to the lowest practical level that satisfies the Sink load requirement. Doing so will minimize the inrush current that occurs when the transition to Current Limit occurs. When operating with an SPR PPS Source that is in Current Limit, the Sink **Shall Not** change its load in a manner that exceeds **iPpsCLLoadStepRate** or **iPpsCLLoadReleaseRate**. The load change magnitude **Shall Not** request a change to the Current Limit setpoint that exceeds **iPpsCLLoadStep**.

If the Sink negotiates for a new PPS APDO, then the Sink **Shall** transition to Sink Standby while changing between PPS APDOs as described in [Section 7.3.1 "Transitions caused by a Request Message"](#).

7.2.4 Suspend Power Consumption

When Source has set its USB Suspend Supported flag (see [Section 6.4.1.2.2.2 "USB Suspend Supported"](#)), a Sink **Shall** go to the lowest power state during USB suspend. The lowest power state **Shall** be **pSnkSusp** or lower for a PDUSB Peripheral and **pHubSusp** or lower for a PDUSB Hub. There is no requirement for the Source Voltage to be changed during USB suspend.

7.2.5 Zero Negotiated Current

When a Sink Requests zero current as part of a power negotiation with a Source, the Sink **Shall** go to the lowest power state, **pSnkSusp** or lower, where it can still communicate using PD signaling.

7.2.6 Transient Load Behavior

When a Sink's operating current changes due to a load step, load release or any other change in load level, the positive or negative overshoot of the new load current **Shall Not** exceed the range defined by **iOvershoot**. For the purposes of measuring **iOvershoot** the new load current value is defined as the average steady state value of the load current after the load step has settled. The rate of change of any shift in Sink load current during normal operation **Shall Not** exceed **iLoadStepRate** (for load steps) and **iLoadReleaseRate** (for load releases) as measured at the Sink receptacle.

The Sink's operating current **Shall Not** change faster than the value reported in the Source's Load Step Slew Rate field and **Shall** ensure that PD Communications meet the transmit and receive masks as specified in [Section 5.8.2 "Transmit and Receive Masks"](#).

7.2.7 Swap Standby for Sinks

The Sink capability in a Dual-Role Power Port **Shall** support Swap Standby. Swap Standby occurs for the Sink after evaluating the **Accept** Message from the Source during a Power Role Swap negotiation. While in Swap Standby the Sink's current draw **Shall Not** exceed **iSnkSwapStdby** from V_{BUS} and the Dual-Role Power Port **Shall** be configured as a Source after V_{BUS} has been discharged to **vSafe0V** by the existing Initial Source. The Sink's USB connection **Should Not** be reset even though **vSafe5V** is not present on the V_{BUS} conductor (see [Section 9.1.2 "Mapping to USB Device States"](#)). The time for the Sink to transition to Swap Standby **Shall** be no more than **tSnkSwapStdby**. When in Swap Standby the Sink has relinquished its role as Sink and will prepare to become the new Source. The transition time from Swap Standby to new Source **Shall** be no more than **tNewSrc**.

7.2.8 Sink Peak Current Operation

Sinks **Shall** only make use of a Source overload capability when the corresponding Fixed Supply PDO Peak Current (see [Section 6.4.1.2.2.8 "Peak Current"](#)) or Adjustable Voltage Supply APDO Peak Current (see [Section 6.4.1.2.5.2.2 "Peak Current"](#)) bits are set to 01b, 10b and 11b. Sinks **Shall** manage thermal aspects of the overload event by not exceeding the average negotiated output of a Fixed Supply or **VS** that supports Peak Current operation.

Sinks that depend on the Peak Current capability for enhanced system performance **Shall** also function correctly when Attached to a Source that does not offer the Peak Current capability or when the Peak Current capability has been inhibited by the Source.

7.2.9 Robust Sink Operation

7.2.9.1 Sink Bulk Capacitance Discharge at Detach

When a Source is Detached from a Sink, the Sink **Shall** continue to draw power from its input bulk capacitance until V_{BUS} is discharged to $vSafe5V$ or lower by no longer than $tSafe5V$ from the Detach event. This safe Sink requirement **Shall** apply to all Sinks operating with a negotiated V_{BUS} level greater than $vSafe5V$ and **Shall** apply during all low power and high-power operating modes of the Sink.

If the Detach is detected during a Sink low power state, such as USB Suspend, the Sink can then draw as much power as needed from its bulk capacitance since a Source is no longer Attached. In order to achieve a successful Detach detect based on V_{BUS} Voltage level droop, the Sink power consumption **Shall** be high enough so that V_{BUS} will decay below $vSrcValid(min)$ well within $tSafe5V$ after the Source bulk capacitance is removed due to the Detach. Once adequate V_{BUS} droop has been achieved, a discharge circuit can be enabled to meet the safe Sink requirement.

To illustrate the point, the following set of Sink conditions will not meet the safe Sink requirement without additional discharge circuitry:

- Negotiated $V_{BUS} = 20V$.
- Maximum allowable supplied V_{BUS} Voltage = 21.55V.
- Maximum bulk capacitance = 30 μF .
- Power consumption at Detach = 12.5mW.

When the Detach occurs (hence removal of the Source bulk capacitance) the 12.5mW power consumption will draw down the V_{BUS} Voltage from the worst-case maximum level of 21.55V to 17V in approximately 205ms. At this point, with V_{BUS} well below $vSrcValid$ (min) an approximate 100mW discharge circuit can be enabled to increase the rate of Sink bulk capacitance discharge and meet the safe Sink requirement. The power level of the discharge circuit is dependent on how much time is left to discharge the remaining Voltage on the Sink bulk capacitance. If a Sink has the ability to detect the Detach in a different manner and in much less time than $tSafe5V$, then this different manner of detection can be used to enable a discharge circuit, allowing even lower power dissipation during low power modes such as USB Suspend.

In most applications, the safe Sink requirement will limit the maximum Sink bulk capacitance well below the $cSnkBulkPd$ limit. A Detach occurring during Sink high power operating modes must quickly discharge the Sink bulk capacitance to $vSafe5V$ or lower as long as the Sink continues to draw adequate power until V_{BUS} has decayed to $vSafe5V$ or lower.

7.2.9.2 Input Over Voltage Protection

Sinks **Shall** implement input over Voltage protection (OVP)^A to prevent damage from input Voltage that exceeds the Voltage handling capability of the Sink. The definition of Voltage handling capability is left to the discretion of the Sink implementation. The over Voltage response of Sinks **Shall Not** interfere with normal PD operation and **Shall** account for $vSrcNew$, $vSrcValid$ or $vPpsNew$, $vPpsValid$ as determined by the negotiated V_{BUS} value. SPR Sinks **Should** tolerate input Voltages as high as $vSprMax$ and **Shall** meet applicable safety requirements if $vSprMax$ is exceeded. Likewise, EPR Sinks **Should** tolerate input Voltages as high as $vEprMax$ and **Shall** meet applicable safety requirements if $vEprMax$ is exceeded.

Sinks **Should** attempt to send a **Hard Reset** message when over Voltage protection engages followed by an **Alert** Message indicating an OVP event once an Explicit Contract has been established. The over Voltage protection response **May** engage at either the port or system level. Systems or ports that have engaged over Voltage protection **Shall** resume **USB Default Operation** when the Source has re-established $vSafe5V$ on V_{BUS} .

The Sink **Shall** be able to renegotiate with the Source after resuming USB Default Operation. The decision of how to respond to renegotiation after an over Voltage event is left to the discretion of the Sink implementation.

The Sink **Shall** prevent continual system or port cycling if over Voltage protection continues to engage after initially resuming either USB Default Operation or renegotiation. Latching off the port or system is an acceptable response to recurring over Voltage.

7.2.9.3 Over Temperature Protection

Sinks **Shall** implement over temperature protection (OTP) to prevent damage from temperature that exceeds the thermal capability of the Sink. The definition of thermal capability and the monitoring locations used to trigger the over temperature protection are left to the discretion of the Sink implementation.

Sinks **Shall** attempt to send a **Hard Reset** message when over temperature protection engages followed by an **Alert** Message indicating an OTP event once an Explicit Contract has been established. The over temperature protection response **May** engage at either the port or system level. Systems or ports that have engaged over temperature protection **Should** attempt to resume USB Default Operation after sufficient cooling is achieved and **May** latch off to protect the port or system. The definition of sufficient cooling is left to the discretion of the Sink implementation.

The Sink **Shall** be able to renegotiate with the Source after resuming USB Default Operation. The decision of how to respond to renegotiation after an over temperature event is left to the discretion of the Sink implementation.

The Sink **Shall** prevent continual system or port cycling if over temperature protection continues to engage after initially resuming either USB Default Operation or renegotiation. Latching off the port or system is an acceptable response to recurring over temperature.

7.2.9.4 Over Current Protection

Sinks that operate with a Programmable Power Supply **Shall** implement their own internal current protection mechanism to protect against internal V_{BUS} current faults as well as erratic Source current regulation. The Sink **Shall** never draw higher current than the Maximum Current value in the PPS APDO.

7.2.10 Fast Role Swap

As described in [Section 7.1.13 “Fast Role Swap”](#) a Fast Role Swap limits the interruption of V_{BUS} power to a bus powered accessory connected to a Hub DFP that has a UFP attached to a power source and a DRP attached to a Host port that supports DRP. This configuration is shown in [Figure 7-17 “V_{BUS} Power during Fast Role Swap”](#).

The Host DRP, upon establishing an explicit contract, **Shall** query the initial Source’s Sink Capabilities to determine whether the initial Source supports Fast Role Swap, and what level of current it requires. If the **Sink Capabilities** Message received from the initial Source has at least one of the Fast Role Swap bits set, and the Host DRP is able to source the requested current at 5V, the Host DRP **May** arm itself for Fast Role Swap. If the Host DRP has not queried the Sink Capabilities from the initial Source, or if the **Sink Capabilities** Message reports no Fast Role Swap support or a current that is beyond what the Host DRP is able or willing to source in the event of a Fast Role Swap, the Host DRP **Shall Not** arm itself for Fast Role Swap and **Shall Ignore** any Fast Role Swap signals that are detected.

When the Host DRP that supports Fast Role Swap detects the Fast Role Swap signal, the Host DRP **Shall** stop sinking current and **Shall** be ready and able to source **vSafe5V** if the residual V_{BUS} Voltage level at the Host DRP connector is greater than **vSafe5V**. When the residual V_{BUS} Voltage level at the Host DRP connector discharges below **vSafe5V(min)** the Host DRP as the new Source **Shall** supply **vSafe5V** to the Hub DRP within **tSrcFRSwap**. The Host DRP **Shall Not** enable V_{BUS} discharge circuitry when changing roles from initial Sink to new Source.

The new Source **Shall** supply **vSafe5V** at USB Type-C® Current (see [\[USB Type-C 2.3\]](#)) at the value Advertised in the Fast Role Swap USB Type-C® Current field (see [Section 6.4.1.3.1.6 “Fast Role Swap USB Type-C® Current”](#)). All Source requirements **Shall** apply to the new Source after the Fast Role Swap is complete. The Fast Role Swap response of the Hub DRP is described in [Section 7.1.13 “Fast Role Swap”](#) since the Hub DRP is operating as the initial Source prior to the Fast Role Swap.

After the Host DRP is providing V_{BUS} power to the Hub DRP, a **PS_RDY** Message **Shall** be sent to the Hub DRP as defined by the Fast Role Swap signaling and messaging sequence detailed in [Section 7.3.5 “Transitions Caused by Fast Role Swap”](#).

7.3 Transitions

The following sections illustrate the power supply's response to various types of negotiations. The negotiations are triggered by certain Messages or Signaling. It provides examples of the transitions and is organized around each of the Messages and Signals that result in a response from the power supply. The response to a Message or Signal can result in different transitions depending upon the power supply's starting conditions and the requested change.

- Transitions caused by a Request Message:
 - Generic transition between (A)PDOs:
 - Increase the current.
 - Increase the Voltage.
 - Increase the Voltage and the current.
 - Increase the Voltage and decrease the current.
 - Decrease the Voltage and increase the current.
 - Decrease the Voltage and the current.
 - No change in Current or Voltage.
 - Transitions within the same PDO (Fixed, Battery, Variable):
 - Increase the current.
 - Decrease the current.
 - No change in current.
 - Transitions within the same PPS APDO:
 - Increasing the Programmable Power Supply (PPS) Voltage.
 - Decreasing the Programmable Power Supply (PPS) Voltage.
 - Increasing the Programmable Power Supply (PPS) Current.
 - Decreasing the Programmable Power Supply (PPS) Current.
 - Same Request Programmable Power Supply (PPS).
 - Transitions within the same AVS APDO:
 - Increasing the Adjustable Voltage Supply (AVS) Voltage
 - Decreasing the Adjustable Voltage Supply (AVS) Voltage
 - Same Request Adjustable Voltage Supply (AVS) 
- Transitions caused by the **PR_Swap** Message:
 - Source requests a Power Role Swap
 - Sink requests a Power Role Swap
- Transitions caused by the **GotoMin** Message:
 - Sink decreases its current draw to pre-negotiated minimum.

- Transitions caused by **Hard Reset** Signaling:
 - Source issues **Hard Reset** Signaling.
 - Sink issues **Hard Reset** Signaling.
- Transitions caused by Fast Role Swap Signaling:
 - Source asserts R_d at its preferred **[USB Type-C 2.3]** current.

7.3.1 Transitions caused by a Request Message

This section describes transitions that are caused by a Request Message.

7.3.1.1 Changing the Source between Different (A)PDOs

In these transition descriptions the term (A)PDO is used to describe any Power Data Object, regardless of whether it is a PDO or an APDO in the Capabilities Message.

This section describes transitions in response to a Request message:

- From one (A)PDO to another (A)PDO
- From an Implicit contract to an Explicit Contract
- From [\[USB Type-C 2.3\]](#)operation to the [First Explicit Contract](#)

These transitions usually result in a Voltage change but is not required.

The interaction of the Device Policy Manager, the port Policy Engine and the Power Supply in the cases described above, is shown in [Figure 7-23 “Generic Change for the Source to another \(A\)PDO”](#).

The Source Voltage as the transition starts **Shall** be any Voltage within the **Valid V_{BUS}** range of the previous Source PDO or APDO. The Source Voltage after the transition is complete **Shall** be any Voltage within the **Valid V_{BUS}** range of the new Source PDO or APDO. The sequence that **Shall** be followed is described in [Table 7.1 “Sequence Description for Changing the Source to another \(A\)PDO”](#)... The timing parameters that **Shall** be followed are listed in [Table 7.25 “Source Electrical Parameters”](#), [Table 7.26 “Sink Electrical Parameters”](#), and [Table 7.27 “Common Source/Sink Electrical Parameters”](#). Note in this figure, the Sink has previously sent a **Request** Message to the Source.

The voltage is considered to increase if the change from V_{OLD} to V_{NEW} is greater than **vSmallStep**. The determination **Shall** be based on the nominal (A)PDO voltage before and after, unless either (A)PDO is Battery or Variable when the worst case of the following is assumed in making this determination.

- Minimum Voltage to Voltage.
- Minimum Voltage to Maximum Voltage.
- Voltage to Maximum Voltage.

The following sections begin with a description of the generic process followed by more specific examples of the most common transitions.

7.3.1.1.1

Generic Transition Diagram for changing the Source to another (A)PDO

The process for changing from one (A)PDO to another (A)PDO is described in general terms in this section. Note it also applies to the transition from [\[USB 2.0\]](#), [\[USB 3.2\]](#), [\[USB4\]](#), [\[USB Type-C 2.3\]](#) or [\[USBBC 1.2\]](#) operation into Power Delivery Mode during the initial Contract negotiation.

The interaction of the Device Policy Manager, the port Policy Engine and the Power Supply that **Shall** be followed when increasing the current is shown in [Figure 7-23 “Generic Change for the Source to another \(A\)PDO”](#).

The sequence that **Shall** be followed is described in [Table 7.1 “Sequence Description for Changing the Source to another \(A\)PDO”](#). The timing parameters that **Shall** be followed are listed in [Table 7.25 “Source Electrical Parameters”, Table 7.26 “Sink Electrical Parameters”, and Table 7.27 “Common Source/Sink Electrical Parameters”](#). Note in this figure, the Sink has previously sent a **Request** Message to the Source.

[Figure 7-23 “Generic Change for the Source to another \(A\)PDO”](#)

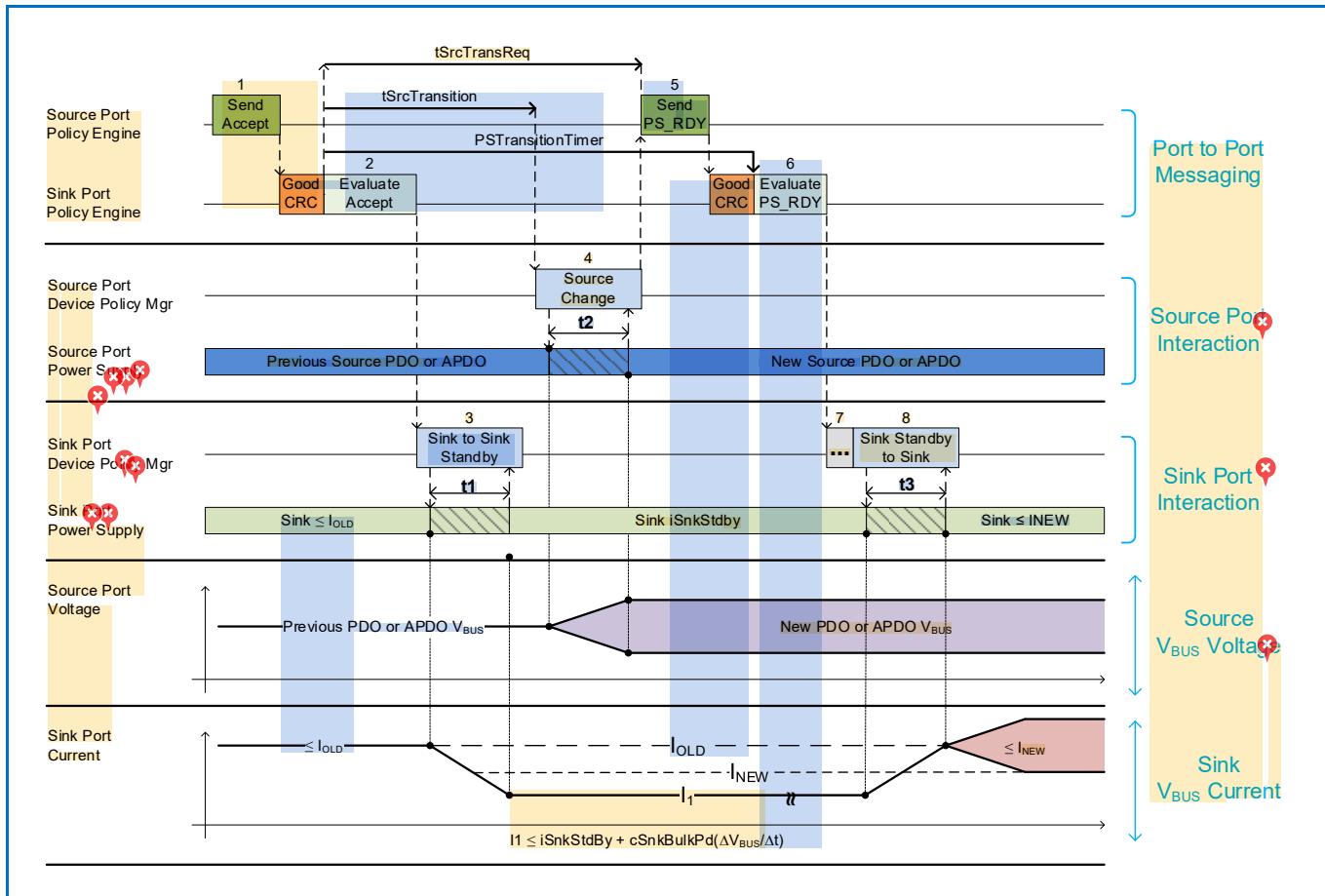


Table 7.1 “Sequence Description for Changing the Source to another (A)PDO”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>Accept</i> Message to the Sink.	Policy Engine receives the <i>Accept</i> Message.
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to change to the new Source (A)PDO.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then starts the <i>PSTransitionTimer</i> and evaluates the <i>Accept</i> Message. There are 3 cases: <ol style="list-style-type: none"> 1) If the voltage is expected to increase between different (A)PDOS, the Sink Port Current <i>Shall</i> be decreased to <i>iSinkStdby</i>. 2) If the voltage is not expected to increase and I_{NEW} is lower than I_{OLD} the current <i>Shall</i> be reduced to I_{NEW}. 3) If the voltage is not expected to increase and I_{NEW} is greater than or equal to I_{OLD} the Sink Port Current <i>May</i> remain the same.
3		For case 1) in Step 2 the Policy Engine tells the Device Policy Manager to instruct the power supply to reduce current drawn to <i>iSinkStdby</i> within <i>tSinkStdby</i> (t_1); t_1 <i>Shall</i> complete before <i>tSrcTransition</i> . The Sink <i>Shall Not</i> violate transient load behavior defined in Section 7.2.6 “Transient Load Behavior” while transitioning to and operating at the new power level.
4	✖ <i>tSrcTransition</i> after the <i>GoodCRC</i> Message was received the Source starts to change to the new (A)PDO. The Source <i>Shall</i> be ready to operate at the new power level within <i>tSrcReady</i> (t_2). The power supply informs the Device Policy Manager that it is ready to operate at the new power level. The power supply status is passed to the Policy Engine.	
5	✖ The Policy Engine sends the <i>PS_RDY</i> Message to the Sink starting within <i>tSrcTransReq</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> Message.	The Policy Engine receives the <i>PS_RDY</i> Message from the Source.
6	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then stops the <i>PSTransitionTimer</i> , evaluates the <i>PS_RDY</i> Message from the Source and tells the Device Policy Manager that the Source is operating at the new (A)PDO. If the <i>PS_RDY</i> Message is not received before <i>PSTransitionTimer</i> times out the Sink sends <i>Hard Reset</i> signaling.
7		✖ The Sink <i>May</i> begin operating at the new power level any time after evaluation of the <i>PS_RDY</i> Message. This time duration is indeterminate.
8		✖ The Sink <i>Shall Not</i> violate the transient load behavior defined in Section 7.2.6 “Transient Load Behavior” while transitioning to and operating at the new power level. The time duration (t_3) depends on the magnitude of the load change.

7.3.1.1.2 Examples of changes from one (A)PDO to another (A)PDO

The seven examples of (A)PDO change transitions below illustrate the most common transitions.

7.3.1.1.2.1 Increasing the Voltage

The interaction of the System Policy, Device Policy, and power supply that **Shall** be followed when changing from one (A)PDO to another while increasing the Voltage is shown in [Figure 7-24 “Transition Diagram for Increasing the Voltage”](#). The sequence that **Shall** be followed is described in [Table 7.2 “Sequence Description for Increasing the Voltage”](#). The timing parameters that **Shall** be followed are listed in [Table 7.25 “Source Electrical Parameters”](#), [Table 7.26 “Sink Electrical Parameters”](#), and [Table 7.27 “Common Source/Sink Electrical Parameters”](#). Note in this figure, the Sink has previously sent a **Request** Message to the Source.

[Figure 7-24 “Transition Diagram for Increasing the Voltage”](#)

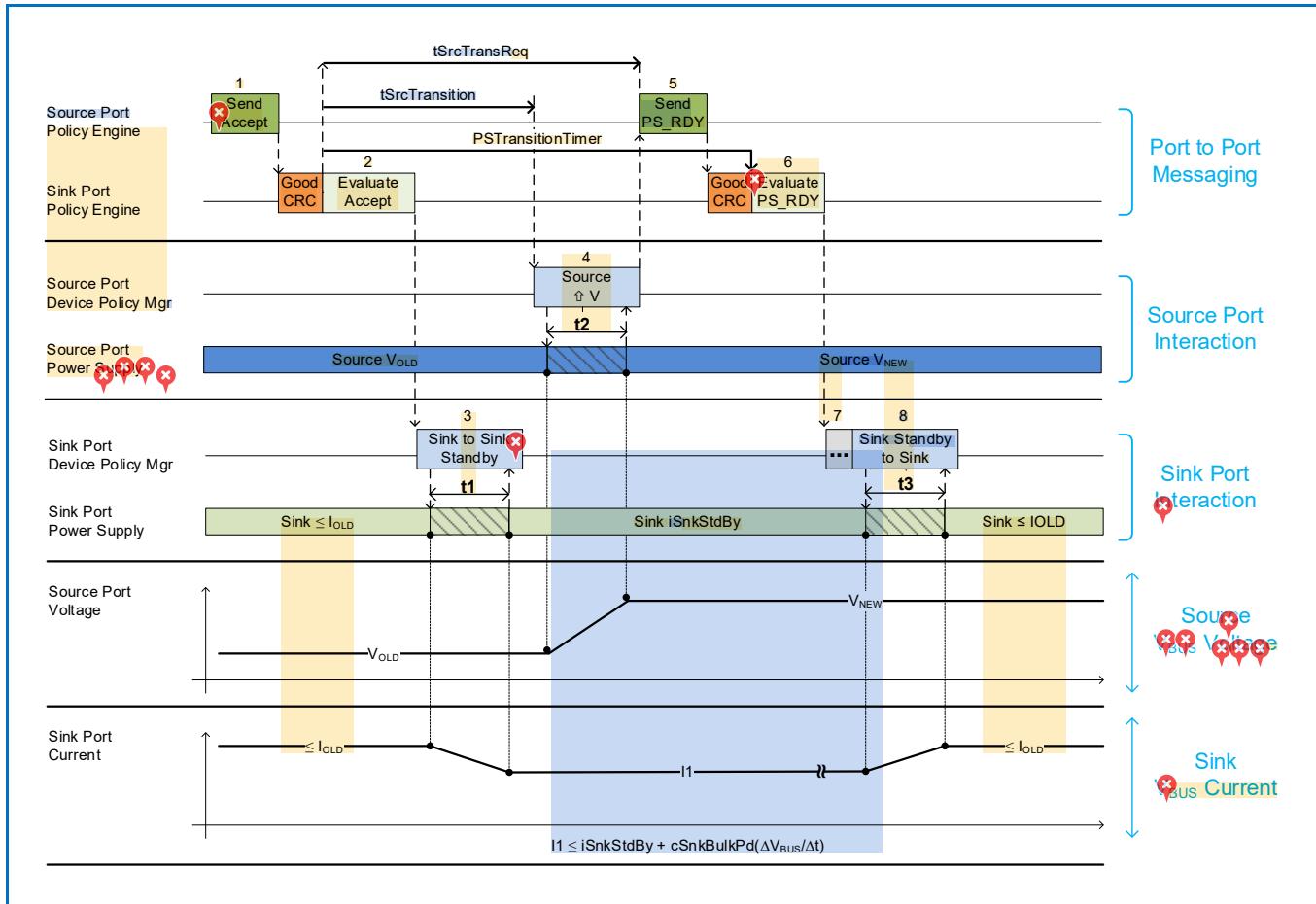


Table 7.2 “Sequence Description for Increasing the Voltage”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>Accept</i> Message to the Sink.	Policy Engine receives the <i>Accept</i> Message.
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to modify its output power.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then starts the <i>PSTransitionTimer</i> and evaluates the <i>Accept</i> Message.
3		Policy Engine tells the Device Policy Manager to instruct the power supply to reduce current drawn to <i>tSnkStdby</i> within <i>tSnkStdby</i> (t1); t1 <i>Shall</i> complete before <i>tSrcTransition</i> . The Sink <i>Shall Not</i> violate transient load behavior defined in <i>Section 7.2.6 “Transient Load Behavior”</i> while transitioning to and operating at the new power level.
4	<i>tSrcTransition</i> after the <i>GoodCRC</i> Message was received, the power supply starts to change its output power capability. The power supply <i>Shall</i> be ready to operate at the new power level within <i>tSrcReady</i> (t2). The power supply informs the Device Policy Manager that it is ready to operate at the new power level. The power supply status is passed to the Policy Engine.	
5	The Policy Engine sends the <i>PS_RDY</i> Message to the Sink starting within <i>tSrcTransReq</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> message.	The Policy Engine receives the <i>PS_RDY</i> Message from the Source.
6	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then stops the <i>PSTransitionTimer</i> , evaluates the <i>PS_RDY</i> Message from the Source and tells the Device Policy Manager that the Source is operating at the new (A)PDO. If the <i>PS_RDY</i> Message is not received before <i>PSTransitionTimer</i> times out the Sink sends <i>Hard Reset</i> signaling.
7		The Sink <i>May</i> begin operating at the new power level any time after evaluation of the <i>PS_RDY</i> Message. This time duration is indeterminate.
8		The Sink <i>Shall Not</i> violate the transient load behavior defined in <i>Section 7.2.6 “Transient Load Behavior”</i> while transitioning to and operating at the new power level. The time duration (t3) depends on the magnitude of the load change.

7.3.1.1.2.2

Increasing the Voltage and Current

The interaction of the System Policy, Device Policy, and power supply that *Shall* be followed when changing from one (A)PDO to another while increasing the Voltage and current is shown in [Figure 7-25 “Transition Diagram for Increasing the Voltage and Current”](#). The sequence that *Shall* be followed is described in [Table 7.3 “Sequence Diagram for Increasing the Voltage and Current”](#). The timing parameters that *Shall* be followed are listed in [Table 7.25 “Source Electrical Parameters”](#), [Table 7.26 “Sink Electrical Parameters”](#), and [Table 7.27 “Common Source/Sink Electrical Parameters”](#). Note in this figure, the Sink has previously sent a *Request* Message to the Source.

[Figure 7-25 “Transition Diagram for Increasing the Voltage and Current”](#)

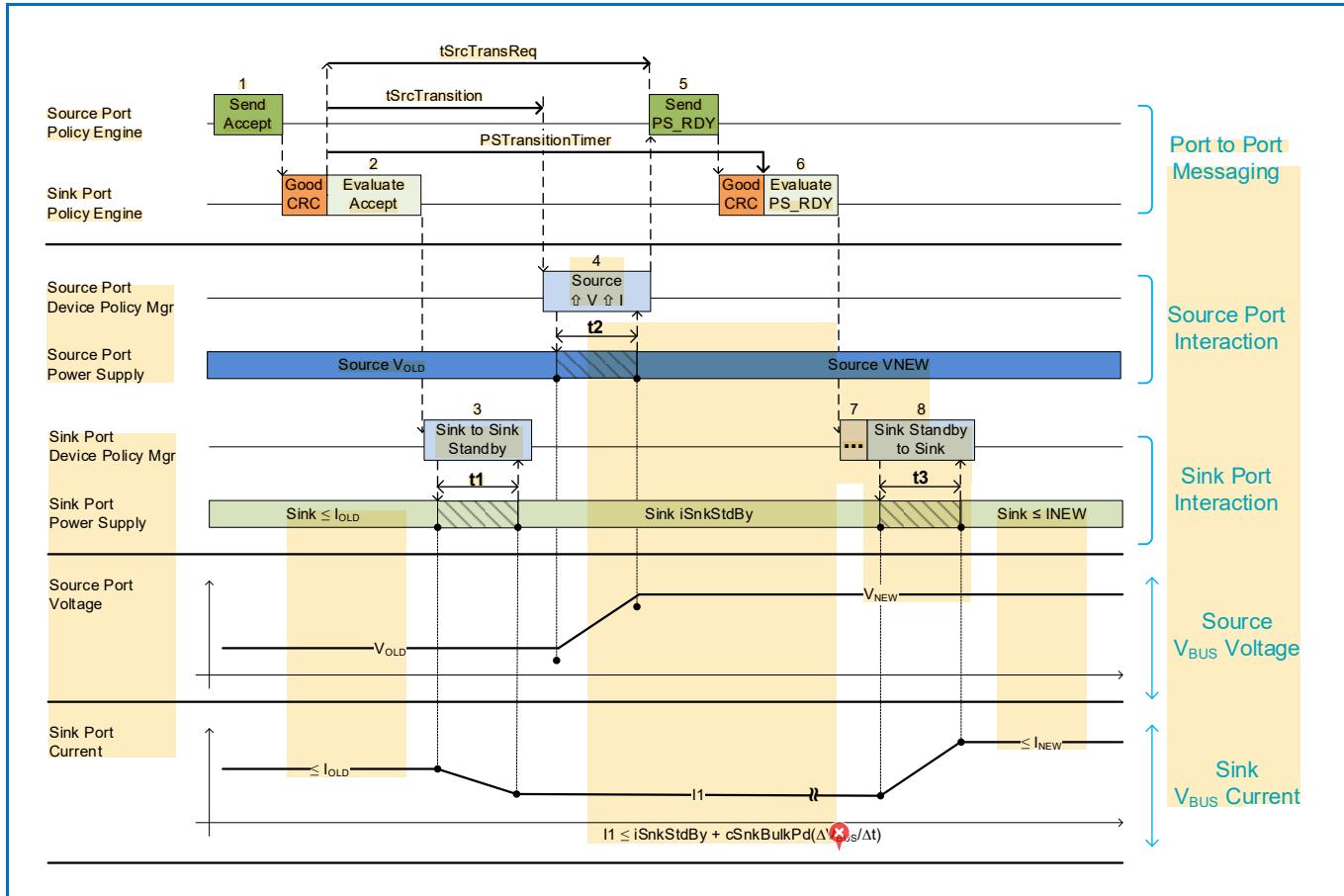


Table 7.3 “Sequence Diagram for Increasing the Voltage and Current”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>Accept</i> Message to the Sink.	Policy Engine receives the <i>Accept</i> .
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to modify its output power.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then starts the <i>PSTransitionTimer</i> and evaluates the <i>Accept</i> Message.
3		Policy Engine tells the Device Policy Manager to instruct the power supply to reduce current drawn to <i>tSnkStdby</i> within <i>tSnkStdby</i> (t1); t1 <i>Shall</i> complete before <i>tSrcTransition</i> . The Sink <i>Shall Not</i> violate transient load behavior defined in <i>Section 7.2.6 “Transient Load Behavior”</i> while transitioning to and operating at the new power level.
4	<i>tSrcTransition</i> after the <i>GoodCRC</i> Message was received, the power supply starts to change its output power capability. The power supply <i>Shall</i> be ready to operate at the new power level within <i>tSrcReady</i> (t2). The power supply informs the Device Policy Manager that it is ready to operate at the new power level. The power supply status is passed to the Policy Engine.	
5	The Policy Engine sends the <i>PS_RDY</i> Message to the Sink starting within <i>tSrcTransReq</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> message.	The Policy Engine receives the <i>PS_RDY</i> Message from the Source.
6	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then stops the <i>PSTransitionTimer</i> , evaluates the <i>PS_RDY</i> Message from the Source and tells the Device Policy Manager that the Source is operating at the new (A)PDO. If the <i>PS_RDY</i> Message is not received before <i>PSTransitionTimer</i> times out, the Sink sends <i>Hard Reset</i> signaling.
7		The Sink <i>May</i> begin operating at the new power level any time after evaluation of the <i>PS_RDY</i> Message. This time duration is indeterminate.
8		The Sink <i>Shall Not</i> violate the transient load behavior defined in <i>Section 7.2.6 “Transient Load Behavior”</i> while transitioning to and operating at the new power level. The time duration (t3) depends on the magnitude of the load change.

7.3.1.1.2.3

Increasing the Voltage and Decreasing the Current

The interaction of the System Policy, Device Policy, and power supply that *Shall* be followed when changing from one (A)PDO to another while increasing the Voltage and decreasing the current is shown in [Figure 7-26 "Transition Diagram for Increasing the Voltage and Decreasing the Current"](#). The sequence that *Shall* be followed is described in [Table 7.4 "Sequence Description for Increasing the Voltage and Decreasing the Current"](#). The timing parameters that *Shall* be followed are listed in [Table 7.25 "Source Electrical Parameters"](#), [Table 7.26 "Sink Electrical Parameters"](#), and [Table 7.27 "Common Source/Sink Electrical Parameters"](#). Note in this figure, the Sink has previously sent a **Request** Message to the Source.

[Figure 7-26 "Transition Diagram for Increasing the Voltage and Decreasing the Current"](#)

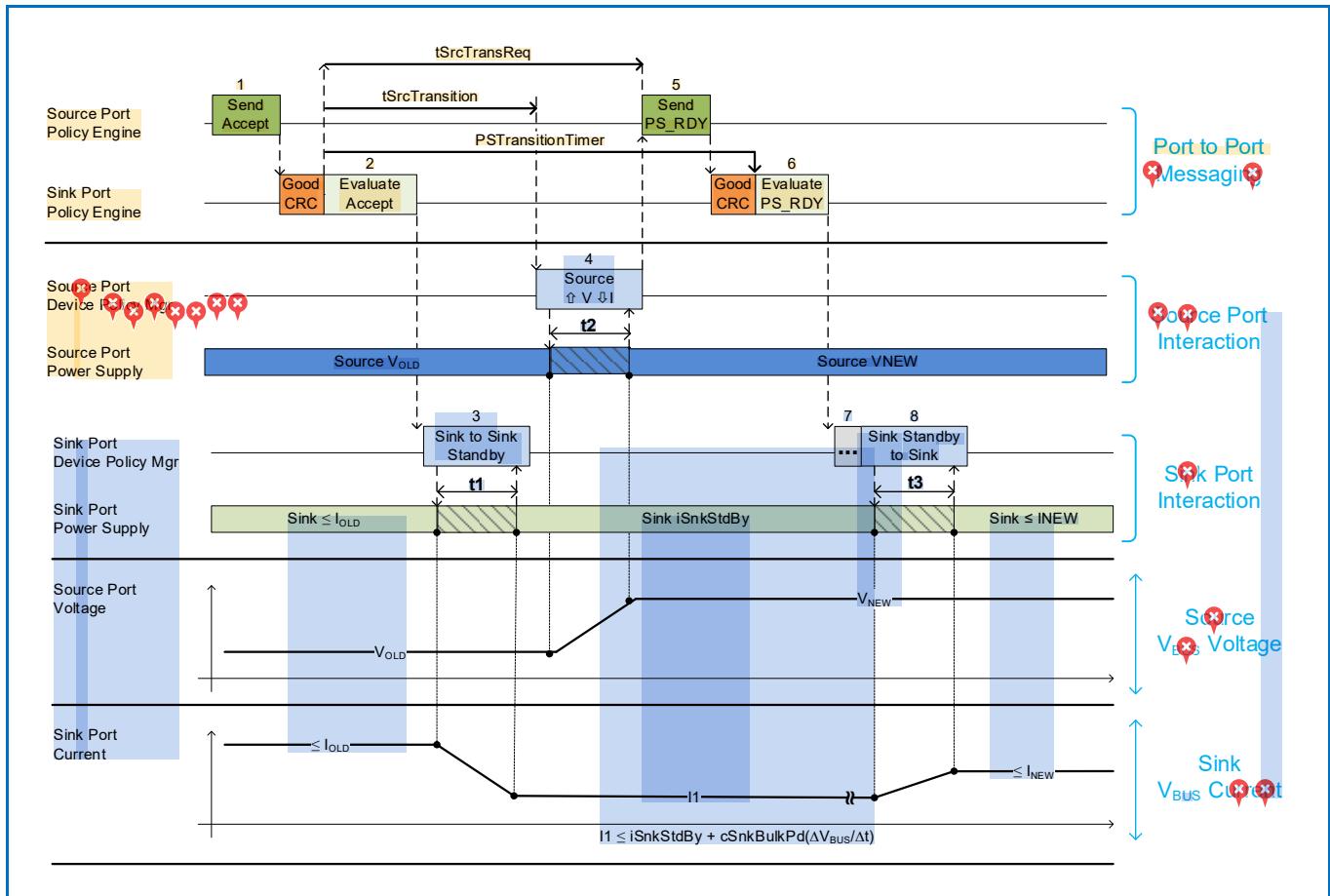


Table 7.4 “Sequence Description for Increasing the Voltage and Decreasing the Current”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>Accept</i> Message to the Sink.	Policy Engine receives the <i>Accept</i> Message.
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to modify its output power.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then starts the <i>PSTransitionTimer</i> and evaluates the <i>Accept</i> Message.
3		Policy Engine tells the Device Policy Manager to instruct the power supply to reduce current drawn to <i>tSnkStdby</i> within <i>tSnkStdby</i> (t1); t1 <i>Shall</i> complete before <i>tSrcTransition</i> . The Sink <i>Shall Not</i> violate transient load behavior defined in <i>Section 7.2.6 “Transient Load Behavior”</i> while transitioning to and operating at the new power level.
4	<i>tSrcTransition</i> after the <i>GoodCRC</i> Message was received, the power supply starts to change its output power capability. The power supply <i>Shall</i> be ready to operate at the new power level within <i>tSrcReady</i> (t2). The power supply informs the Device Policy Manager that it is ready to operate at the new power level. The power supply status is passed to the Policy Engine.	
5	The Policy Engine sends the <i>PS_RDY</i> Message to the Sink starting within <i>tSrcTransReq</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> message.	The Policy Engine receives the <i>PS_RDY</i> Message from the Source.
6	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then stops the <i>PSTransitionTimer</i> , evaluates the <i>PS_RDY</i> Message from the Source and tells the Device Policy Manager that the Source is operating at the new (A)PDO. If the <i>PS_RDY</i> Message is not received before <i>PSTransitionTimer</i> times out the Sink sends <i>Hard Reset</i> signaling.
7		The Sink <i>May</i> begin operating at the new power level any time after evaluation of the <i>PS_RDY</i> Message. This time duration is indeterminate.
8		The Sink <i>Shall Not</i> violate the transient load behavior defined in <i>Section 7.2.6 “Transient Load Behavior”</i> while transitioning to and operating at the new power level. The time duration (t3) depends on the magnitude of the load change.

7.3.1.1.2.4

Decreasing the Voltage and Increasing the Current

The interaction of the System Policy, Device Policy, and power supply that *Shall* be followed when changing from one (A)PDO to another while decreasing the Voltage and increasing the current is shown in [Figure 7-27 "Transition Diagram for Decreasing the Voltage and Increasing the Current"](#). The sequence that *Shall* be followed is described in [Table 7.5 "Sequence Description for Decreasing the Voltage and Increasing the Current"](#). The timing parameters that *Shall* be followed are listed in [Table 7.25 "Source Electrical Parameters"](#), [Table 7.26 "Sink Electrical Parameters"](#), and [Table 7.27 "Common Source/Sink Electrical Parameters"](#). Note in this figure, the Sink has previously sent a **Request** Message to the Source.

[Figure 7-27 "Transition Diagram for Decreasing the Voltage and Increasing the Current"](#)

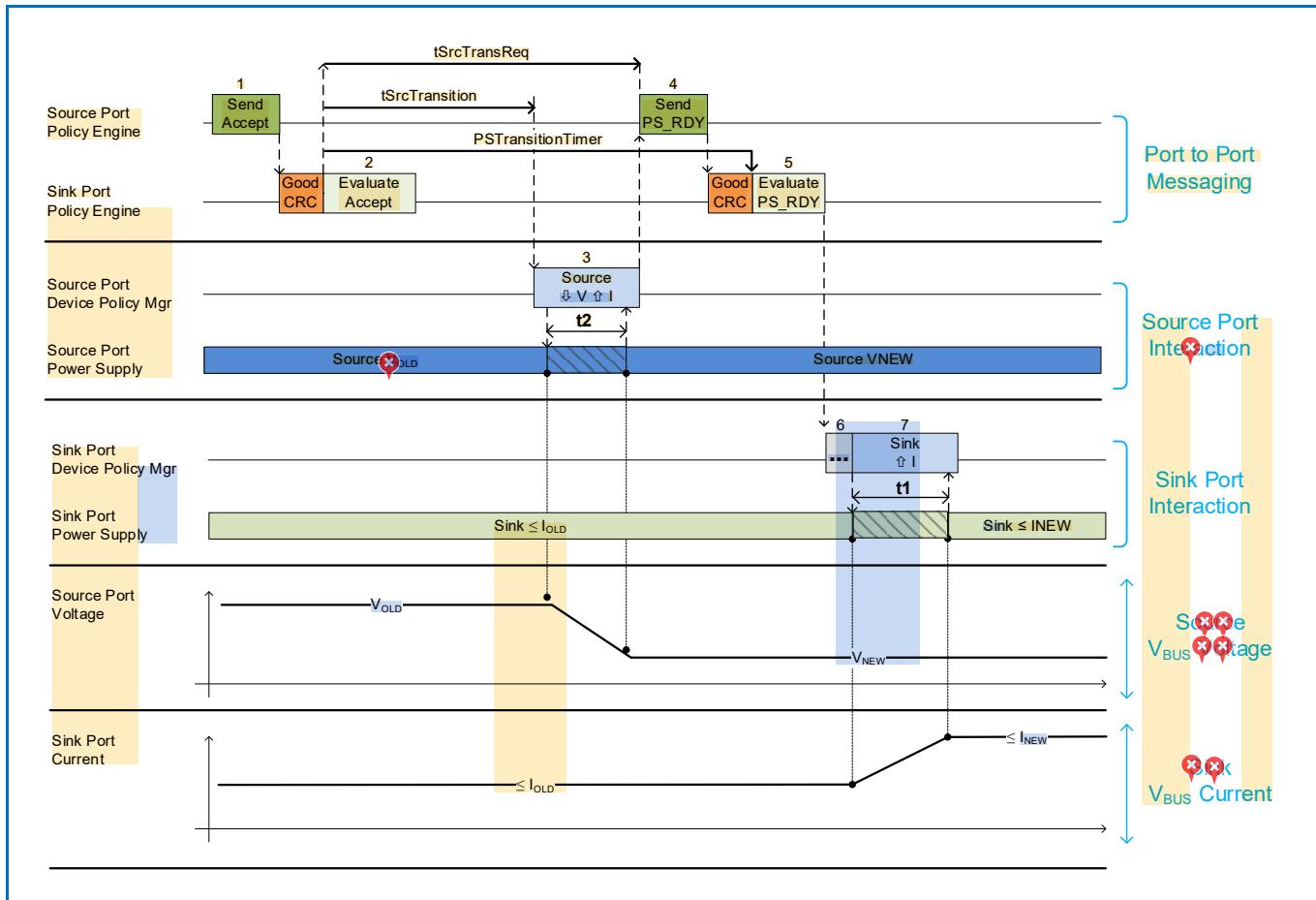


Table 7.5 “Sequence Description for Decreasing the Voltage and Increasing the Current”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>Accept</i> Message to the Sink.	Policy Engine receives the <i>Accept</i> Message.
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to modify its output power.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then starts the <i>PSTransitionTimer</i> and evaluates the <i>Accept</i> Message.
3	<i>tSrcTransition</i> after the <i>GoodCRC</i> Message was received, the power supply starts to change its output power capability. The power supply <i>Shall</i> be ready to operate at the new power level within <i>tSrcReady</i> (t1). The power supply informs the Device Policy Manager that it is ready to operate at the new power level. The power supply status is passed to the Policy Engine.	
4	The Policy Engine sends the <i>PS_RDY</i> Message to the Sink starting within <i>tSrcTransReq</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> message.	The Policy Engine receives the <i>PS_RDY</i> Message from the Source.
5	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then evaluates the <i>PS_RDY</i> Message from the Source and tells the Device Policy Manager it is okay to operate at the new power level.
6		The Sink <i>May</i> begin operating at the new power level any time after evaluation of the <i>PS_RDY</i> Message. This time duration is indeterminate.
7		The Sink <i>Shall Not</i> violate the transient load behavior defined in Section 7.2.6 “Transient Load Behavior” while transitioning to and operating at the new power level. The time duration (t2) depends on the magnitude of the load change.

7.3.1.1.2.5

Decreasing the Voltage

The interaction of the System Policy, Device Policy, and power supply that **Shall** be followed when changing from one (A)PDO to another while decreasing the Voltage is shown in [Figure 7-28 “Transition Diagram for Decreasing the Voltage”](#). The sequence that **Shall** be followed is described in [Table 7.6 “Sequence Description for Decreasing the Voltage”](#). The timing parameters that **Shall** be followed are listed in [Table 7.25 “Source Electrical Parameters”](#), [Table 7.26 “Sink Electrical Parameters”](#), and [Table 7.27 “Common Source/Sink Electrical Parameters”](#). Note in this figure, the Sink has previously sent a **Request** Message to the Source.

[Figure 7-28 “Transition Diagram for Decreasing the Voltage”](#)

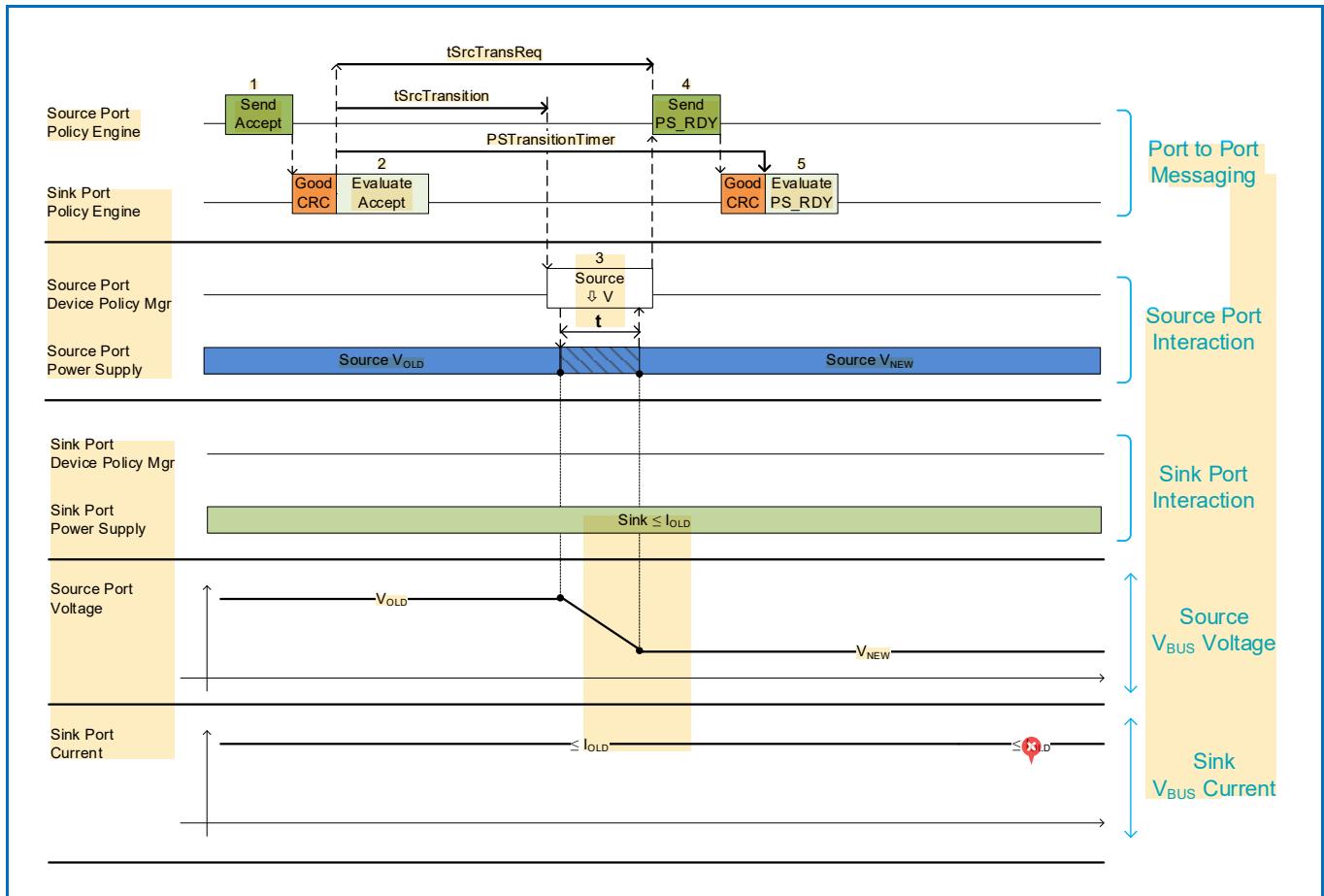


Table 7.6 “Sequence Description for Decreasing the Voltage”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>Accept</i> Message to the Sink.	Policy Engine receives the <i>Accept</i> Message.
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to modify its output power.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then starts the <i>PSTransitionTimer</i> and evaluates the <i>Accept</i> Message.
3	<i>tSrcTransition</i> after the <i>GoodCRC</i> Message was received, the power supply starts to change its output power capability. The power supply <i>Shall</i> be ready to operate at the new power level within <i>tSrcReady</i> (t1). The power supply informs the Device Policy Manager that it is ready to operate at the new power level. The power supply status is passed to the Policy Engine.	
4	The Policy Engine sends the <i>PS_RDY</i> Message to the Sink within <i>tSrcTransReq</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> message.	The Policy Engine receives the <i>PS_RDY</i> Message from the Source.
5	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then stops the <i>PSTransitionTimer</i> , evaluates the <i>PS_RDY</i> Message from the Source and tells the Device Policy Manager that the Source is operating at the new (A)PDO. If the <i>PS_RDY</i> Message is not received before <i>PSTransitionTimer</i> times out the Sink sends <i>Hard Reset</i> signaling.

7.3.1.1.2.6

Decreasing the Voltage and the Current

The interaction of the System Policy, Device Policy, and power supply that *Shall* be followed when changing from one (A)PDO to another while decreasing the Voltage and current is shown in [Figure 7-30 “Transition Diagram for no change in Current or Voltage”](#). The sequence that *Shall* be followed is described in [Table 7.7 “Sequence Description for Decreasing the Voltage and the Current”](#). The timing parameters that *Shall* be followed are listed in [Table 7.25 “Source Electrical Parameters”](#), [Table 7.26 “Sink Electrical Parameters”](#), and [Table 7.27 “Common Source/Sink Electrical Parameters”](#). Note in this figure, the Sink has previously sent a *Request* Message to the Source.

[Figure 7-29 “Transition Diagram for Decreasing the Voltage and the Current”](#)

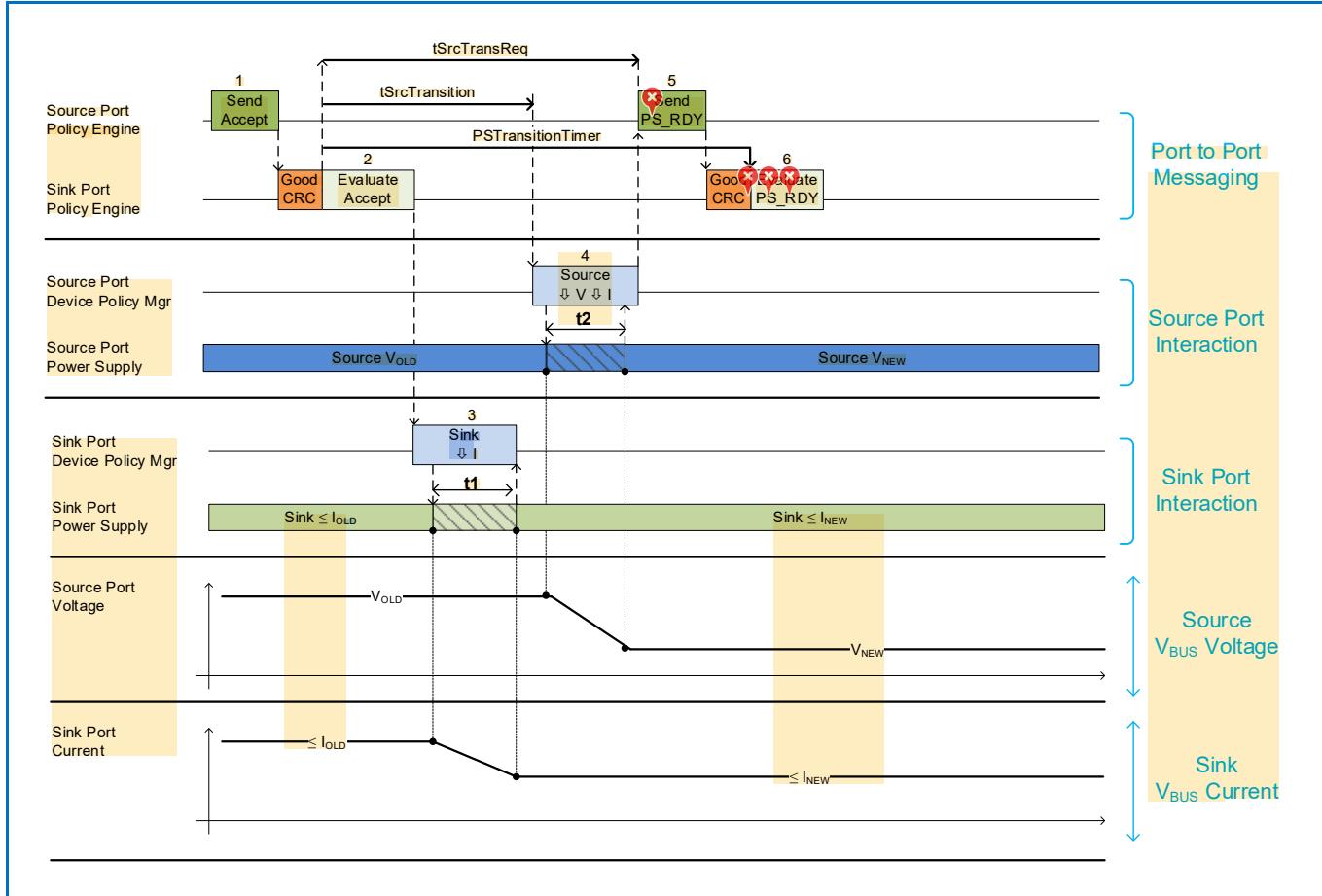


Table 7.7 “Sequence Description for Decreasing the Voltage and the Current”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>Accept</i> Message to the Sink.	Policy Engine receives the <i>Accept</i> Message.
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to modify its output power.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then starts the <i>PSTransitionTimer</i> and evaluates the <i>Accept</i> Message.
3		The Sink Shall be able to operate with lower current within <i>tSnkNewPower</i> (t1); t1 <i>Shall</i> complete before <i>tSrcTransition</i> . The Sink <i>Shall Not</i> violate transient load behavior defined in <i>Section 7.2.6 “Transient Load Behavior”</i> while transitioning to and operating at the new power level.
4	<i>tSrcTransition</i> after the <i>GoodCRC</i> Message was received, the power supply starts to change its output power capability. The power supply <i>Shall</i> be ready to operate at the new power level within <i>tSrcReady</i> (t2). The power supply informs the Device Policy Manager that it is ready to operate at the new power level. The power supply status is passed to the Policy Engine.	
5	The Policy Engine sends the <i>PS_RDY</i> Message to the Sink starting within <i>tSrcTransReq</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> message.	The Policy Engine receives the <i>PS_RDY</i> Message from the Source.
6	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then stops the <i>PSTransitionTimer</i> , evaluates the <i>PS_RDY</i> Message from the Source and tells the Device Policy Manager that the Source is operating at the new (A)PDO. If the <i>PS_RDY</i> Message is not received before <i>PSTransitionTimer</i> times out the Sink sends <i>Hard Reset</i> signaling.
7		The Sink <i>Shall Not</i> violate the transient load behavior defined in <i>Section 7.2.6 “Transient Load Behavior”</i> while transitioning to and operating at the new power level.

7.3.1.1.2.7

No change in Current or Voltage

The interaction of the System Policy, Device Policy, and power supply that **Shall** be followed when changing from one (A)PDO to another while the Sink requests the same Voltage and Current as it is currently operating at is shown in **Figure 7-30 “Transition Diagram for no change in Current or Voltage”**. The sequence that **Shall** be followed is described in **Table 7.8 “Sequence Description for no change in Current or Voltage”**. The timing parameters that **Shall** be followed are listed in **Table 7.25 “Source Electrical Parameters”**, **Table 7.26 “Sink Electrical Parameters”**, and **Table 7.27 “Common Source/Sink Electrical Parameters”**. Note in this figure, the Sink has previously sent a **Request** Message to the Source.

Figure 7-30 “Transition Diagram for no change in Current or Voltage”

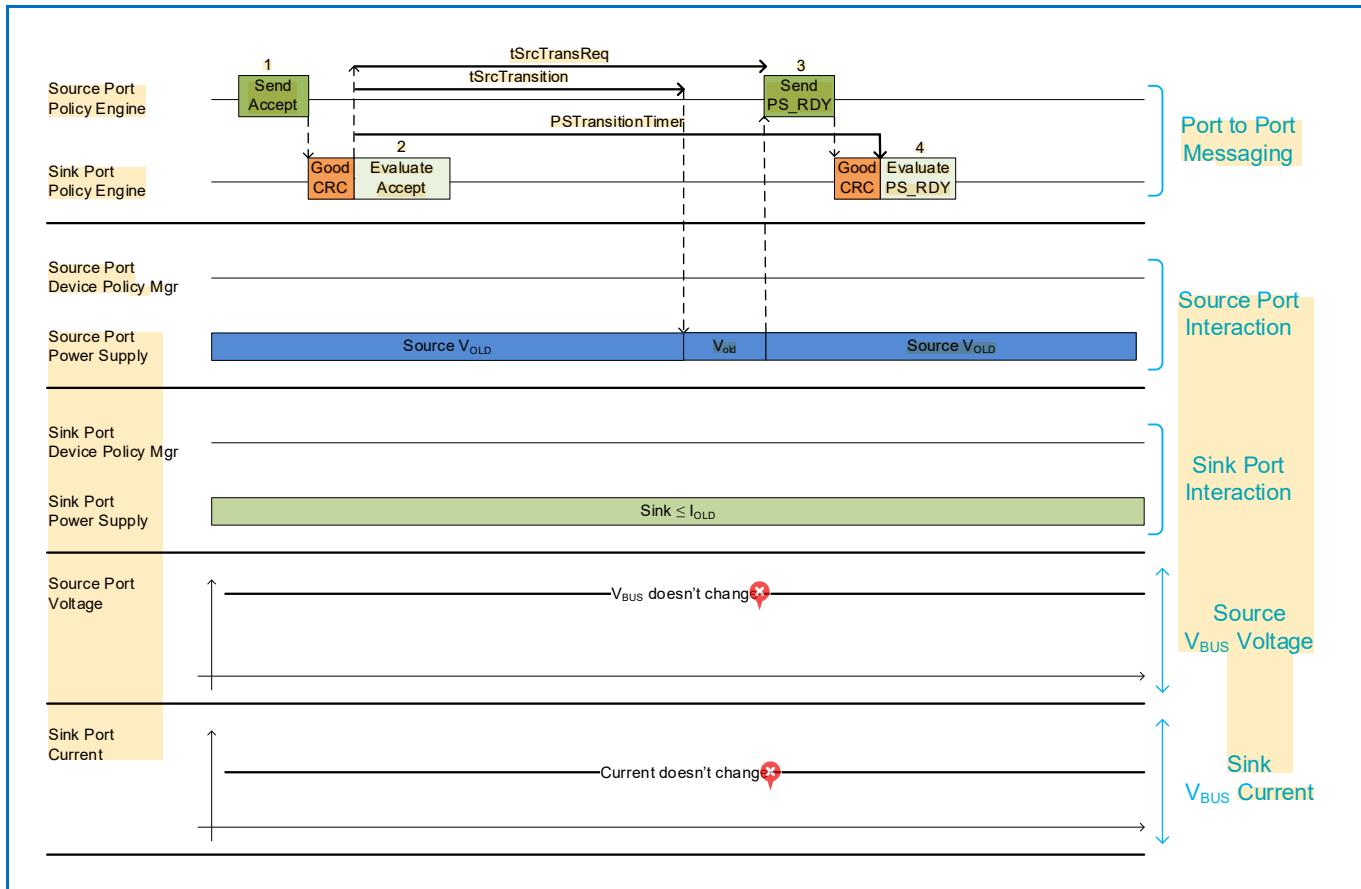


Table 7.8 “Sequence Description for no change in Current or Voltage”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>Accept</i> Message to the Sink.	Policy Engine receives the <i>Accept</i> Message.
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then starts the <i>PSTransitionTimer</i> and evaluates the <i>Accept</i> Message.
3	The Policy Engine waits <i>tSrcTransition</i> then sends the <i>PS_RDY</i> Message to the Sink starting within <i>tSrcTransReq</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> message.	Policy Engine receives the <i>PS_RDY</i> Message.
4	Policy Engine receives the <i>GoodCRC</i> Message from the Sink. Note: the decision that no power transition is required could be made either by the Device Policy Manager or the power supply depending on implementation.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine evaluates the <i>PS_RDY</i> Message.

7.3.1.2 Transitions within the same Fixed, Battery or Variable PDO or between Different (A)PDOs

7.3.1.2.1 Increasing the Current Only

The interaction of the System Policy, Device Policy, and power supply that *Shall* be followed when increasing the current without changing the voltage is shown in [Figure 7-31 “Transition Diagram for Increasing the Current”](#). The sequence that *Shall* be followed is described in [Table 7.9 “Sequence Description for Increasing the Current”](#). The timing parameters that *Shall* be followed are listed in [Table 7.25 “Source Electrical Parameters”](#), [Table 7.26 “Sink Electrical Parameters”](#), and [Table 7.27 “Common Source/Sink Electrical Parameters”](#). Note in this figure, the Sink has previously sent a **Request** Message to the Source.

[Figure 7-31 “Transition Diagram for Increasing the Current”](#)

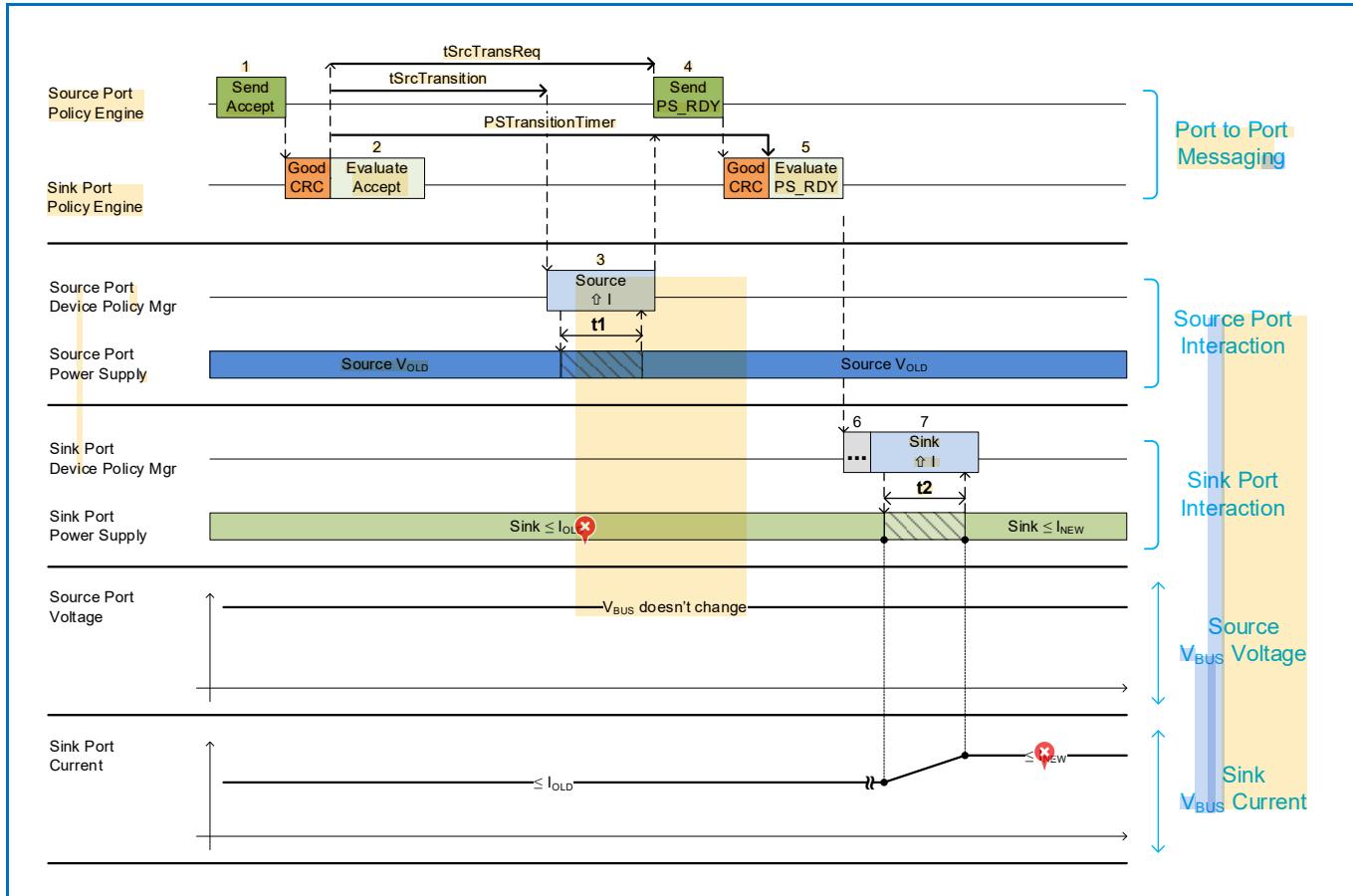


Table 7.9 “Sequence Description for Increasing the Current”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>Accept</i> Message to the Sink.	Policy Engine receives the <i>Accept</i> Message.
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to modify its output power.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then starts the <i>PSTransitionTimer</i> and evaluates the <i>Accept</i> Message.
3	<i>tSrcTransition</i> after the <i>GoodCRC</i> Message was received, the power supply starts to change its output power capability. The power supply <i>Shall</i> be ready to operate at the new power level within <i>tSrcReady</i> (t1). The power supply informs the Device Policy Manager that it is ready to operate at the new power level. The power supply status is passed to the Policy Engine.	
4	The Policy Engine sends the <i>PS_RDY</i> Message to the Sink starting within <i>tSrcTransReq</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> message.	The Policy Engine receives the <i>PS_RDY</i> Message from the Source.
5	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then stops the <i>PSTransitionTimer</i> , evaluates the <i>PS_RDY</i> Message from the Source and tells the Device Policy Manager that the Source is operating at the new (A)PDO. If the <i>PS_RDY</i> Message is not received before <i>PSTransitionTimer</i> times out the Sink sends <i>Hard Reset</i> signaling.
6		The Sink <i>May</i> begin operating at the new power level any time after evaluation of the <i>PS_RDY</i> Message. This time duration is indeterminate.
7		The Sink <i>Shall Not</i> violate the transient load behavior defined in Section 7.2.6 “Transient Load Behavior” while transitioning to and operating at the new power level. The time duration (t2) depends on the magnitude of the load change.

7.3.1.2.2

Decreasing the Current Only

The interaction of the System Policy, Device Policy, and power supply that **Shall** be followed when decreasing the current without changing the voltage is shown in [Figure 7-32 “Transition Diagram for Decreasing the Current”](#). The sequence that **Shall** be followed is described in [Table 7.10 “Sequence Description for Decreasing the Current”](#). The timing parameters that **Shall** be followed are listed in [Table 7.25 “Source Electrical Parameters”](#), [Table 7.26 “Sink Electrical Parameters”](#), and [Table 7.27 “Common Source/Sink Electrical Parameters”](#). Note in this figure, the Sink has previously sent a **Request** Message to the Source.

[Figure 7-32 “Transition Diagram for Decreasing the Current”](#)

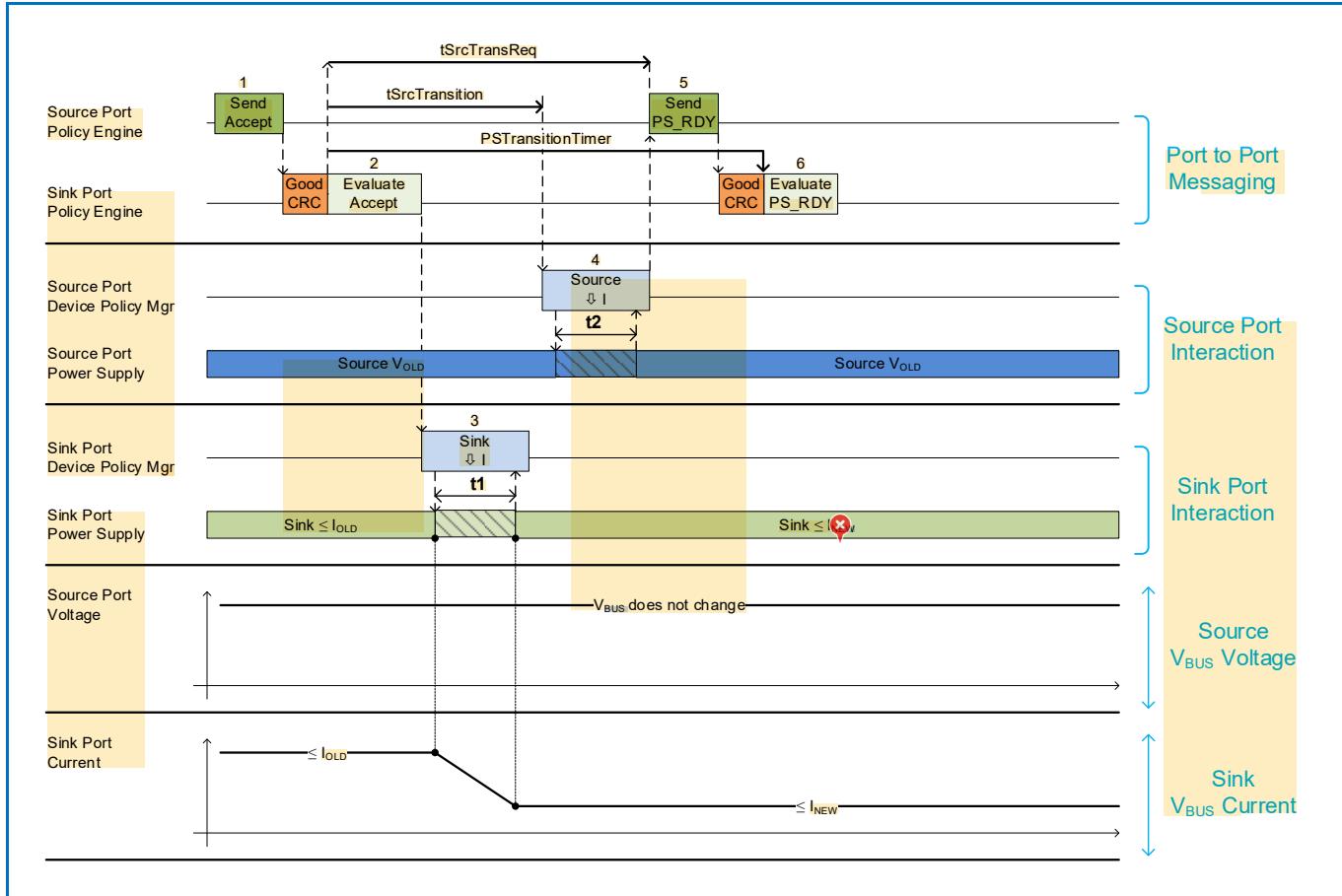


Table 7.10 “Sequence Description for Decreasing the Current”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>Accept</i> Message to the Sink.	Policy Engine receives the <i>Accept</i> Message.
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to modify its output power.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then starts the <i>PSTransitionTimer</i> and evaluates the <i>Accept</i> Message. Policy Engine tells the Device Policy Manager to instruct the power supply to reduce power consumption.
3		The Sink <i>Shall Not</i> violate the transient load behavior defined in Section 7.2.6 “Transient Load Behavior” while transitioning to and operating at the new power level. The Sink Shall be able to operate with lower current within <i>tSnkNewPower</i> (t1); t1 Shall complete before <i>tSrcTransition</i> .
4	<i>tSrcTransition</i> after the <i>GoodCRC</i> Message was received, the power supply starts to change its output power capability. The power supply <i>Shall</i> be ready to operate at the new power level within <i>tSrcReady</i> (t2). The power supply informs the Device Policy Manager that it is ready to operate at the new power level. The power supply status is passed to the Policy Engine.	
5	The Policy Engine sends the <i>PS_RDY</i> Message to the Sink starting within <i>tSrcTransReq</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> message.	The Policy Engine receives the <i>PS_RDY</i> Message from the Source.
6	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then stops the <i>PSTransitionTimer</i> , evaluates the <i>PS_RDY</i> Message from the Source and tells the Device Policy Manager that the Source is operating at the new (A)PDO. If the <i>PS_RDY</i> Message is not received before <i>PSTransitionTimer</i> times out the Sink sends <i>Hard Reset</i> signaling.

7.3.1.3 Changing Voltage or Current within the same PPS APDO

7.3.1.3.1 Increasing the Programmable Power Supply (PPS) Voltage

The interaction of the System Policy, Device Policy, and power supply that *Shall* be followed when increasing the Voltage is shown in [Figure 7-33 “Transition Diagram for Increasing the Programmable Power Supply Voltage”](#). The sequence that *Shall* be followed is described in [Table 7.11 “Sequence Description for Increasing the Programmable Power Supply Voltage”](#). The timing parameters that *Shall* be followed are listed in [Table 7.25 “Source Electrical Parameters”](#), [Table 7.26 “Sink Electrical Parameters”](#), and [Table 7.27 “Common Source/Sink Electrical Parameters”](#). Note in this figure, the Sink has previously sent a *Request* Message to the Source.

Figure 7-33 “Transition Diagram for Increasing the Programmable Power Supply Voltage”

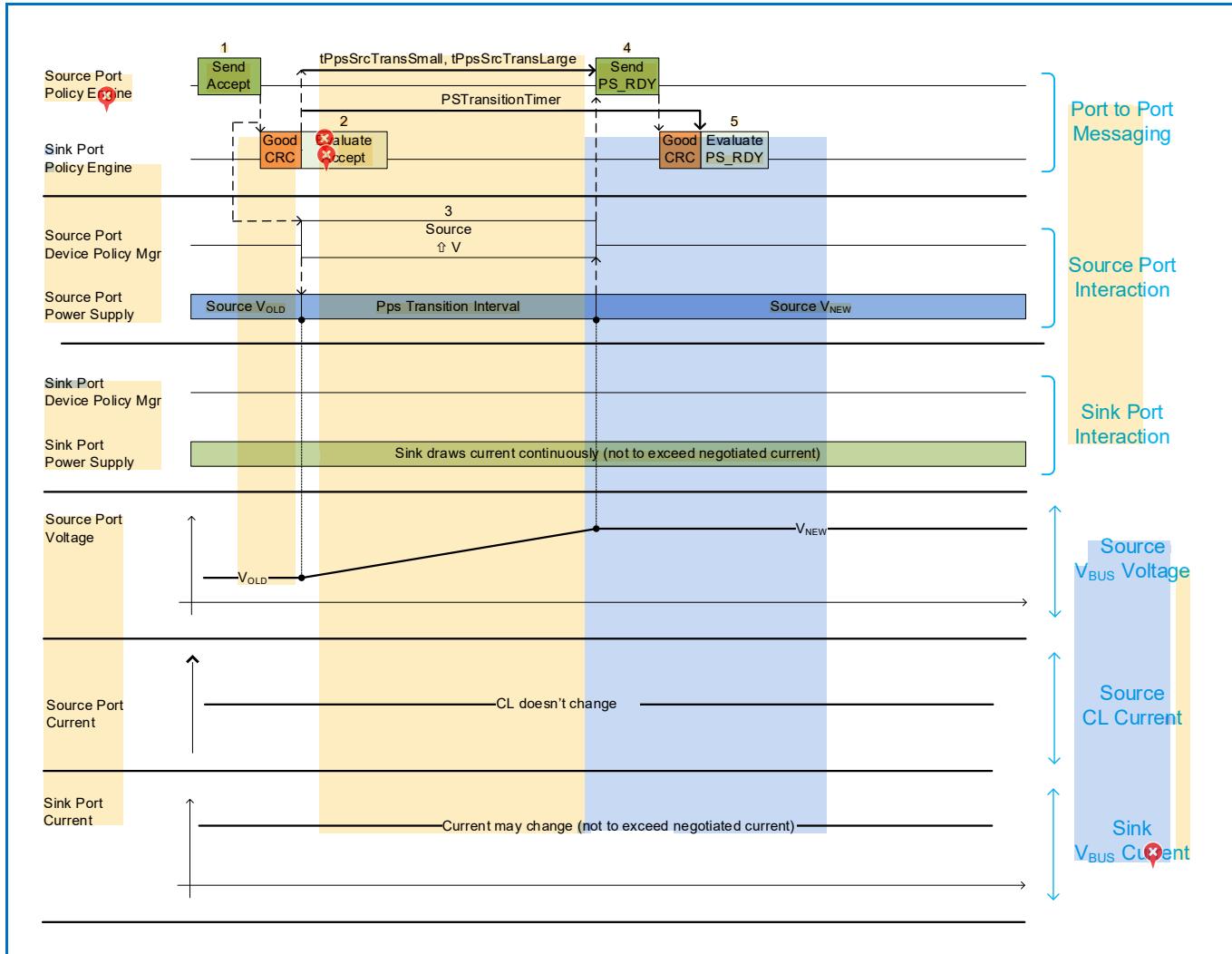


Table 7.11 “Sequence Description for Increasing the Programmable Power Supply Voltage”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>Accept</i> Message to the Sink.	Policy Engine receives the <i>Accept</i> Message.
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to increase its output Voltage.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then starts the <i>PSTransitionTimer</i> and evaluates the <i>Accept</i> Message.
3	After sending the <i>Accept</i> Message, the Programmable Power Supply starts to increase its output Voltage. The Programmable Power Supply new Voltage set-point <i>Shall</i> be reached by <i>tPpsSrcTransLarge</i> for steps larger than <i>vPpsSmallStep</i> or else by <i>tPpsSrcTransSmall</i> . The power supply informs the Device Policy Manager that it has reached the new set-point and whether V_{BUS} is at the corresponding new level, or if the supply is operating in CL mode. The power supply status is passed to the Policy Engine.	
4	✖ The Policy Engine sends the <i>PS_RDY</i> Message to the Sink starting within <i>tPpsSrcTransSmall</i> or <i>tPpsSrcTransLarge</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> Message.	The Policy Engine receives the <i>PS_RDY</i> Message from the Source.
5	✖ Protocol Layer receives the <i>GoodCRC</i> Message from the Sink.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then stops the <i>PSTransitionTimer</i> , evaluates the <i>PS_RDY</i> Message from the Source and tells the Device Policy Manager that the Source is operating at the new voltage set point (corresponding to <i>vPpsNew</i>). If the <i>PS_RDY</i> Message is not received before <i>PSTransitionTimer</i> times out the Sink sends <i>Hard Reset</i> signaling.

7.3.1.3.2

Decreasing the Programmable Power Supply (PPS) Voltage

The interaction of the System Policy, Device Policy, and power supply that *Shall* be followed when decreasing the Voltage is shown in [Figure 7-34 “Transition Diagram for Decreasing the Programmable Power Supply Voltage”](#). The sequence that *Shall* be followed is described in [Table 7.12 “Sequence Description for Decreasing the Programmable Power Supply Voltage”](#). The timing parameters that *Shall* be followed are listed in [Table 7.25 “Source Electrical Parameters”](#), [Table 7.26 “Sink Electrical Parameters”](#), and [Table 7.27 “Common Source/Sink Electrical Parameters”](#). Note in this figure, the Sink has previously sent a *Request* Message to the Source.

Figure 7-34 “Transition Diagram for Decreasing the Programmable Power Supply Voltage”

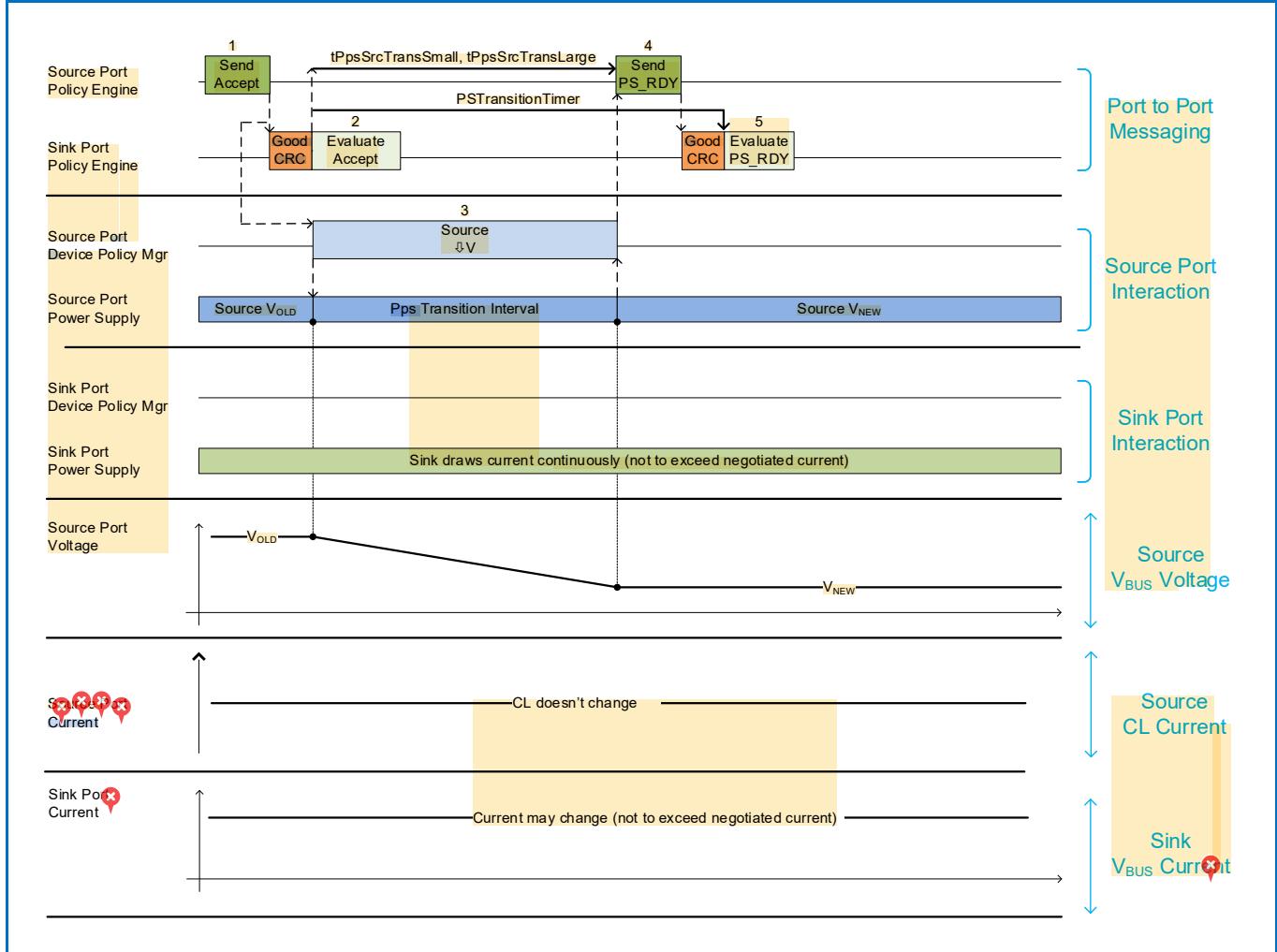


Table 7.12 “Sequence Description for Decreasing the Programmable Power Supply Voltage”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>Accept</i> Message to the Sink.	Policy Engine receives the <i>Accept</i> Message.
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to decrease its output Voltage.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine. Policy Engine then starts the <i>PSTransitionTimer</i> and evaluates the <i>Accept</i> Message.
3	After sending the <i>Accept</i> Message, the Programmable Power Supply starts to decrease its output Voltage. The Programmable Power Supply new Voltage set-point (corresponding to <i>vPpsNew</i>) Shall be reached by <i>tPpsSrcTransLarge</i> for steps larger than <i>vPpsSmallStep</i> or else by <i>tPpsSrcTransSmall</i> . The power supply informs the Device Policy Manager that it has reached the new level. The power supply status is passed to the Policy Engine.	
4	The Policy Engine sends the PS_RDY Message to the Sink starting within <i>tPpsSrcTransSmall</i> or <i>tPpsSrcTransLarge</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> Message.	The Policy Engine receives the <i>PS_RDY</i> Message from the Source.
5	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then stops the <i>PSTransitionTimer</i> , evaluates the <i>PS_RDY</i> Message from the Source and tells the Device Policy Manager that the Source is operating at the new voltage set point (corresponding to <i>vPpsNew</i>). If the <i>PS_RDY</i> Message is not received before <i>PSTransitionTimer</i> times out the Sink sends <i>Hard Reset</i> signaling.

7.3.1.3.3

Increasing the Programmable Power Supply (PPS) Current

The interaction of the System Policy, Device Policy, and power supply that **Shall** be followed when increasing the current limit in the same APDO, not exceeding the maximum for that APDO and without changing the requested Voltage is shown in **Figure 7-35 “Transition Diagram for increasing the Current in PPS mode”**. The sequence that **Shall** be followed is described in **Table 7.13 “Sequence Description for increasing the Current in PPS mode”**. The timing parameters that **Shall** be followed are listed in **Table 7.25 “Source Electrical Parameters”**, **Table 7.26 “Sink Electrical Parameters”**, and **Table 7.27 “Common Source/Sink Electrical Parameters”**. Note in this figure, the Sink has previously sent a **Request** Message to the Source.

The Sink **May** draw current equal to the increasing Current Limit of the Source before it has received the **PS_RDY** Message for the new request.

Figure 7-35 “Transition Diagram for increasing the Current in PPS mode”

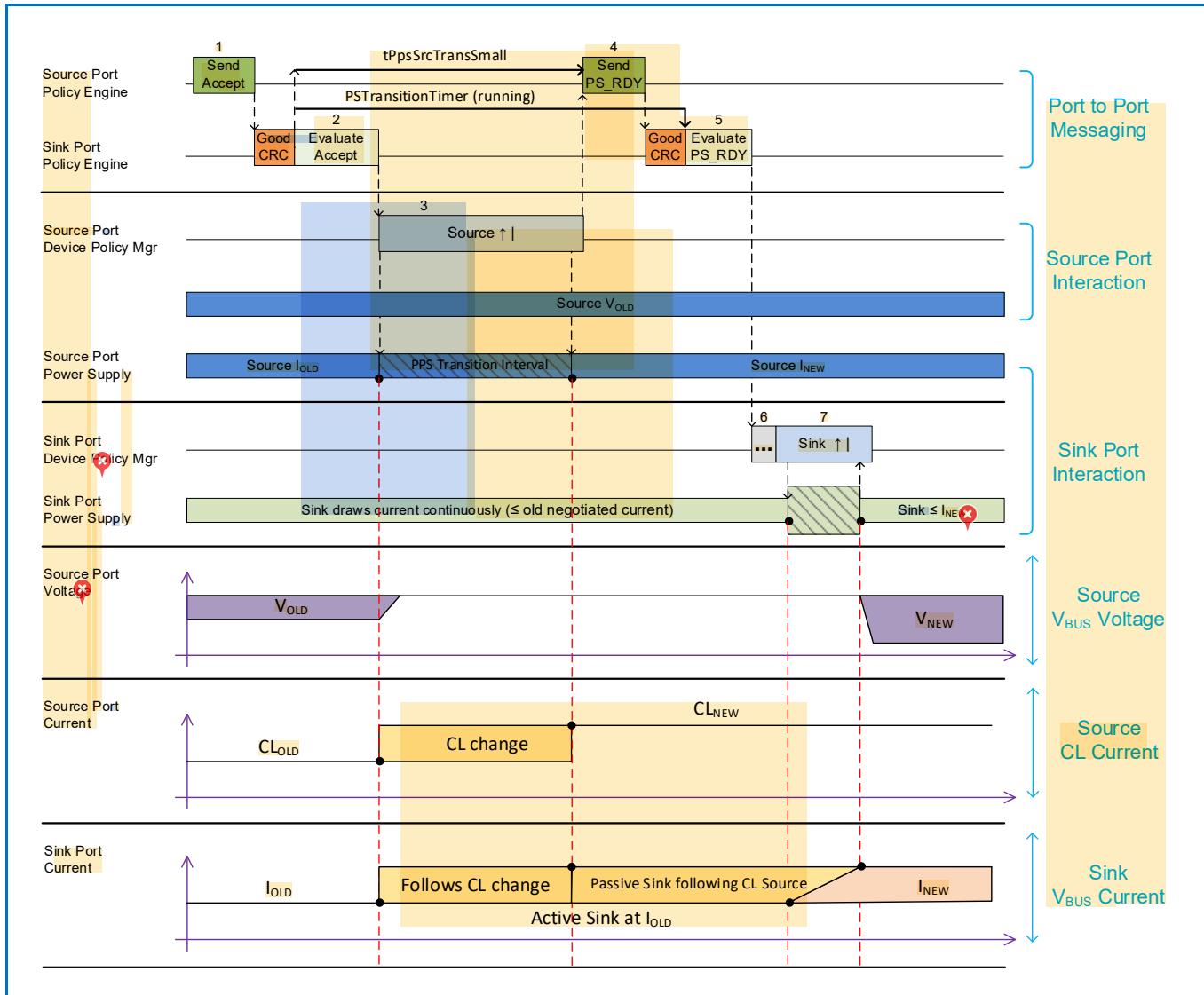


Table 7.13 “Sequence Description for increasing the Current in PPS mode”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>Accept</i> Message to the Sink.	Policy Engine receives the <i>Accept</i> Message.
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to increase its set-point for the current limit.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then starts the <i>PSTransitionTimer</i> and evaluates the <i>Accept</i> Message.
3	The Power Supply increases its Current Limit set-point to the new requested value.	The Sink draws current according to the increased Current Limit of the Source.
4	The Policy Engine waits <i>tPpsSrcTransSmall</i> then sends the <i>PS_RDY</i> Message to the Sink starting within <i>tPpsCLProgramSettle</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> Message.	Policy Engine receives the <i>PS_RDY</i> Message.
5	Policy Engine receives the <i>GoodCRC</i> Message from the Sink.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source.
6		Policy Engine then stops the <i>PSTransitionTimer</i> , evaluates the <i>PS_RDY</i> Message and tells the Device Policy Manager it can increase the current up to the requested value without the Source going into CL mode. If the <i>PS_RDY</i> Message is not received before <i>PSTransitionTimer</i> times out the Sink sends <i>Hard Reset</i> signaling.
7		The Sink increases its current.

7.3.1.3.4

Decreasing the Programmable Power Supply (PPS) Current

The interaction of the System Policy, Device Policy, and power supply that **Shall** be followed when decreasing the current limit in the same APDO, not exceeding the minimum for that APDO and without changing the requested Voltage is shown in [Figure 7-36 “Transition Diagram for decreasing the Current in PPS mode”](#). The sequence that **Shall** be followed is described in [Table 7.14 “Sequence Description for decreasing the Current in PPS mode”](#). The timing parameters that **Shall** be followed are listed in [Table 7.25 “Source Electrical Parameters”, Table 7.26 “Sink Electrical Parameters”, and Table 7.27 “Common Source/Sink Electrical Parameters”](#). Note in this figure, the Sink has previously sent a **Request** Message to the Source.

[Figure 7-36 “Transition Diagram for decreasing the Current in PPS mode”](#)

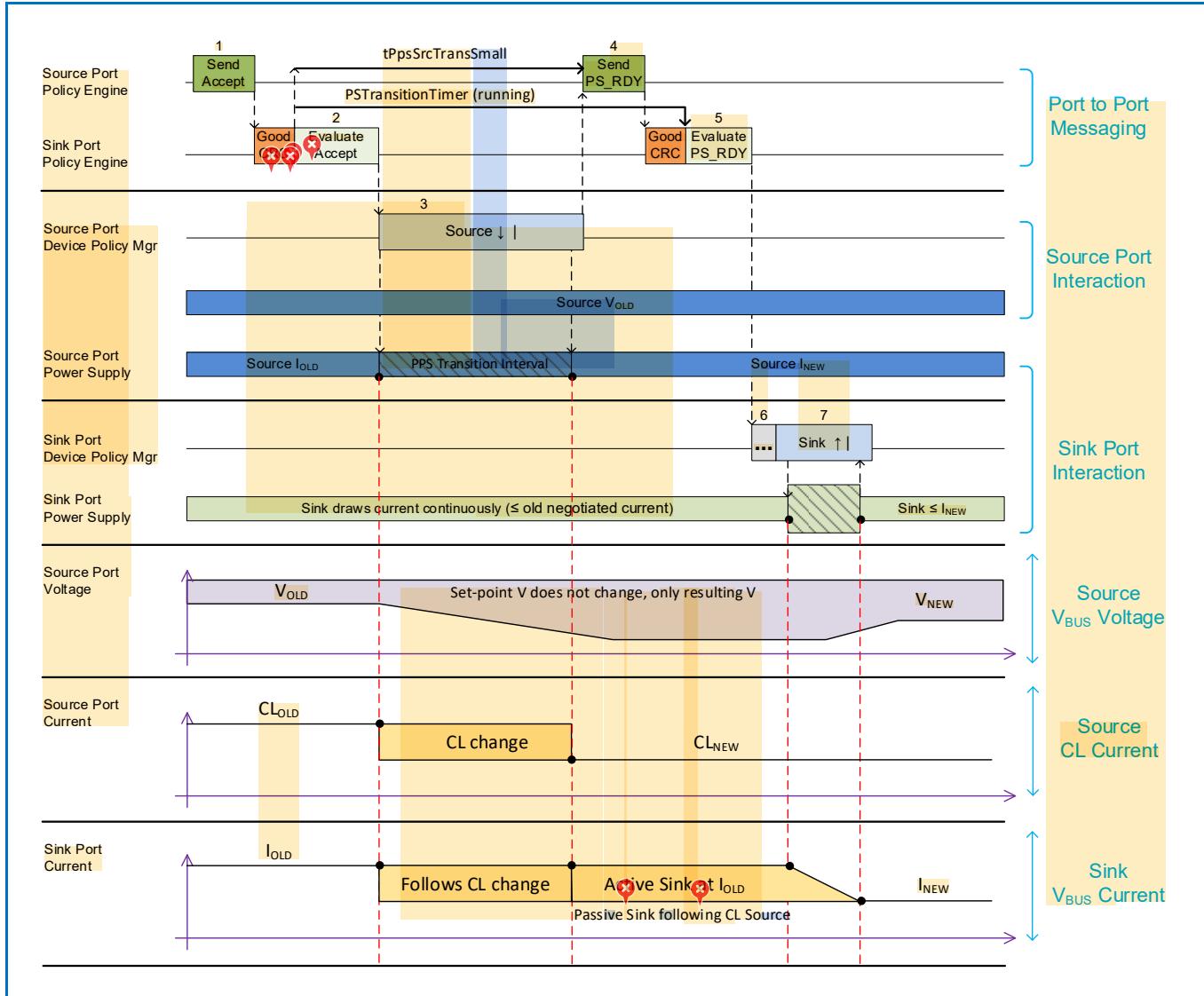


Table 7.14 “Sequence Description for decreasing the Current in PPS mode”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>Accept</i> Message to the Sink.	Policy Engine receives the <i>Accept</i> Message.
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to decrease its set-point for the current limit.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then evaluates the <i>Accept</i> Message and instructs the Sink to reduce its current to below the new negotiated current level and starts the <i>PSTransitionTimer</i> .
3	The Power Supply decreases its Current Limit set-point to the new negotiated value.	The Sink reduces its current to less than the new negotiated current to prevent the Source from going into Current Limit.
4	The Policy Engine sends the <i>PS_RDY</i> Message to the Sink starting within <i>tPpsSrcTransSmall</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> Message.	
5	Policy Engine receives the <i>GoodCRC</i> Message from the Sink.	Policy Engine receives the <i>PS_RDY</i> Message.
6		Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then stops the <i>PSTransitionTimer</i> and evaluates the <i>PS_RDY</i> Message. If the <i>PS_RDY</i> Message is not received before <i>PSTransitionTimer</i> times out the Sink sends <i>Hard Reset</i> signaling.
7		⚠️ The Sink is allowed to draw I_{NEW} but must be aware the Voltage on V_{BUS} can drop doing so.

7.3.1.3.5

Same Request Programmable Power Supply (PPS)

The interaction of the System Policy, Device Policy, and power supply that **Shall** be followed when the Sink requests the same Voltage and current levels as the present negotiated levels for Voltage and current is shown in [Figure 7-37 “Transition Diagram for no change in Current or Voltage in PPS mode”](#). The sequence that **Shall** be followed is described in [Table 7.15 “Sequence Description for no change in Current or Voltage in PPS mode”](#). The timing parameters that **Shall** be followed are listed in [Table 7.25 “Source Electrical Parameters”](#), [Table 7.26 “Sink Electrical Parameters”](#), and [Table 7.27 “Common Source/Sink Electrical Parameters”](#). Note in this figure, the Sink has previously sent a **Request** Message to the Source.

[Figure 7-37 “Transition Diagram for no change in Current or Voltage in PPS mode”](#)

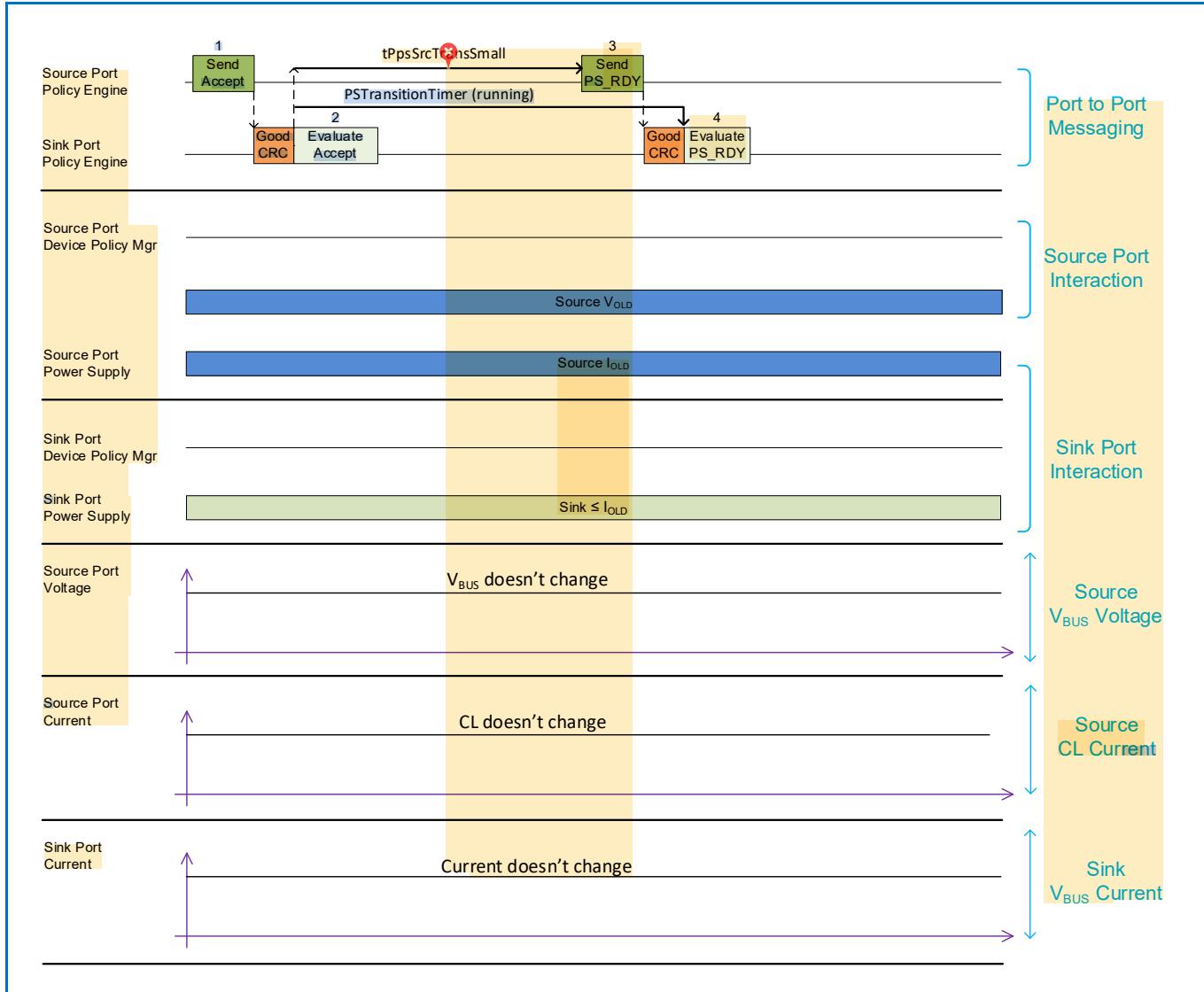


Table 7.15 “Sequence Description for no change in Current or Voltage in PPS mode”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>Accept</i> Message to the Sink.	Policy Engine receives the <i>Accept</i> Message.
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. 	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then evaluates the <i>Accept</i> Message and starts the <i>PSTransitionTimer</i> .
3	The Policy Engine then sends the <i>PS_RDY</i> Message to the Sink starting within <i>tPpsSrcTransSmall</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> Message. 	Policy Engine receives the <i>PS_RDY</i> Message.
4	 Policy Engine receives the <i>GoodCRC</i> Message from the Sink. Note: the decision that no power transition is required could be made either by the Device Policy Manager or the power supply depending on implementation.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then stops the <i>PSTransitionTimer</i> and evaluates the <i>PS_RDY</i> Message from the Source. The Sink is already operating at the new power level, so no further action is required. If the <i>PS_RDY</i> Message is not received before <i>PSTransitionTimer</i> times out the Sink sends <i>Hard Reset</i> signaling.

7.3.1.4 Changing Voltage or Current within the same AVS APDO

7.3.1.4.1 Increasing the Adjustable Voltage Supply (AVS) Voltage

The interaction of the System Policy, Device Policy, and power supply that **Shall** be followed when increasing the Voltage is shown in [Figure 7-38 "Transition Diagram for Increasing the Adjustable Power Supply Voltage"](#). The sequence that **Shall** be followed is described in [Table 7.16 "Sequence Description for Increasing the Adjustable Voltage Supply Voltage"](#). The timing parameters that **Shall** be followed are listed in [Table 7.25 "Source Electrical Parameters"](#), [Table 7.26 "Sink Electrical Parameters"](#), and [Table 7.27 "Common Source/Sink Electrical Parameters"](#). Note in this figure, the Sink has previously sent a **Request** Message to the Source.

Figure 7-38 "Transition Diagram for Increasing the Adjustable Power Supply Voltage"

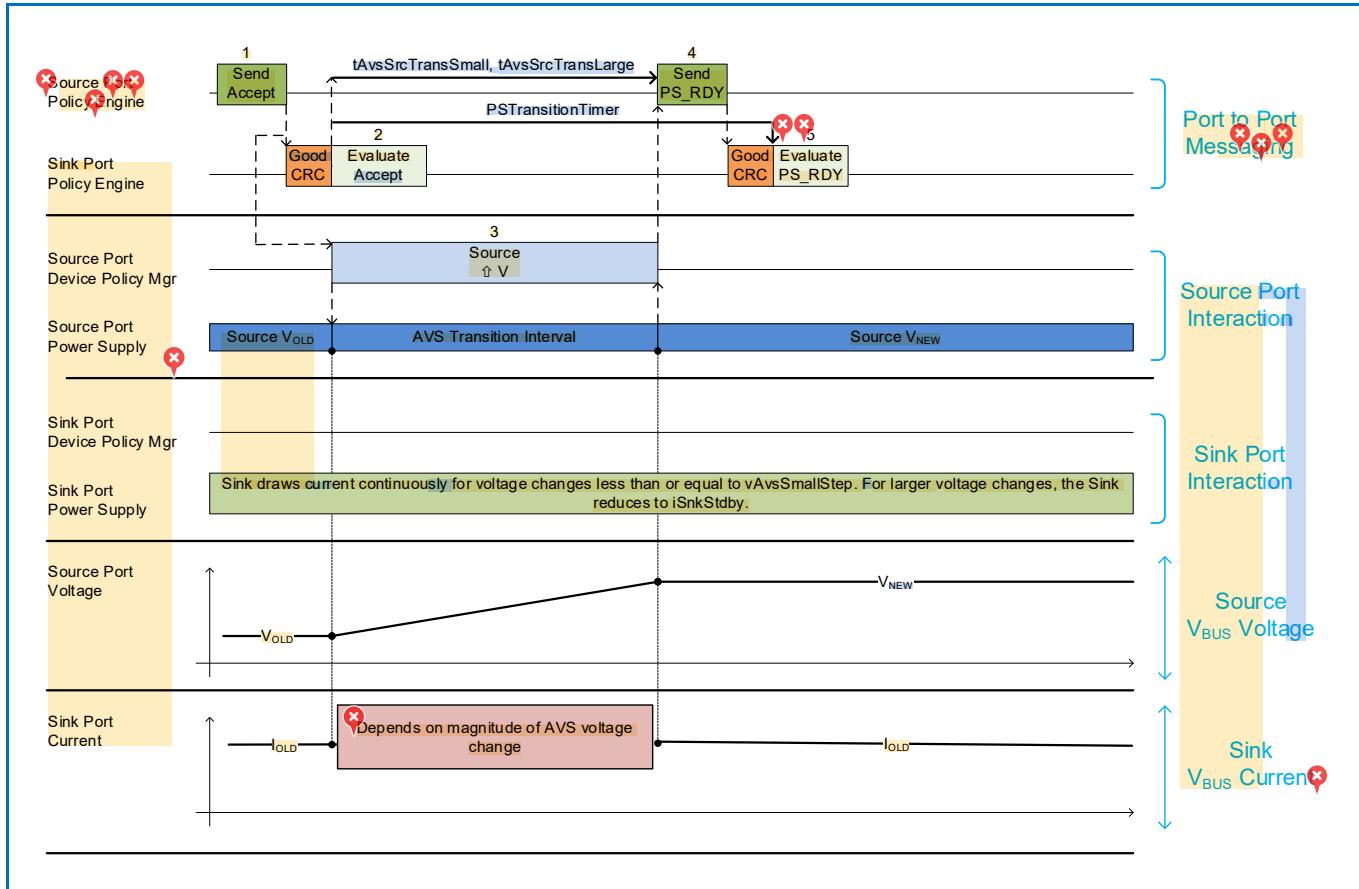


Table 7.16 “Sequence Description for Increasing the Adjustable Voltage Supply Voltage”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>Accept</i> Message to the Sink.	Policy Engine receives the <i>Accept</i> Message.
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to increase its output Voltage.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then starts the <i>PSTransitionTimer</i> and evaluates the <i>Accept</i> Message. If the Voltage increase is larger than <i>vAvsSmallStep</i> , the Sink Shall reduce its current draw to <i>iSnkStdby</i> within <i>tSnkStdby</i> . The reduction to <i>iSnkStdby</i> is not required if the Voltage increase is less than or equal to <i>vAvsSmallStep</i> .
3	After sending the <i>Accept</i> Message, the Adjustable Voltage Supply starts to increase its output Voltage. The Adjustable Voltage Supply new Voltage set-point Shall be reached by <i>tAvsSrcTransLarge</i> for steps larger than <i>vAvsSmallStep</i> or else by <i>tAvsSrcTransSmall</i> . The power supply informs the Device Policy Manager that it has reached the new level. The power supply status is passed to the Policy Engine.	
4	The Policy Engine sends the <i>PS_RDY</i> Message to the Sink starting within <i>tAvsSrcTransSmall</i> or <i>tAvsSrcTransLarge</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> Message.	The Policy Engine receives the <i>PS_RDY</i> Message from the Source.
5	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then stops the <i>PSTransitionTimer</i> , evaluates the <i>PS_RDY</i> Message from the Source and tells the Device Policy Manager that the Source is operating at the new Voltage set point. The Sink May begin operating at the new power level any time after evaluation of the <i>PS_RDY</i> Message. If the <i>PS_RDY</i> Message is not received before <i>PSTransitionTimer</i> times out the Sink ends <i>Hard Reset</i> signaling.

7.3.1.4.2

Decreasing the Adjustable Voltage Supply (AVS) Voltage

The interaction of the System Policy, Device Policy, and power supply that *Shall* be followed when decreasing the Voltage is shown in [Figure 7-39 “Transition Diagram for Decreasing the Adjustable Voltage Supply Voltage”](#). The sequence that *Shall* be followed is described in [Table 7.17 “Sequence Description for Decreasing the Adjustable Voltage Supply Voltage”](#). The timing parameters that *Shall* be followed are listed in [Table 7.25 “Source Electrical Parameters”](#), [Table 7.26 “Sink Electrical Parameters”](#), and [Table 7.27 “Common Source/Sink Electrical Parameters”](#). Note in this figure, the Sink has previously sent a **Request** Message to the Source.

 [Figure 7-39 “Transition Diagram for Decreasing the Adjustable Voltage Supply Voltage”](#)

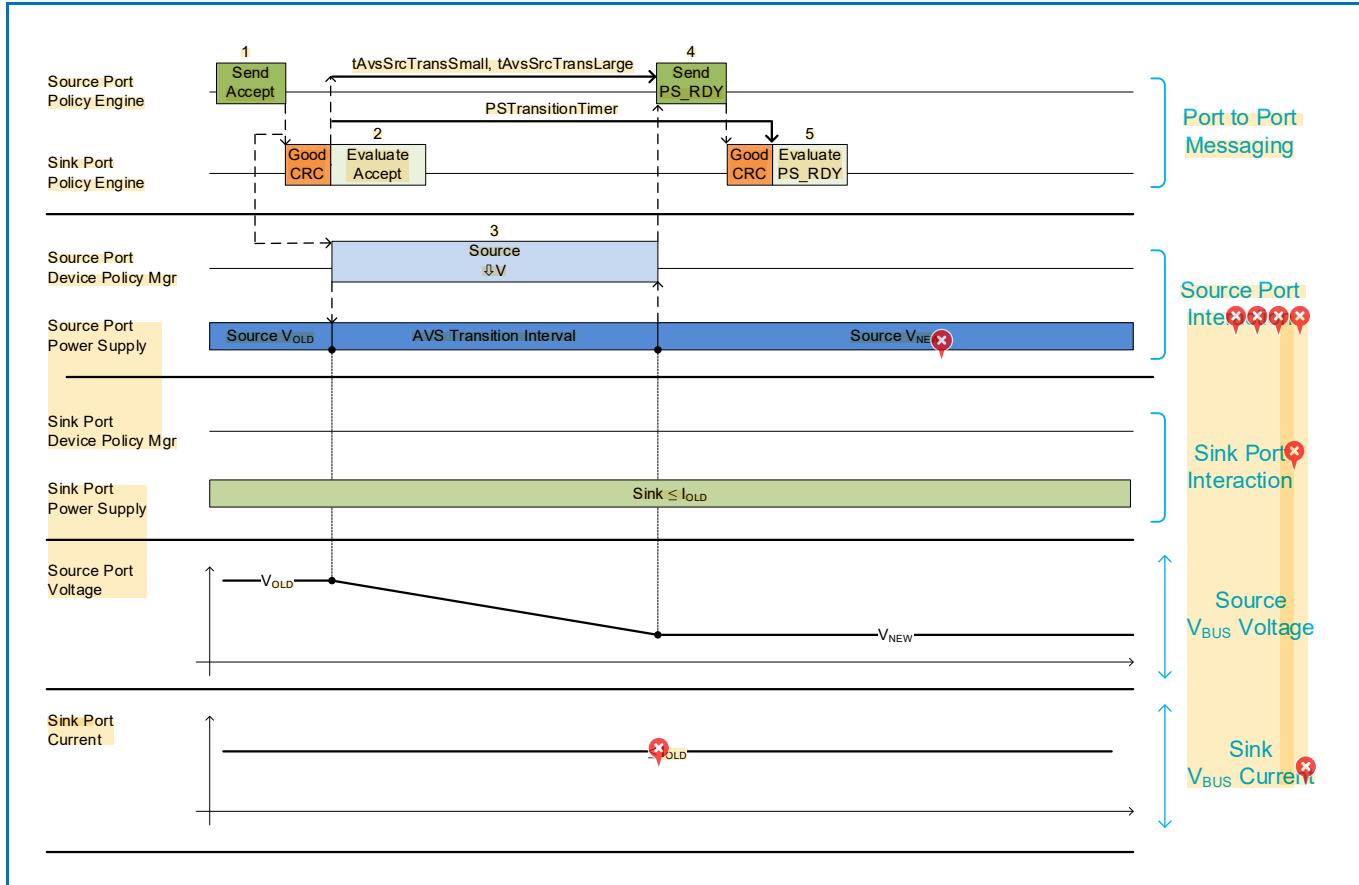


Table 7.17 “Sequence Description for Decreasing the Adjustable Voltage Supply Voltage”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>Accept</i> Message to the Sink.	Policy Engine receives the <i>Accept</i> Message.
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to decrease its output Voltage.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then starts the <i>PSTransitionTimer</i> and evaluates the <i>Accept</i> Message.
3	After sending the <i>Accept</i> Message, the Adjustable Voltage Supply starts to decrease its output Voltage. The Adjustable Voltage Supply new Voltage set-point <i>Shall</i> be reached by <i>tAvsSrcTransLarge</i> for steps larger than <i>vAvsSmallStep</i> or else by <i>tAvsSrcTransSmall</i> . The power supply informs the Device Policy Manager that it has reached the new level. The power supply status is passed to the Policy Engine.	
4	The Policy Engine sends the <i>PS_RDY</i> Message to the Sink starting within <i>tAvsSrcTransSmall</i> or <i>tAvsSrcTransLarge</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> Message.	The Policy Engine receives the <i>PS_RDY</i> Message from the Source.
5	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink.	Protocol Layer sends the GoodCRC Message to the Source. Policy Engine then stops the <i>PSTransitionTimer</i> , evaluates the <i>PS_RDY</i> Message from the Source and tells the Device Policy Manager that the Source is operating at the new Voltage set point (corresponding to <i>vAvsNew</i>). If the <i>PS_RDY</i> Message is not received before <i>PSTransitionTimer</i> times out the Sink sends <i>Hard Reset</i> signaling.

7.3.1.4.3 Same Request Adjustable Voltage Supply (AVS) Voltage

The interaction of the System Policy, Device Policy, and power supply that **Shall** be followed when the Sink requests the same Voltage and current levels as the present negotiated levels for Voltage and current as shown in [Figure 7-40 “Transition Diagram for no change in Current or Voltage in AVS mode”](#). The sequence that **Shall** be followed is described in [Table 7.18 “Sequence Description for no change in Current or Voltage in AVS mode”](#). The timing parameters that **Shall** be followed are listed in [Table 7.25 “Source Electrical Parameters”](#), [Table 7.26 “Sink Electrical Parameters”](#), and [Table 7.27 “Common Source/Sink Electrical Parameters”](#). Note in this figure, the Sink has previously sent a **Request** Message to the Source.

Figure 7-40 “Transition Diagram for no change in Current or Voltage in AVS mode”

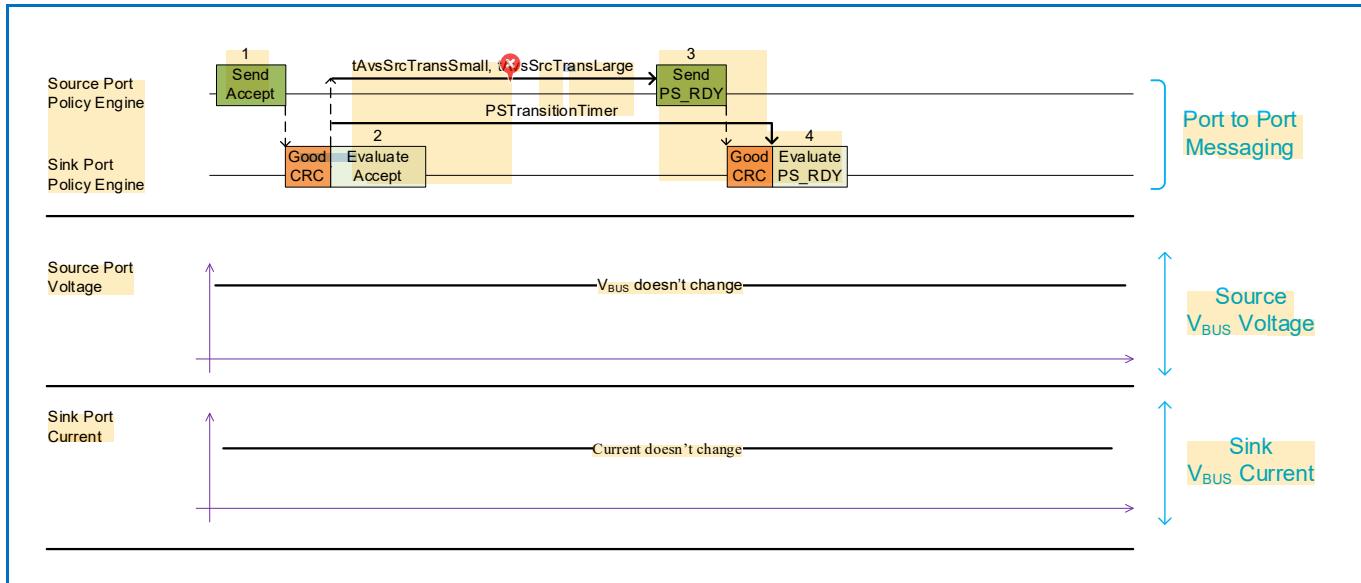


Table 7.18 “Sequence Description for no change in Current or Voltage in AVS mode”

Step	Source Port	Sink Port
1	Policy Engine sends the Accept Message to the Sink.	Policy Engine receives the Accept Message.
2	Protocol Layer receives the GoodCRC Message from the Sink.	Protocol Layer sends the GoodCRC Message to the Source. Policy Engine then starts the PSTransitionTimer and evaluates the Accept Message.
3	The Policy Engine sends the PS_RDY Message to the Sink starting within tAvsSrcTransSmall of the end of the GoodCRC Message following the Accept Message.	The Policy Engine receives the PS_RDY Message from the Source.
4	Protocol Layer receives the GoodCRC Message from the Sink. Note: the decision that no power transition is required could be made either by the Device Policy Manager or the power supply depending on implementation.	Protocol Layer sends the GoodCRC Message to the Source. Policy Engine then stops the PSTransitionTimer , evaluates the PS_RDY Message from the Source. The Sink is already operating at the new power level, so no further action is required. If the PS_RDY Message is not received before PSTransitionTimer times out the Sink sends Hard Reset signaling.

7.3.2 Transitions Caused by Power Role Swap

7.3.2.1 Sink Requested Power Role Swap

The interaction of the System Policy, Device Policy, and power supply that **Shall** be followed during a Sink requested Power Role Swap is shown in [Figure 7-41 “Transition Diagram for a Sink Requested Power Role Swap”](#). The sequence that **Shall** be followed is described in [Table 7.19 “Sequence Description for a Sink Requested Power Role Swap”](#). The timing parameters that **Shall** be followed are listed in [Table 7.25 “Source Electrical Parameters”](#), [Table 7.26 “Sink Electrical Parameters”](#), and [Table 7.27 “Common Source/Sink Electrical Parameters”](#). Note in this figure, the Sink has previously sent a [PR_Swap](#) Message to the Source.

Figure 7-41 “Transition Diagram for a Sink Requested Power Role Swap”

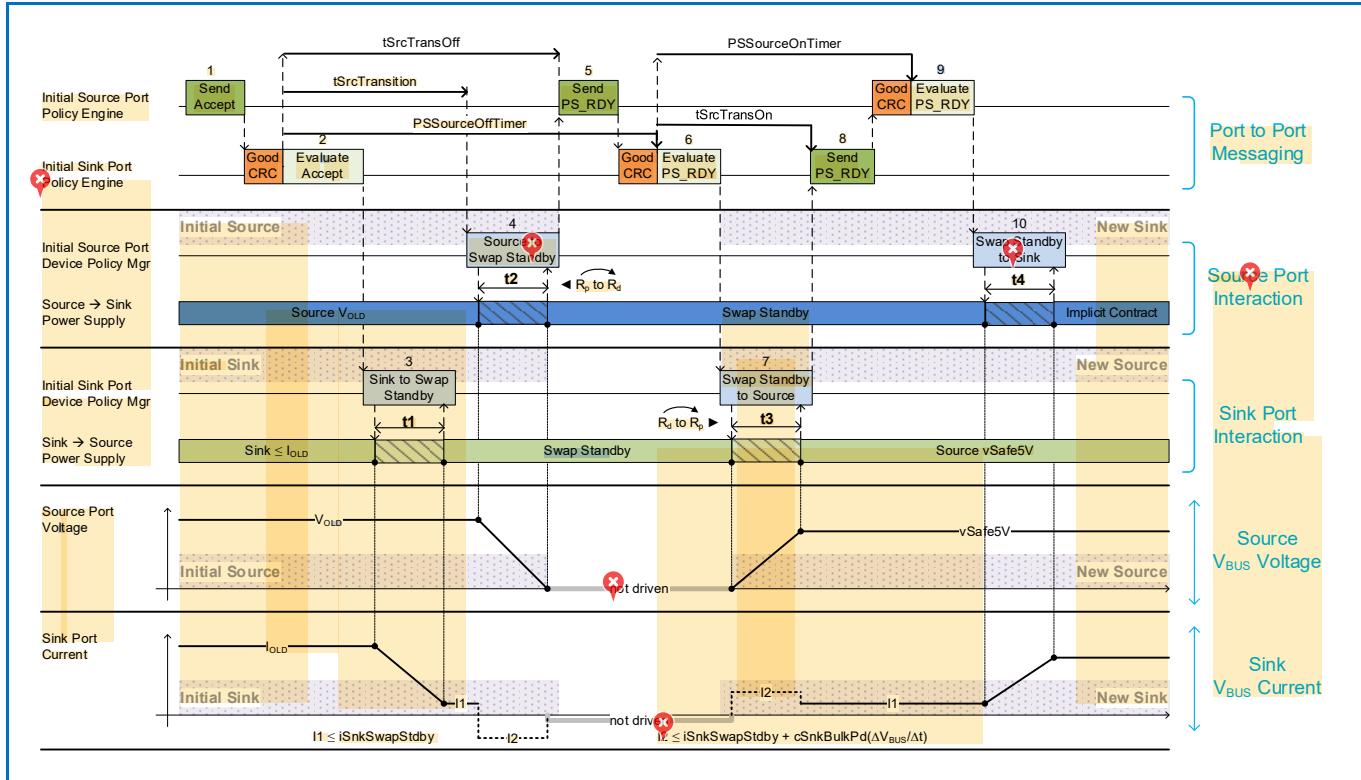


Table 7.19 “Sequence Description for a Sink Requested Power Role Swap”

Step	Initial Source Port → New Sink Port	Initial Sink Port → New Source Port
1	Policy Engine sends the <i>Accept</i> Message to the Initial Sink.	Policy Engine receives the <i>Accept</i> .
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to modify its output power.	Protocol Layer sends the <i>GoodCRC</i> Message to the Initial Source. Policy Engine then starts the <i>PSSourceOffTimer</i> and evaluates the <i>Accept</i> Message.
3		Policy Engine tells the Device Policy Manager to instruct the power supply to transition to Swap Standby within <i>tSinkStdby</i> (t1); t1 <i>Shall</i> complete before <i>tSrcTransition</i> min. When in Sink Standby the Initial Sink <i>Shall Not</i> draw more than <i>iSinkSwapStdby</i> (I1). The Sink <i>Shall Not</i> violate transient load behavior defined in <i>Section 7.2.6 “Transient Load Behavior”</i> while transitioning to and operating at the new power level.
4	<i>tSrcTransition</i> after the <i>GoodCRC</i> Message was received, the power supply starts to change its output power capability to Swap Standby (see <i>Section 7.1.10 “Swap Standby for Sources”</i>). The power supply <i>Shall</i> complete the transition to Swap Standby within <i>tSrcSwapStdby</i> (t2). The power supply informs the Device Policy Manager that it is ready to operate as the new Sink. The CC termination is changed from R _p to R _d (see <i>[USB Type-C 2.3]</i>). The power supply status is passed to the Policy Engine.	
5	The power supply is ready, and the Policy Engine sends the <i>PS_RDY</i> Message to the device that will become the new Source, starting within <i>tSrcTransOff</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> Message.	
6	Protocol Layer receives the <i>GoodCRC</i> Message from the device that will become the new Source. Policy Engine starts the <i>PSSourceOnTimer</i> . Upon sending the <i>PS_RDY</i> Message and receiving the <i>GoodCRC</i> Message the Initial Source is ready to be the new Sink.	The Protocol Layer sends the <i>GoodCRC</i> Message to the new Sink. Policy Engine the stops the <i>PSSourceOffTimer</i> and tells the Device Policy to instruct the power supply to operate as the new Source. If the <i>PS_RDY</i> Message is not received before <i>PSTransitionTimer</i> times out the Sink sends <i>Hard Reset</i> signaling.
7		The CC termination is changed from R _d to R _p (see <i>[USB Type-C 2.3]</i>). The power supply as the new Source transitions from Swap Standby to sourcing default <i>vSafe5V</i> within <i>tNewSrc</i> (t3). The power supply informs the Device Policy Manager that it is operating as the new Source.
8	Policy Engine receives the <i>PS_RDY</i> Message from the Source.	Device Policy Manager informs the Policy Engine the power supply is ready, and the Policy Engine sends the <i>PS_RDY</i> Message to the new Sink, starting within <i>tSrcTransOn</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> Message.

9	<p>Protocol Layer sends the <i>GoodCRC</i> Message to the new Source and then stops the <i>PSSourceOnTimer</i>... Policy Engine evaluates the <i>PS_RDY</i> Message from the new Source and tells the Device Policy Manager to instruct the power supply to draw current as the new Sink. </p>	<p>Protocol Layer receives the <i>GoodCRC</i> Message from the new Sink.</p>
10	<p>The power supply as the new Sink transitions from Swap Standby and begins to drawing the current allowed by the Implicit Contract. The power supply informs the Device Policy Manager that it is operating as the new Sink. At this point subsequent negotiations between the new Source and the new Sink <i>May</i> proceed as normal. The Sink <i>Shall Not</i> violate the transient load behavior defined in <i>Section 7.2.6 “Transient Load Behavior”</i> while transitioning to and operating at the new power level. The time duration (t4) depends on the magnitude of the load change (<i>iLoadStepRate</i>).</p>	

7.3.2.2 Source Requested Power Role Swap

The interaction of the System Policy, Device Policy, and power supply that **Shall** be followed during a Source requested Power Role Swap is shown in [Figure 7-42 “Transition Diagram for a Source Requested Power Role Swap”](#). The sequence that **Shall** be followed is described in [Table 7.20 “Sequence Description for a Source Requested Power Role Swap”](#). The timing parameters that **Shall** be followed are listed in [Table 7.25 “Source Electrical Parameters”, Table 7.26 “Sink Electrical Parameters”, and Table 7.27 “Common Source/Sink Electrical Parameters”](#). Note in this figure, the Source has previously sent a **PR_Swap** Message to the Sink.

[Figure 7-42 “Transition Diagram for a Source Requested Power Role Swap”](#)

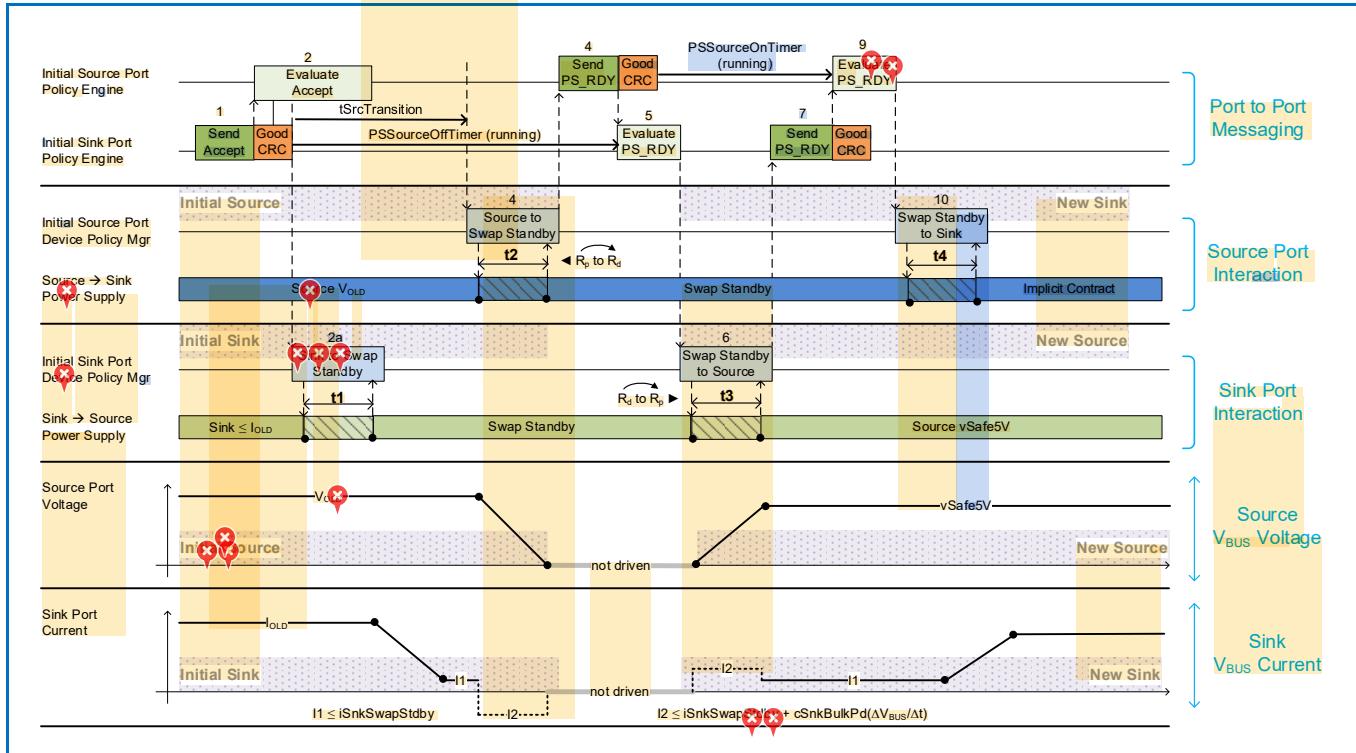


Table 7.20 “Sequence Description for a Source Requested Power Role Swap”

Step	Initial Source Port → New Sink Port	Initial Sink Port → New Source Port
1	Policy Engine receives the <i>Accept</i> Message.	Policy Engine sends the <i>Accept</i> Message to the Initial Source.
2	Protocol Layer sends the <i>GoodCRC</i> Message to the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to modify its output power.	Protocol Layer receives the <i>GoodCRC</i> Message from the Initial Source. Policy Engine starts the <i>PSSourceOffTimer</i> .
2a		The Policy Engine tells the Device Policy Manager to instruct the power supply to transition to Swap Standby. The power supply Shall complete the transition to Swap Standby within <i>tSinkStdby</i> (t1); t1 Shall complete before <i>tSrcTransition</i> . The Sink Shall Not violate the transient load behavior defined in Section 7.2.6 “Transient Load Behavior” while transitioning to and operating at the new power level. When in Sink Standby the Initial Sink Shall Not draw more than <i>iSinkSwapStdby</i> (11).
3	<i>tSrcTransition</i> after the <i>GoodCRC</i> Message was sent the power supply starts to change its output power capability to Swap Standby (see Section 7.1.10 “Swap Standby for Sources”). The power supply Shall complete the transition to Swap Standby within <i>tSrcSwapStdby</i> (t2). The power supply informs the Device Policy Manager that it is ready to operate as the new Sink. The CC termination is changed from R_p to R_d (see [USB Type-C 2.3]). The power supply status is passed to the Policy Engine.	
4	The Policy Engine sends the <i>PS_RDY</i> Message to the device that will become the new Source, starting within <i>tSrcTransOff</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> Message.	Policy Engine receives the <i>PS_RDY</i> .
5	Protocol Layer receives the <i>GoodCRC</i> Message from the soon to be new Source. Policy Engine starts the <i>PSSourceOnTimer</i> . At this point the Initial Source is ready to be the new Sink.	Protocol Layer sends the <i>GoodCRC</i> Message to the new Sink. Policy Engine then stops the <i>PSSourceOffTimer</i> and tells the Device Policy to instruct the power supply to operate as the new Source. If the <i>PS_RDY</i> Message is not received before the <i>PSSourceOffTimer</i> times out the Sink starts sending Hard Reset Signaling .
6		The CC termination is changed from R_d to R_p (see [USB Type-C 2.3]). The power supply as the new Source transitions from Swap Standby to sourcing default <i>vSafe5V</i> within <i>tNewSrc</i> (t3). The power supply informs the Device Policy Manager that it is operating as the new Source.
7	Policy Engine receives the <i>PS_RDY</i> Message.	Device Policy Manager informs the Policy Engine the power supply is ready, and the Policy Engine sends the <i>PS_RDY</i> Message to the new Sink, starting within <i>tSrcTransOn</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> Message.
8	Protocol Layer sends the <i>GoodCRC</i> Message to the new Source and then stops the <i>PSSourceOnTimer</i> . Policy Engine evaluates the <i>PS_RDY</i> Message from the new Source and tells the Device Policy Manager to instruct the power supply to draw current as the new Sink.	Protocol Layer receives the <i>GoodCRC</i> Message from the new Sink.

9	<p>The power supply as the new Sink transitions from SwapStandby to drawing the power allowed by the Implicit Contract. The power supply informs the Device Policy Manager that it is operating as the new Sink. At this point subsequent negotiations between the new Source and the new Sink <i>May</i> proceed as normal. The new Sink <i>Shall Not</i> violate the transient load behavior defined in Section 7.2.6 “Transient Load Behavior” while transitioning to and operating at the new power level. The time duration (t4) depends on the magnitude of the load change (<i>iLoadStepRate</i>).</p>	
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7.3.3 Transitions Caused by GotoMin

7.3.3.1 GotoMin Current Decrease

The interaction of the System Policy, Device Policy, and power supply that **Shall** be followed during a GotoMin current decrease is shown in [Figure 7-43 “Transition Diagram for a GotoMin Current Decrease”](#). The sequence that **Shall** be followed is described in [Table 7.21 “Sequence Description for a GotoMin Current Decrease”](#). The timing parameters that **Shall** be followed are listed in [Table 7.25 “Source Electrical Parameters”](#), [Table 7.26 “Sink Electrical Parameters”](#), and [Table 7.27 “Common Source/Sink Electrical Parameters”](#).

[Figure 7-43 “Transition Diagram for a GotoMin Current Decrease”](#)

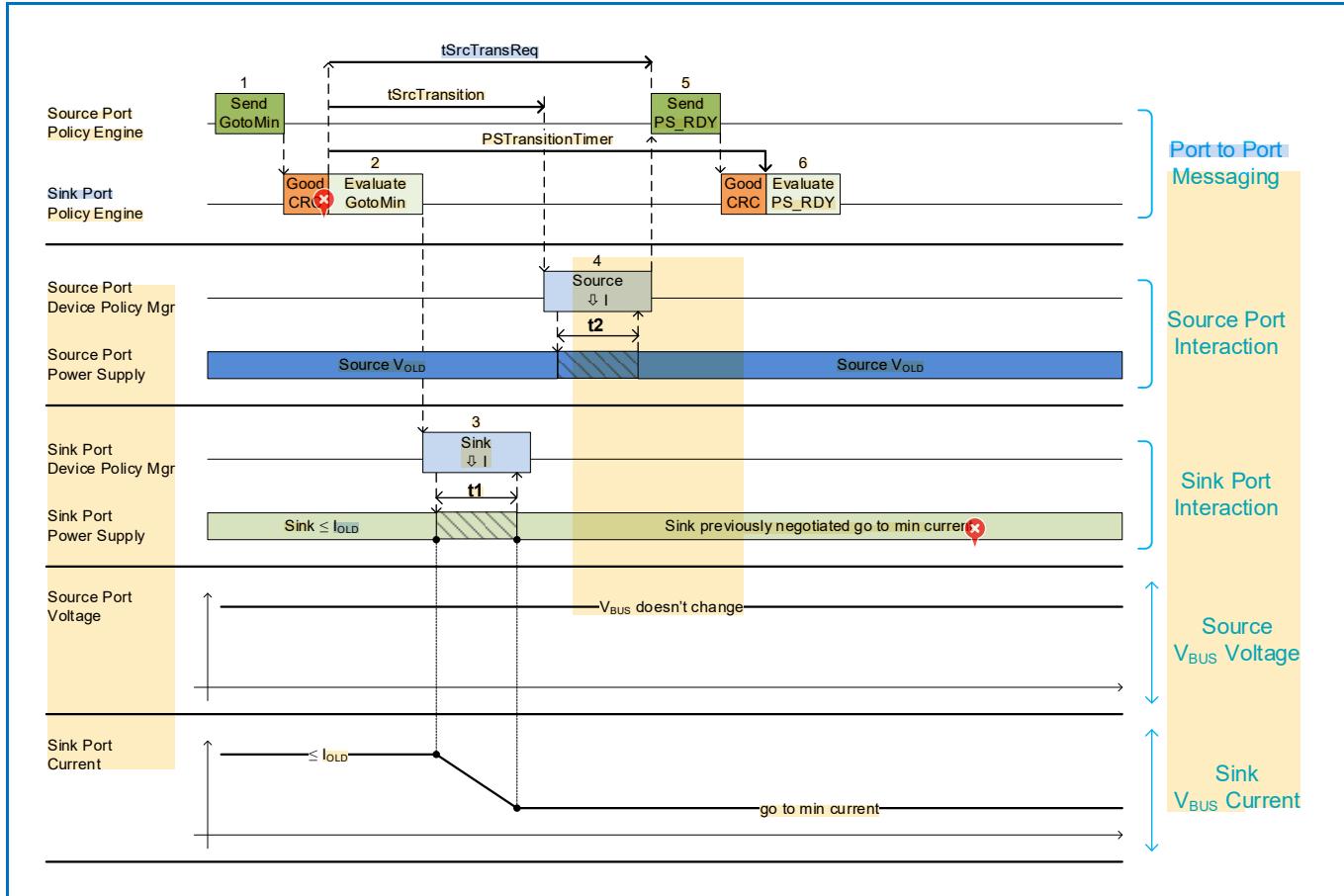


Table 7.21 “Sequence Description for a GotoMin Current Decrease”

Step	Source Port	Sink Port
1	Policy Engine sends the <i>GotoMin</i> Message to the Sink.	Policy Engine receives the <i>GotoMin</i> Message.
2	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink. The Policy Engine tells the Device Policy Manager to instruct the power supply to modify its output power.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then starts the <i>PSTransitionTimer</i> and evaluates the <i>GotoMin</i> Message.
3		Policy Engine tells the Device Policy Manager to instruct the power supply to reduce power consumption, within <i>tSnkNewPower</i> (t1), to the pre-negotiated go to reduced power level; t1 <i>Shall</i> complete before <i>tSrcTransition</i> min. The Sink <i>Shall Not</i> violate the transient load behavior defined in Section 7.2.6 “Transient Load Behavior” while transitioning to and operating at the new power level.
4	<i>tSrcTransition</i> after the <i>GoodCRC</i> Message was received the power supply starts to change its output power capability. The power supply <i>Shall</i> be ready to operate at the new power level within <i>tSrcReady</i> (t2). The power supply informs the Device Policy Manager that it is ready to operate at the new power level. The power supply status is passed to the Policy Engine.	
5	The Policy Engine sends the <i>PS_RDY</i> Message to the Sink starting within <i>tSrcTransReq</i> of the end of the <i>GoodCRC</i> Message following the <i>Accept</i> message.	The Policy Engine receives the <i>PS_RDY</i> Message.
6	Protocol Layer receives the <i>GoodCRC</i> Message from the Sink.	Protocol Layer sends the <i>GoodCRC</i> Message to the Source. Policy Engine then stops the <i>PSTransitionTimer</i> and evaluates the <i>PS_RDY</i> Message from the Source and no further action is required. If the <i>PS_RDY</i> Message is not received before <i>PSTransitionTimer</i> times out the Sink sends <i>Hard Reset</i> signaling.

7.3.4 Transitions Caused by Hard Reset

7.3.4.1 Source Initiated Hard Reset

The interaction of the System Policy, Device Policy, and power supply that **Shall** be followed during a Source Initiated Hard Reset is shown in [Figure 7-44 “Transition Diagram for a Source Initiated Hard Reset”](#). The sequence that **Shall** be followed is described in [Table 7.22 “Sequence Description for a Source Initiated Hard Reset”](#). The timing parameters that **Shall** be applied are listed in [Table 7.25 “Source Electrical Parameters”](#), [Table 7.26 “Sink Electrical Parameters”](#), and [Table 7.27 “Common Source/Sink Electrical Parameters”](#).

[Figure 7-44 “Transition Diagram for a Source Initiated Hard Reset”](#)

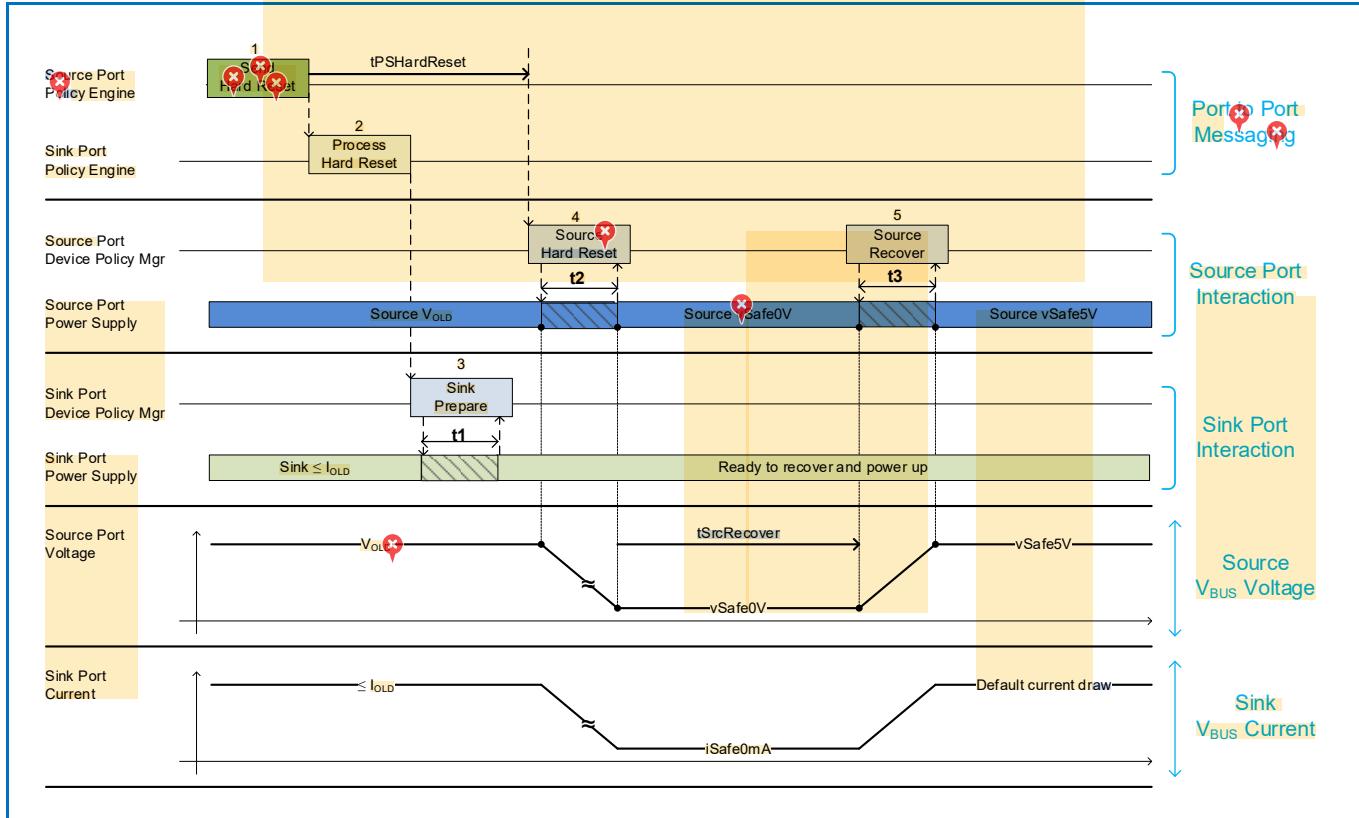


Table 7.22 “Sequence Description for a Source Initiated Hard Reset”

Step	Source Port	Sink Port
1	Policy Engine sends Hard Reset Signaling to the Sink.	Sink receives Hard Reset Signaling.
2		Policy Engine is informed of the Hard Reset. Policy Engine tells the Device Policy Manager to instruct the power supply to prepare for a Hard Reset.
3		The Sink prepares for the Hard Reset within tSnkHardResetPrepare (t1) and passes an indication to the Device Policy Manager. The Sink Shall Not draw more than iSafe0mA when V_{BUS} is driven to vSafe0V .
4	Policy Engine waits tPSHardReset after sending Hard Reset Signaling and then tells the Device Policy Manager to instruct the power supply to perform a Hard Reset. The transition to vSafe0V Shall occur within tSafe0V (t2).	
5	After tSrcRecover the Source applies power to V_{BUS} in an attempt to re-establish communication with the Sink and resume USB Default Operation. The transition to vSafe5V Shall occur within tSrcTurnOn (t3).	The Sink Shall Not violate the transient load behavior defined in Section 7.2.6 “Transient Load Behavior” while transitioning to and operating at the new power level.

7.3.4.2 Sink Initiated Hard Reset

The interaction of the System Policy, Device Policy, and power supply that **Shall** be followed during a Sink Initiated Hard Reset is shown in [Figure 7-45 “Transition Diagram for a Sink Initiated Hard Reset”](#). The sequence that **Shall** be followed is described in [Table 7.23 “Sequence Description for a Sink Initiated Hard Reset”](#). The timing parameters that **Shall** be followed are listed in [Table 7.25 “Source Electrical Parameters”](#), [Table 7.26 “Sink Electrical Parameters”](#), and [Table 7.27 “Common Source/Sink Electrical Parameters”](#).

[Figure 7-45 “Transition Diagram for a Sink Initiated Hard Reset”](#)

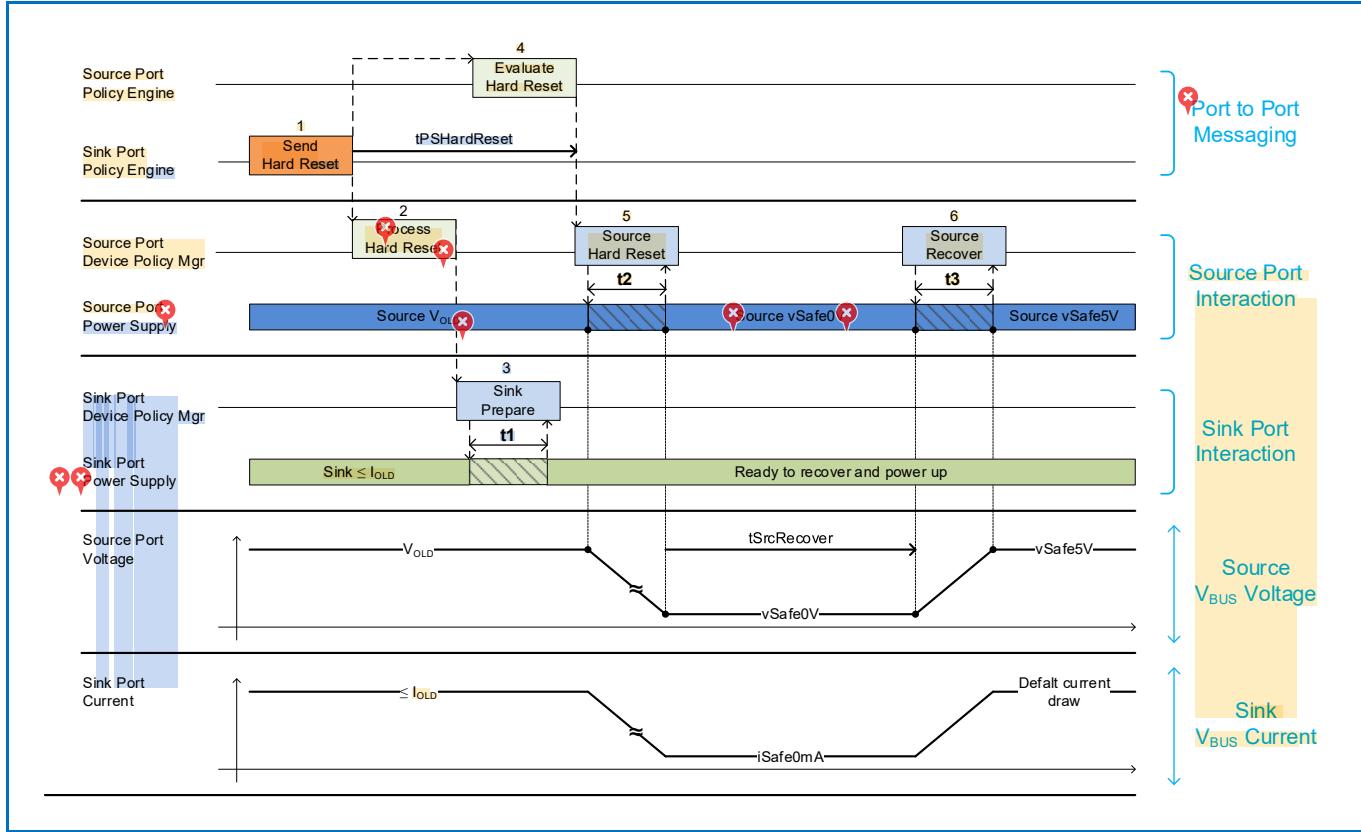


Table 7.23 “Sequence Description for a Sink Initiated Hard Reset”

Step	Source Port	Sink Port
1		Policy Engine sends Hard Reset Signaling to the Source.
2		Policy Engine tells the Device Policy Manager to instruct the power supply to prepare for a Hard Reset.
3		The Sink prepares for the Hard Reset within tSinkHardResetPrepare (t1) and passes an indication to the Device Policy Manager. The Sink Shall Not draw more than iSafe0mA when V_{BUS} is driven to vSafe0V .
4	Policy Engine is informed of the Hard Reset.	
5	Policy Engine waits tPSHardReset after receiving Hard Reset Signaling and then tells the Device Policy Manager to instruct the power supply to perform a Hard Reset. The transition to vSafe0V Shall occur within tSafe0V (t2).	
6	After tSrcRecover the Source applies power to V_{BUS} in an attempt to re-establish communication with the Sink and resume USB Default Operation. The transition to vSafe5V Shall occur within tSrcTurnOn (t3).	The Sink Shall Not violate the transient load behavior defined in Section 7.2.6 “Transient Load Behavior” while transitioning to and operating at the new power level.

7.3.5 Transitions Caused by Fast Role Swap

7.3.5.1 Fast Role Swap

The interaction of the System Policy, Device Policy, and power supply that *Shall* be followed during a Fast Role Swap is shown in [Figure 7-46 “Transition Diagram for Fast Role Swap”](#). The parallel sequences that *Shall* be followed are described in [Table 7.24 “Sequence Description for Fast Role Swap”](#). The timing parameters that *Shall* be followed are listed in [Table 7.25 “Source Electrical Parameters”](#), [Table 7.26 “Sink Electrical Parameters”](#), and [Table 7.27 “Common Source/Sink Electrical Parameters”](#). Negotiations between the new Source and the new Sink *May* occur after the new Source sends the final **PS_RDY** Message.

Note: in [Figure 7-46 “Transition Diagram for Fast Role Swap”](#). and [Table 7.24 “Sequence Description for Fast Role Swap”](#) numbers are used to indicate Message related steps and letters are used to indicate other events.

Figure 7-46 “Transition Diagram for Fast Role Swap”

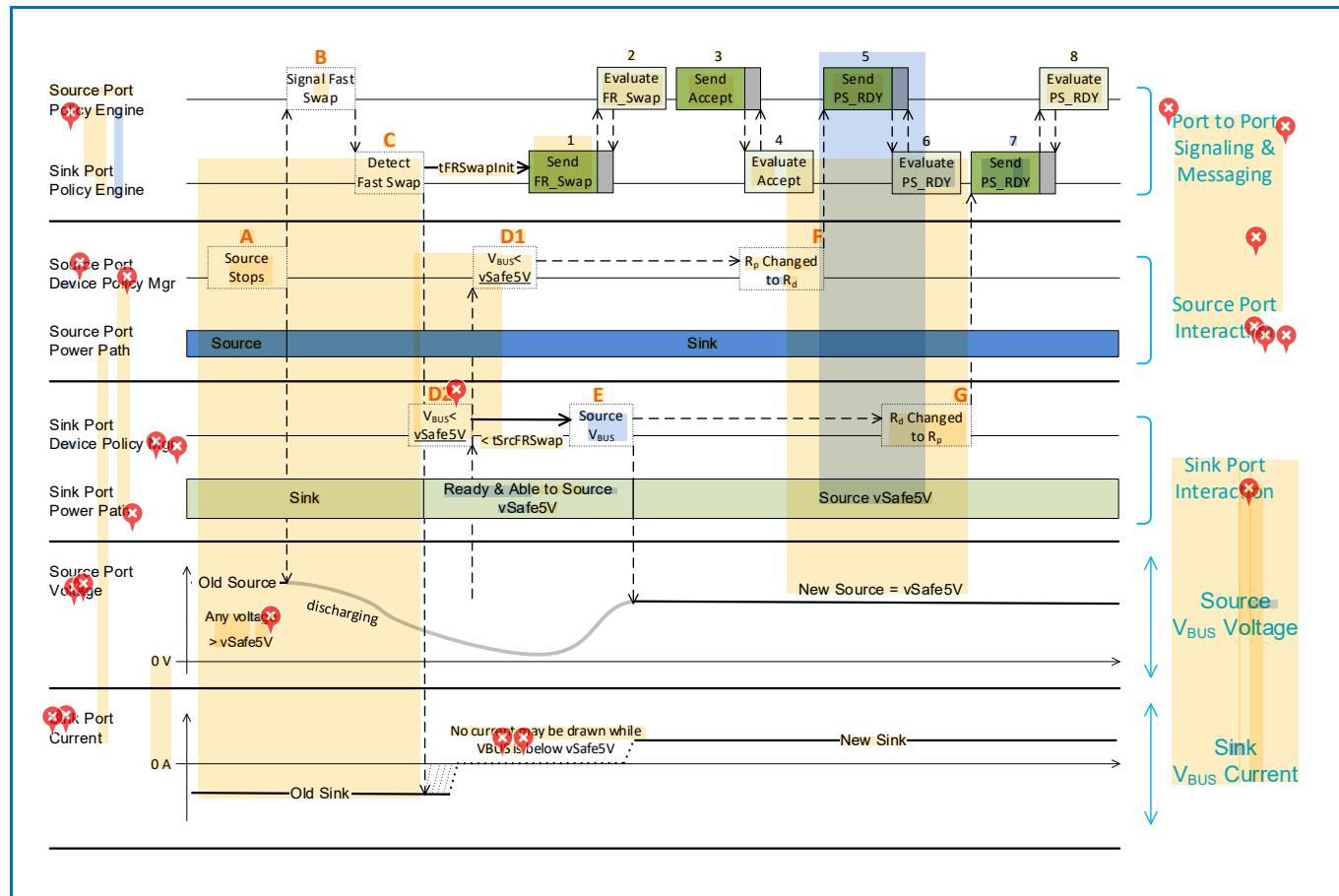


Table 7.24 “Sequence Description for Fast Role Swap

Step	Initial Source Port → New Sink Port	Initial Sink Port → New Source Port
Fast Role Swap Signaling and Power Transition		
A	The Source connected to the Hub UFP (see Figure 7-17 “VBUS Power during Fast Role Swap”) stops sourcing V _{BUS} .	
B	Policy Engine signals the Fast Role Swap to the initial Sink on the CC wire. When V _{BUS} < <i>vSafe5V</i> (min), it tells the Device Policy Manager not to draw more than <i>iSnkStdby</i> until the <i>tSnkFRSwap</i> timer has elapsed.	
C		Policy Engine detects the Fast Role swap signal on the CC wire from the initial Source and <i>Shall</i> send the <i>FR_Swap</i> Message back to the initial Source (that is no longer powering V _{BUS}) within time <i>tFRSwapInit</i> .
D1	The Policy engine monitors for V _{BUS} ≤ <i>vSafe5V</i> so that a <i>PS_RDY</i> Message can be sent to the new Source at Step 5 of the messaging sequence.	
D2		The Policy engine monitors for V _{BUS} ≤ <i>vSafe5V</i> so the initial Sink can assume the role of new Source and begin to source V _{BUS} .
E		When V _{BUS} = <i>vSafe5V</i> the new Source <i>May</i> provide power to V _{BUS} . When V _{BUS} < <i>vSafe5V</i> the new Source <i>Shall</i> provide power to V _{BUS} within <i>tSrcFRSwap</i> . Once the new Source is providing power, the <i>PS_RDY</i> Message can be sent to the new Sink at Step 7 of the messaging sequence.
F	The CC termination is changed from R _p to R _d (see [USB Type-C 2.3]) before the new Sink sends the <i>PS_RDY</i> Message at Step 5 to the new Source.	
G		The CC termination is changed from R _d to R _p (see [USB Type-C 2.3]) before the new Source sends the <i>PS_RDY</i> Message at Step 7 to the new Sink.
Fast Role Swap Message Sequence		
1	Policy Engine receives the <i>FR_Swap</i> Message from the initial Sink that is transitioning to be the new Source.	Policy Engine sends the <i>FR_Swap</i> Message to the initial Source (that is no longer powering V _{BUS}) after detecting the Fast Role Swap signal at Step C.
2	Protocol Layer sends the <i>GoodCRC</i> Message to the initial Sink. Policy Engine then evaluates the <i>FR_Swap</i> Message.	Protocol Layer receives the <i>GoodCRC</i> Message from the initial Source.
3	Policy Engine sends an <i>Accept</i> Message to the initial Sink that is transitioning to be the new Source.	Policy Engine receives the <i>Accept</i> Message from the initial Source that is transitioning to be the new Sink.
4	Protocol Layer receives the <i>GoodCRC</i> Message from the initial Sink that is transitioning to be the new Source.	Protocol Layer sends the <i>GoodCRC</i> Message to the initial Source that is transitioning to be the new Sink.

5	Policy Engine sends a <i>PS_RDY</i> Message to the initial Sink that is transitioning to be the new Source. The Policy Engine <i>Shall</i> start the <i>PS_RDY</i> Message at least <i>tFRSwap5V</i> after it has sent the <i>Accept</i> Message, and when Step D1 has also been completed. 	Policy Engine receives the <i>PS_RDY</i> Message from the new Sink.
6	Protocol Layer receives the <i>GoodCRC</i> Message from the new Source. 	Protocol Layer sends the <i>GoodCRC</i> Message from the initial Sink that has completed the transition to new Source. Policy Engine then evaluates the <i>PS_RDY</i> Message.
7	Policy Engine receives the <i>PS_RDY</i> Message from the new Source. 	Policy Engine sends a <i>PS_RDY</i> Message to the new Sink. The Policy Engine <i>Shall</i> wait for Step E before sending the <i>PS_RDY</i> Message, and <i>Shall</i> send the <i>PS_RDY</i> Message within <i>tFRSwapComplete</i> of receiving the <i>PS_RDY</i> Message from the Initial Source Port.

7.4 Electrical Parameters

7.4.1 Source Electrical Parameters

The Source Electrical Parameters that *Shall* be followed are specified in [Table 7.25 "Source Electrical Parameters"](#).

Table 7.25 "Source Electrical Parameters"

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
<i>cSrcBulk</i> ¹	Source bulk capacitance when a Port is powered from a dedicated supply.	10			µF	Section 7.1.2
<i>cSrcBulkShared</i> ¹	Source bulk capacitance when a Port is powered from a shared supply.	120			µF	Section 7.1.2
<i>DNL</i> ² (Differential Non-Linearity)	Deviation between ideal analog values corresponding to adjacent input digital values.	-1	0	+1	LSB	Section 7.1.4.2.1
<i>iPpsCLMin</i>	SPR PPS Minimum Current Limit setting.	1			A	Section 7.1.4.2.2
<i>iPpsCLNew</i>	Current Limit accuracy					Section 7.1.4.2.2
	1A ≤ Operating Current ≤ 3A	-150		150	mA	
	Operating current > 3A	-5		5	%	
<i>iPpsCLStep</i>	SPR PPS Current Limit programming step size (1 LSB).		50		mA	Section 7.1.4.2.2
<i>iPpsCLLoadReleaseRate</i> ³	Maximum load decrease slew rate during Current Limit setpoint changes.	-150			mA/µs	Section 7.1.4.2.2
<i>iPpsCLLoadStepRate</i>	Maximum load increase slew rate during Current Limit setpoint changes.			150	mA/µs	Section 7.1.4.2.2
<i>iPpsCLTransient</i>	Allowed output current overshoot when a load increase occurs while in CL mode.			New load + 100	mA	Section 7.1.4.2.2
	Allowed output current undershoot when a load decrease occurs while in CL mode.	New load - 100			mA	

<i>tPpsCVCLTransient</i>	CV to CL transient current bounds assuming the Operating Voltage reduction of Section 7.2.3.1 "Programmable Power Supply Sink Standby".	<i>iPpsCLNe</i> <i>w</i> - 100		New load + 500	mA	Section 7.1.4.2.2
<i>tAvsTransient</i>	The maximum time for the Adjustable Voltage Supply to be between <i>vAvsNew</i> and <i>vAvsValid</i> in response to a load transient. *			5	ms	Section 7.1.8.2
<i>tAvsSrcTransLarge</i>	The time the Adjustable Voltage Supply set-point <i>Shall</i> transition between requested Voltages for steps larger than <i>vAvsSmallStep</i> .	0		700	ms	Section 7.1.4.3.1
<i>tAvsSrcTransSmall</i>	The time the Adjustable Voltage Supply set-point <i>Shall</i> transition between requested Voltages for steps smaller than <i>vAvsSmallStep</i> . *	0		50	ms	Section 7.1.4.3.1
<i>tNewSnk</i>	Time allowed for an initial Source in Swap Standby to transition new Sink operation.			15	ms	Section 7.1.10 Figure 7-41 Figure 7-42
<i>tPpsCLCVTransient</i> *	CL to CV transient. * Voltage settling time.			275	ms	Section 7.1.4.2.2
<i>tPpsCLProgramSettle</i>	* SPR PPS Current Limit programming settling time.			250	ms	Section 7.1.4.2.2
<i>tPpsCLSettle</i>	* CL load transient current settling time.			250	ms	Section 7.1.4.2.2
<i>tPpsCVCLTransient</i>	* CV to CL transient settling time.			250	ms	Section 7.1.8.1
<i>tPpsSrcTransLarge</i>	The time the Programmable Power Supply's set-point <i>Shall</i> transition between requested Voltages for steps larger than <i>vPpsSmallStep</i> .	0		275	ms *	Section 7.3.16 Section 7.3.17

<i>tPpsSrcTransSmall</i>	The time the Programmable Power Supply's set-point <i>Shall</i> transition between requested Voltages for steps less than or equal to <i>vPpsSmallStep</i> .	0		25	ms	Section 7.3.16 Section 7.3.17
<i>tPpsTransient</i>	The maximum time for the Programmable Power Supply to be between <i>vPpsNew</i> and <i>vPpsValid</i> in response to a load transient when target load is greater than or equal to 60mA.		5		ms	Section 7.1.8.1
	The maximum time for the Programmable Power Supply to be between <i>vPpsNew</i> and <i>vPpsValid</i> in response to a load transient when target load is less than 60mA.		150		ms	Section 7.1.8.1
<i>tSrcFRSwap</i>	Time from the initial Sink detecting that V_{BUS} has dropped below <i>vSafe5V</i> until the initial Sink/new Source is able to supply USB Type-C® Current (see [USB Type-C 2.3])		150		μs	Section 7.1.13
<i>tSrcReady</i>	SPR Mode	Time from positive/negative transition start (t_0) to when the Source is ready to provide the newly negotiated power level. Applies only to SPR mode voltage transitions.		285	ms	Figure 7-2 Figure 7-3
	EPR Mode	Time from positive/negative transition start (t_0) to when the Source is ready to provide the newly negotiated power level. Applies to EPR mode voltage transitions and any voltage transition that either begins or ends in EPR mode.		720		

<i>tSrcRecover</i>	SPR Mode	Time allotted for the Source to recover.	0.66		1.0	s	Section 7.1.5
	EPR Mode		1.085		1.425		
<i>tSrcSettle</i>	SPR Mode	Time from positive/negative transition start (t_0) to when the transitioning Voltage is within the range v_{SrcNew} . Applies only to SPR mode voltage transitions.			275	ms	Figure 7-2
	✖️ EPR Mode	Time from positive/negative transition start (t_0) to when the transitioning Voltage is within the range v_{AvsNew} . Applies to EPR mode voltage transitions and any voltage transition that either begins or ends in EPR mode.			700		
<i>tSrcSwapStdby</i>	The maximum time for the Source to transition to Swap Standby.				650	ms	Section 7.1.10 Table 7.19 Table 7.20
<i>tSrcTransient</i>	The maximum time for the Source output Voltage to be between v_{SrcNew} and $v_{SrcValid}$ in response to a load transient when target load is greater or equal to than 60mA.				5	ms	Section 7.1.8
	The maximum time for the Source output Voltage to be between v_{SrcNew} and $v_{SrcValid}$ in response to a load transient when target load is less than 60mA.				150	ms	Section 7.1.8
<i>tSrcTransition</i>	The time the Source <i>Shall</i> wait before transitioning the power supply to ensure that the Sink has sufficient time to prepare (does not apply to transitions within the same PPS or AVS APDO).	25			35	ms	Section 7.3

<i>tSrcTransOff</i>	SPR Mode  	Time from the last bit of the <i>GoodCRC</i> Message acknowledging the <i>Accept</i> Message in response to the <i>PR_Swap</i> Message until the <i>PS_RDY</i> Message must be started. Applies only to SPR mode voltage transitions.		690	ms	<i>Section 7.3.2</i>
<i>tSrcTransOn</i>		Time from the last bit of the <i>GoodCRC</i> Message acknowledging the <i>PS_RDY</i> Message sent by the new Source, in response to the <i>PR_Swap</i> Message until the <i>PS_RDY</i> Message must be started.		280	ms	 <i>Section 7.3.2</i>
<i>tSrcTransReq</i>	SPR Mode	Time from the last bit of the <i>GoodCRC</i> Message acknowledging the <i>Accept</i> Message in response to the Request Message until the <i>PS_RDY</i> Message must be started. Applies only to SPR mode voltage transitions.		325	ms	<i>Section 7.3</i>
	   EPR Mode	Time from the last bit of the <i>GoodCRC</i> Message acknowledging the <i>Accept</i> Message in response to the Request Message until the <i>PS_RDY</i> Message must be started. Applies to EPR mode voltage transitions and any voltage transition that either begins or ends in EPR mode.		760	ms	<i>Section 7.3</i>
<i>tSrcTurnOn</i>		Transition time from <i>vSafe0V</i> to <i>vSafe5V</i> .		275	ms	<i>Figure 7-13</i> <i>Table 7.22</i> <i>Table 7.23</i>

vAvsMaxVoltage	Maximum Voltage Field in the Adjustable Voltage Supply APDO.	APDO Max Voltage *0.95	✖	APDO Max Voltage *1.05	V	Section 7.1.4.3.1
vAvsMinVoltage	Minimum Voltage Field in the Adjustable Voltage Supply APDO.	APDO Min Voltage *0.95	✖	APDO Min Voltage *1.05	V	Section 7.1.4.3.1
vAvsNew	Adjustable RDO Output Voltage measured at the Source receptacle.	RDO Output Voltage *0.95	✖	RDO Output Voltage *1.05	V	Section 7.1.8.2
vAvsSlewNeg	Adjustable Voltage Supply maximum slew rate for negative Voltage changes.			-30	mV/μs	Section 7.1.8.2
vAvsSlewPos	Adjustable Voltage Supply maximum slew rate for positive Voltage changes.			30	mV/μs	Section 7.1.8.2
vAvsSmallStep	Adjustable Voltage Supply step size defined as a small step relative to the previous vAvsNew .	✖-1.0		1.0	V	Section 7.1.4.3.1
vAvsStep	Adjustable Voltage Supply Voltage programming step size.		100		mV	Section 7.1.8.2
vAvsValid	The range in addition to vAvsNew which the Adjustable Voltage Supply output is considered Valid during and after a transition as well as in response to a transient load condition.	✖-0.5		0.5	V	Section 7.1.8.2
vPpsCLCVTransient	CL to CV load transient Voltage bounds.	Operating Voltage * 0.95 – 0.1V		✖Operating Voltage * 1.05 + 0.1V	✖V	Section 7.1.4.2.2
vPpsMaxVoltage	Maximum Voltage Field in the Programmable Power Supply APDO.	APDO Max Voltage *0.95		APDO Max Voltage *1.05	V	Section 7.1.4.2.1

vPpsMinVoltage	Minimum Voltage Field in the Programmable Power Supply APDO	APDO Min Voltage *0.95		APDO Min Voltage * 1.05	V	Section 7.1.4.2.1
vPpsNew	Programmable RDO Output Voltage measured at the Source receptacle.	RDO Output Voltage *0.95	RDO Output Voltage	RDO Output Voltage *1.05	V	Section 7.1.8.1
vPpsShutdown	The Voltage at which the SPR PPS shuts down when operating in CL.	APDO Minimum Voltage * 0.85		APDO Minimum Voltage *	V	Section 7.1.4.2.2
vPpsSlewNeg	Programmable Power Supply maximum slew rate for negative Voltage changes			-30	mV/μs	Section 7.1.8.1
vPpsSlewPos	Programmable Power Supply maximum slew rate for positive Voltage changes			30	mV/μs	Section 7.1.8.1
vPpsSmallStep	PPS Step size defined as a small step relative to the previous vPpsNew .	-500		500	mV	Section 7.1.4.2.1
vPpsStep	PPS Voltage programming step size (1 LSB).		20		mV	Section 7.1.8.1
vPpsValid	The range in addition to vPpsNew which the Programmable Power Supply output is considered valid in response to a load step.	-0.1		0.1	V	Section 7.1.8.1
vSmallStep	VBUS step size increase defined as a small step relative to the previous VBUS when Requesting a different (A)PDO.			500	mV	Section 7.1.4.3.1
vSrcNeg	Most negative Voltage allowed during transition.			-0.3	V	Figure 7-13
vSrcNew	Fixed Supply output measured at the Source receptacle.	PDO Voltage *0.95	PDO Voltage	PDO Voltage *1.05	V	Figure 7-2 Figure 7-3
	Variable Supply output measured at the Source receptacle.	PDO Minimum Voltage		PDO Maximum Voltage	V	

	Battery Supply output measured at the Source receptacle.	PDO Minimum Voltage		PDO Maximum Voltage	V	
vSrcPeak	The range that a Fixed Supply or EPR AVS in Peak Current operation is allowed when overload conditions occur.  	PDO Voltage *0.90		PDO Voltage *1.05	V	 Table 6-10 Table 6-15 Figure 7-15
vSrcSlewNeg	Maximum slew rate allowed for negative Voltage transitions. Limits current based on a 3 A connector rating and maximum Sink bulk capacitance of 100 μ F.		-30	mV/ μ s		Section 7.1.4.2 Figure 7-3
vSrcSlewP  	Maximum slew rate allowed for positive Voltage transitions. Limits current based on a 3 A connector rating and maximum Sink bulk capacitance of 100 μ F. 		30	mV/ μ s		Section 7.1.4 Figure 7-2
vSrcValid	The range in addition to vSrcNew which a newly negotiated Voltage is considered Valid during and after a transition as well as in response to a transient load condition. This range also applies to vSafe    	-0.5	0.5	V	  Figure 7-2 Figure 7-3 Section 7.1.8	

- 1) The Source **Shall** charge and discharge the total bulk capacitance to meet the transition time requirements.

7.4.2 Sink Electrical Parameters

The Sink Electrical Parameters that *Shall* be followed are specified in [Table 7.26 “Sink Electrical Parameters”](#).

Table 7.26 “Sink Electrical Parameters”

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
<i>cSnkBulk¹</i>	Sink bulk capacitance on V _{BUS} at Attach and during FRS after the old Source stops sourcing and prior to establishing an Explicit Contract (see Appendix E “FRS System Level Example” for an example).			See [USB 3.2]		Section 7.2.2 [USB 3.2]
<i>cSnkBulkPd¹</i>	Bulk capacitance on V _{BUS} a Sink is allowed after a successful negotiation. ²			100	μF	Section 7.2.2
<i>iLoadReleaseRate²</i>	Load release di/dt.	-150			mA/μs	Section 7.2.6
<i>iLoadStepRate²</i>	Load step di/dt.			150	mA/μs	Section 7.2.6
<i>iNewFrsSink</i>	Maximum current the new Sink can draw during a Fast Role Swap until the new Source applies R _p . Matches the required USB Type-C® Current field of the Fixed Supply PDO of the old Source’s <i>Sink Capabilities</i> Message.			Default USB current or 1.5 or 3.0	A	Section 7.1.13
<i>iOvershoot</i>	Positive or negative overshoot when a load change occurs less than or equal to <i>iLoadStepRate</i> ; relative to the settled value after the load change.	-230		230	mA	Section 7.2.6
<i>iPpsCLLoadStep²</i>	Maximum Current setpoint change while operating in CL mode.	-500		500	mA	Section 7.2.3.1
<i>iSafe0mA²</i>	Maximum current a Sink is allowed to draw when V _{BUS} is driven to <i>vSafe0V</i> .			1.0	mA	Figure 7-31 Figure 7-32
<i>iSnkStd^{2,3}</i>	Maximum current during voltage transition.			500	mA	Section 7.2.3
<i>iSnkSwapStdby</i>	Maximum current a Sink can draw during Swap Standby. Ideally this current is very near to 0 mA largely influenced by Port leakage current.			2.5	mA	Section 7.2.7
<i>pHubSusp</i>	Suspend power consumption for a hub. 25mW + 25mW per downstream Port for up to 4 ports. ²			125	mW	Section 7.2.3

pSnkSusp	Suspend power consumption for a peripheral device.			25	mW	Section 7.2.3
tNewSrc	Maximum time allowed for an initial Sink in Swap Standby to transition to new Source operation.		275	ms	Section 7.2.7 Table 7.19 Table 7.20	
tSnkFRSwap	Time during a Fast Role Swap when the new Sink can draw no more than <i>iSnkStdby</i> .		200	μs	Section 7.1.13	
tSnkHardResetPrepare	Time allotted for the Sink power electronics to prepare for a Hard Reset.		15	ms	Table 7-13	
tSnkNewPower	Maximum transition time between power levels.		15	ms	Section 7.2.3	
tSnkRecover	Time for the Sink to resume USB Default Operation.		150	ms	Table 7.22	
tSnkStdby	Time to transition to Sink Standby from Sink.		15	ms	Section 7.2.3	
tSnkSwapStdby	Maximum time for the Sink to transition to Swap Standby.		15	ms	Section 7.2.7	
vEprMax	Highest Voltage an EPR Sink expected to tolerate		55	V	Section 7.2.9.2	
vSprMax	Highest Voltage an SPR Sink expected to tolerate		24	V	Section 7.2.9.2	

1) If more bypass capacitance than *cSnkBulk* max or *cSnkBulkPd* max is required in the device, then the device *Shall* incorporate some form of V_{BUS} surge current limiting as described in [USB 3.2] Section 11.4.4.1.

7.4.3 Common Electrical Parameters

Electrical Parameters that are common to both the Source and the Sink that *Shall* be followed are specified in [Table 7.27 “Common Source/Sink Electrical Parameters”](#).

Table 7.27 “Common Source/Sink Electrical Parameters”

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
$tSafe0V$	Time to reach $vSafe0V$ max.			650	ms	Section 7.1.5 Figure 7-13 Table 7.22 Table 7.23
$tSafe5V$	Time to reach $vSafe5V$ max.			275	ms	Section 7.1.5 Figure 7-13 Table 7.22 Table 7.23
$tVconnReapplied$	When the UFP is the VCONN source: time from the last bit of the <i>GoodCRC</i> acknowledging the <i>PS_RDY</i> Message before reapplying VCONN. When the DFP is the VCONN source: time from when VCONN drops below vRaReconnect.	10		20	ms	Figure 7-20 Figure 7-21
$tVconnValid$	Time from $tVconnReapplied$ until VCONN is within vVconnValid (see [USB Type-C 2.3]).	0		5	ms	Figure 7-20 Figure 7-21
$tVconnZero$	Time from the last bit of the <i>GoodCRC</i> acknowledging the <i>Accept</i> Message in response to the <i>Data_Reset</i> Message until VCONN is below vRaReconnect (see [USB Type-C 2.3]).			125	ms	Figure 7-20 Figure 7-21
$vSafe0V$	Safe operating Voltage at “zero volts”.	0		0.8	V	Section 7.1.5
$vSafe5V$	Safe operating Voltage at 5V. See [USB 2.0] and [USB 3.2] for allowable V _{BUS} Voltage range.	4.75		5.5	V	Section 7.1.5
① \diamond VconnStable (See [USB Type-C 2.3]) still applies.						