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EG1163 Chip User Manual

High voltage and high current step-down switching power supply chip

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Version Change History

Version Numbe	Date Description	
V1.0	May 15, 2018 EG1163 Datasheet Draft	

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Table of contents

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EG1163 chip data sheet V1.0

1. Features

ÿ Synchronous freewheeling solution, supports high voltage and high current solution. ÿ An external capacitor can set the operating frequency (0-300KHz) ÿ UVLO undervoltage lockout function: ÿ Vcc pin turn-on voltage 16.5V-EG1163 ÿ Vcc pin turn-off voltage 8V-EG1163 ÿ Vcc pin turn-on voltage 8.5V-EG1163S ÿ Vcc pin turn-off voltage 7.5V-EG1163S ÿ MOS tube internal resistance cycle by cycle current limiting control ÿ Support battery charging ÿ Output short circuit protection ÿ Package: SOP16

2. Description

EG1163 is a high-voltage, high-current step-down DC-DC power management chip. It integrates reference power supply, oscillator, error amplifier, current limiting protection, short-circuit protection, half-bridge drive and other functions. It is very suitable for high-voltage and high-current applications. It can support up to 600V power supply voltage input with external high-voltage MOS tube.

3. Application areas

ÿ Electric motorcycle converter ÿ Electric bicycle converter ÿ High voltage analog/ digital system ÿ Industrial control system ÿ Telecom power system ÿ Ethernet POE ÿ Portable mobile device ÿ Inverter system

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4. Pins

4.1 Pin Definition

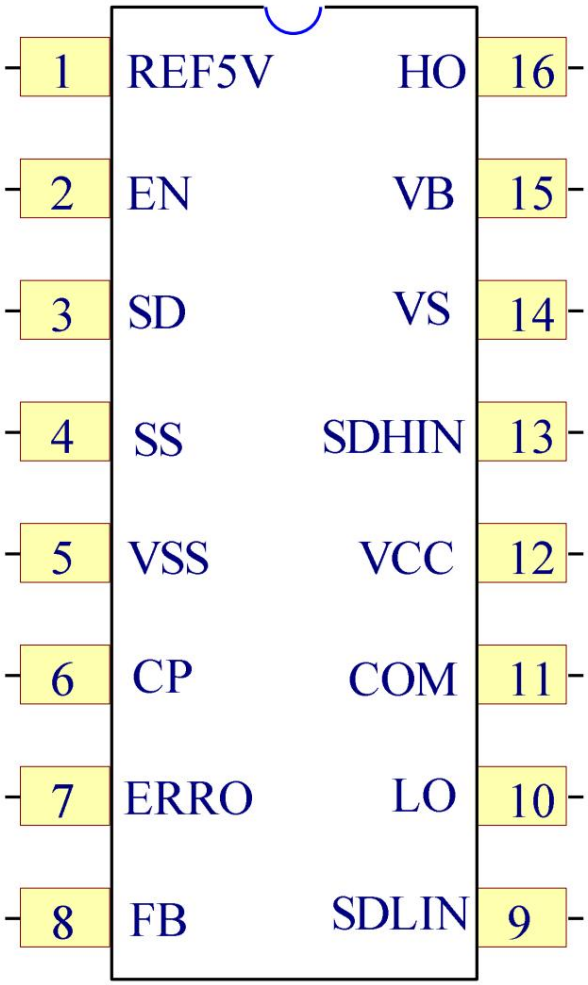

Figure 4-1. EG1163 pin definition

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4.2 Pin Description

Pin No.	Pin Name	I/O	describe
1	REF5V	O	5V reference output, drive current 50mA.
2	IN	I	Chip enable pin, comparison threshold 1.2V; below 1.2V, the chip enters standby mode and turns off 5V Output.
3	SD	I	High level turns off PWM output, low level enables PWM output.
4	SS	I	Soft start pin, external capacitor, capacitor voltage rise speed affects the soft start time.
5	VSS		AGND Chip signal ground.
6	CP	I	External capacitor, frequency f=(14.4 x106)/Cp (in pF).
7	ERROR	O	Voltage loop op amp output port.
8	FB	I	Voltage loop op amp negative input port.
9	SDLIN	I	Low-side MOS tube current comparator input port.
10	IT	O	output controls the conduction and cutoff of the low-end MOS power tube.
11	WITH		PGND Chip power ground.
12	VCC		Power chip power supply, voltage range 10V-20V.
13	SDHIN	I	High-side MOS tube current comparator input port.
14	VS	O	High-end floating ground terminal.
15	VB		Power High-end floating power supply.
16	TO	O	output controls the on and off of the high-side MOS power tube.

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5. Structure diagram

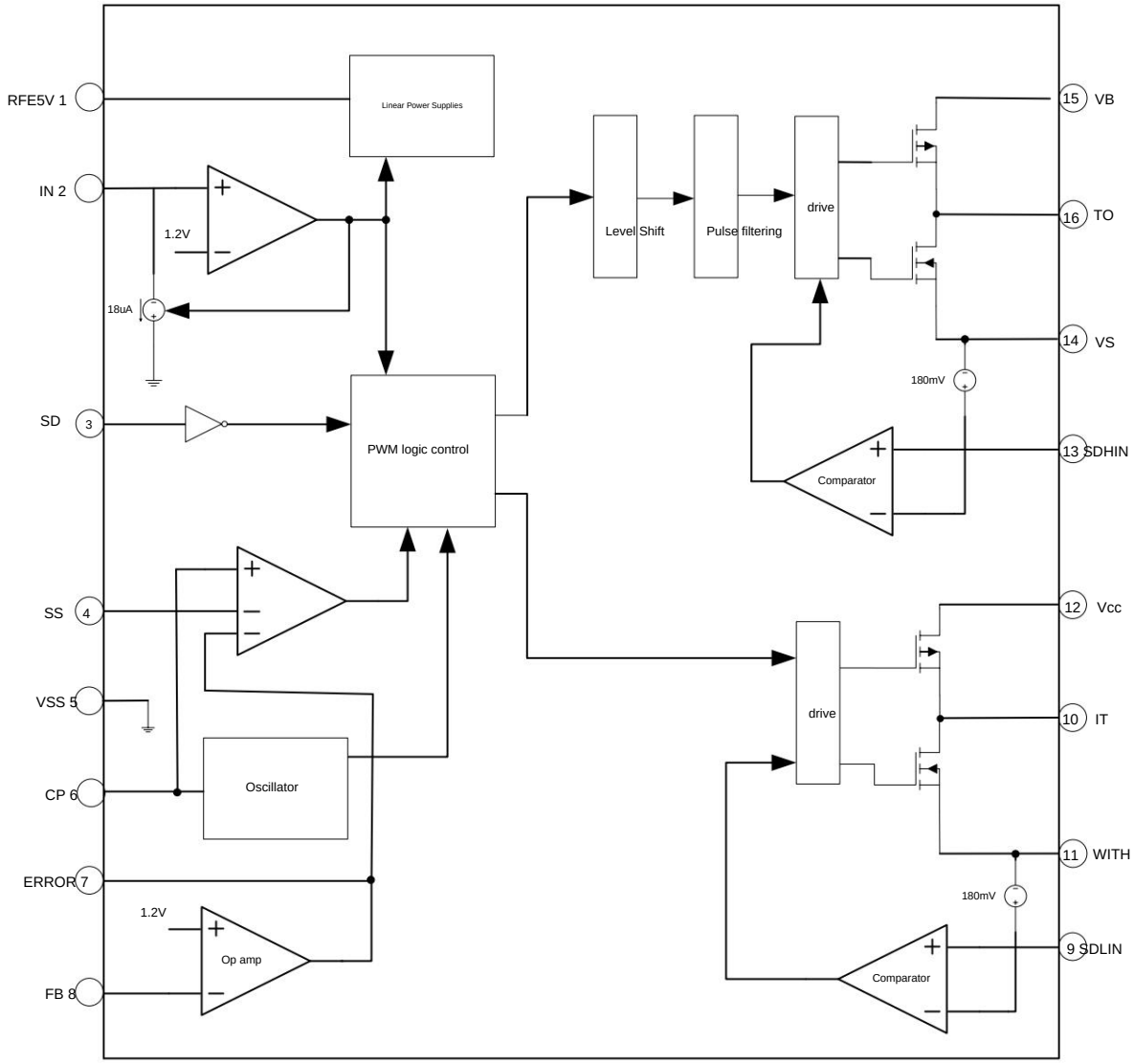

Figure 5-1. EG1163 block diagram

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6. Typical application circuit

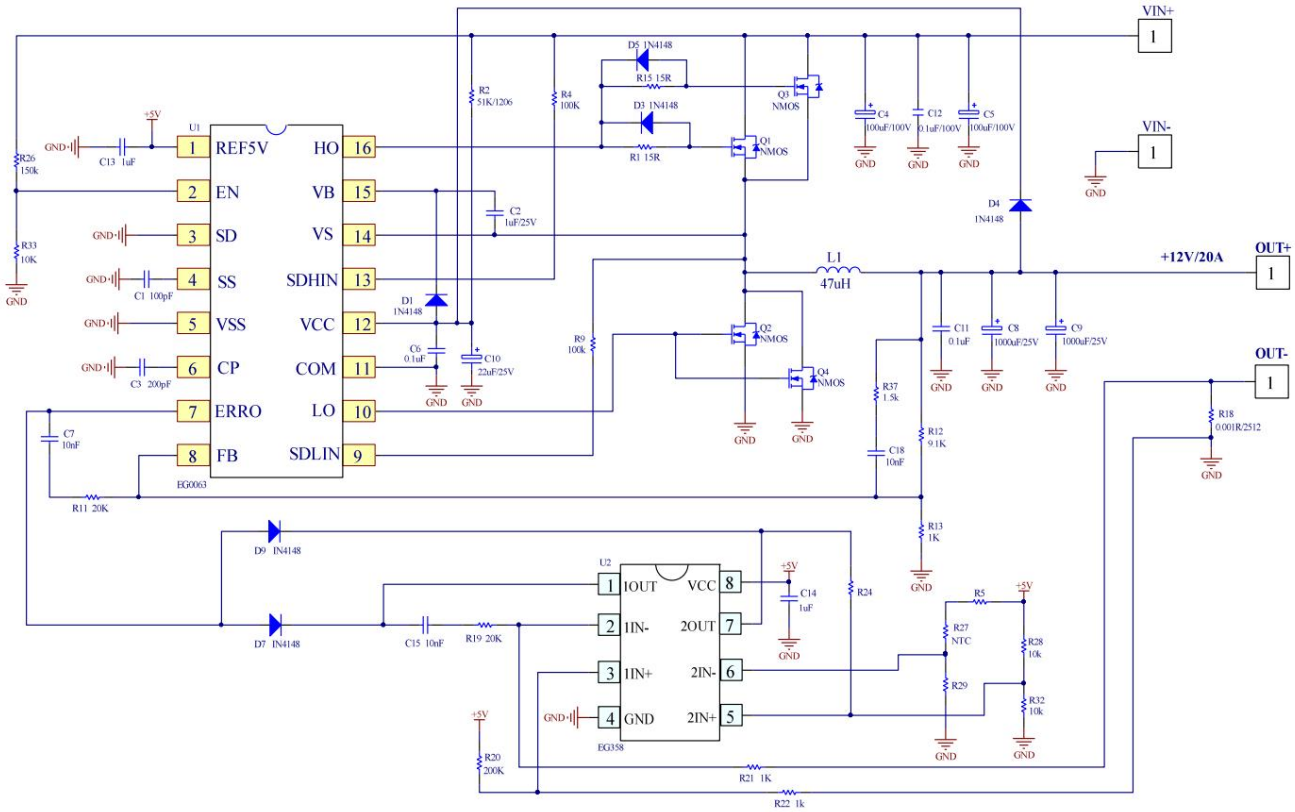

Figure 6-1. Typical application circuit diagram of EG1163 12V20A constant voltage constant current synchronous rectification solution

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7. Electrical characteristics

7.1 Limit parameters

Unless otherwise specified, at TA=25ÿ

Symbolic parameter name		Test conditions	Minimum and maximum units		
TO	High-end output		VS-0.3	VB+0.3	V
VB	Bootstrap high-side VB power supply		-0.3	600	V
VS	High-end floating ground terminal		VB-20	VB+0.3	V
SDHIN	High Side Comparator Input		VS-0.3	VS+5	V
VCC	Low-end power supply		-0.3	20	V
IT	Low-end output		-0.3	VCC+0.3	V
SDLIN	Low-side comparator input		-0.3	+5	V
FBÿERRORÿCPÿSSÿ REF5V	Low pressure port		-0.3	+5.5	V
SDÿEN	Control Port		-0.3	20	V
FACING	Ambient temperature		-45	125	ÿ
Tstr	Storage temperature		-65	150	ÿ
TL	Soldering temperature	T=10S		300	ÿ

Note: Exceeding the listed limit parameters may cause permanent damage to the chip. Long-term operation under extreme conditions will affect the reliability of the chip.

7.2 Typical Parameters

Unless otherwise specified, at TA = 25°C

Symbol Parameter Name High voltage power supply		Test conditions	Min.Typ.Max.Unit			
VB		VB Input Voltage	10		600	V
VCC	Low voltage power supply	VCC Input Voltage	10		20	V
Start	VCC startup current			200	300	uA
VCCÿONÿ	VCC turn-on voltage	EG1163	14	15	17	V
VCCÿOFFÿ	VCC shutdown voltage	EG1163	8	9	10	V
VCCÿONÿ	VCC turn-on voltage	EG1163S	7.5	8.5	9.3	V
VCCÿOFFÿ	VCC shutdown voltage	EG1163S	6.7	7.5	8.3	V

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Reference voltage						
REF5V	5V Reference Output	VCC on, VCC=12V 4.8		4.9	5.0	V
ÿ VREF	Line Regulation	VCC=10V to 20V		3	50	mV
ÿ VREF	Load Regulation	IL=0 to 10mA		5	50	mV
This	Maximum output current			50		mA
Oscillator						
dark	Oscillation frequency range	CT=200pF	65	72	80	KHz
ÿ f/ÿ VCC voltage rejection ratio		CT=200pF		±3 ±5 %		
ÿ f/ÿ T Temperature drift				±5 ±8 %		
Error Amplifier						
FB Error amplifier feedback terminal			1.188	1.2	1.212	V
Iron	Error amplifier output Flow Capacity		15	20	25	uA
Ib Input bias current					0.1	uA
AVOL	Open loop gain		60	75		dB
PWM control						
D(max) Maximum output duty cycle				95		%
IN	EN Enable terminal comparison voltage		1.15	1.2	1.25	V
SD turns off PWM voltage cycle by cycle			3			V
Current Comparator						
SDHIN High-Side Current Comparator		Relative VS voltage		180		mV
SDLIN Low-Side Current Comparator		Relative COM voltage		180		mV
Dead time characteristics						
DT	Dead time		150	200	250	nS
Output **MOS** drive capability						
I HAVE BROWNED Source current	IO+	Vo=0V, VIN=VIH PWÿ10uS	0.8	1.2		A
I HAVE BROWNED Sink Current	IO-	Vo=12V, VIN=VIL PWÿ10uS	1.5	2		A

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8. Application Design

8.1 REF5V Input Capacitance

Placing a high-frequency, small-capacitance bypass capacitor between the REF5V pin and the ground will reduce the high-frequency noise at the REF5V end. A 1uF ceramic capacitor can be used as the high-frequency bypass capacitor. When laying out the board, place it as close to the chip pin REF5V input end as possible.

8.2 VCC Energy Storage Capacitor

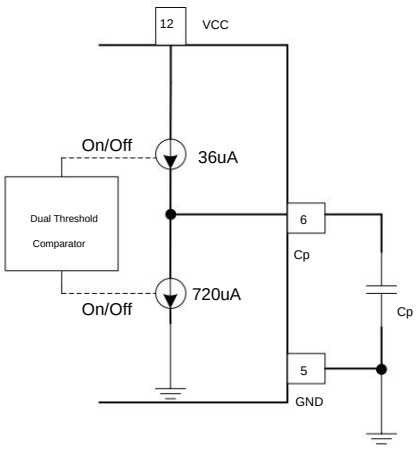
EG1163 requires a 10uF capacitor to be placed between the VCC pin and the ground. It is mainly used to store energy and charge the VCC pin during startup and stabilize the working voltage of the VCC pin during normal operation. At the same time, the capacitor has a certain effect on output short-circuit protection. When the output is short-circuited, the VCC pin will lose power and the chip will enter the UVLO mode. The size of the capacitor will affect the time it takes for the chip gap to turn on the power tube when the output is short-circuited. The larger the capacitor, the longer the gap time and the smaller the heat of the power tube. Otherwise, the heat of the power tube will increase.

8.3 Startup Process

The input power starts to charge the external capacitor of the VCC pin through the external R2 resistor. At this time, the EG1163 chip will consume about <1mA of working current in the low static current working mode. Only the UVLO circuit is working inside, and other oscillators and PWM modules are in the off state. The output voltage is zero. When the capacitor voltage on the VDD pin is charged to more than 17V, the chip starts to work normally, turns on the oscillator, PWM module and feedback processing circuit, and outputs a regulated voltage. At the same time, the output voltage provides VCC working power to the VCC pin through an external diode, and the startup process ends.

8.4 Calculation of the switching frequency of the oscillator Cr capacitor

EG1163 only needs an external capacitor to set the PWM operating frequency. The internal constant current source is used to charge and discharge the Cp capacitor as shown in Figure 8.4a.



The constant current source of current injection provides a current of about 36uA to charge the Cp capacitor, and the constant current source of current sourcing provides a current of about 720uA to discharge the CT capacitor. The approximate relationship between the operating frequency and capacitance is determined by the formula f=(14.4 x106)/Cp (the capacitance unit of this formula is pF). For example , for a capacitor of Cp=200pF, the corresponding PWM operating frequency is about 72KHz.

Figure 8.4a Oscillator CT charging and discharging principle block diagram

8.5 Output Peak Current Limit

The high-end output peak current limit of the EG1163 chip is determined by the internal resistance of the high-end MOS tube, and the peak current relationship is IPK=200mV/(high-end MOS tube internal resistance); the low-end output peak current limit of the chip is determined by the internal resistance of the low-end MOS tube, and the peak current relationship is IPK=200mV/(low-end MOS tube internal resistance).

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8.6 Output short circuit protection

When the output is short-circuited, EG1163 will work at the maximum peak current limiting output, and the voltage of VCC will be lost. Since the output voltage can no longer provide power to the VCC pin through the diode, the static working current of the EG1163 chip quickly discharges the voltage of the capacitor on the VCC pin. When the voltage of the VCC pin is lower than 8 V, the EG1163 chip will completely turn off the PWM output. At the same time, the input power will recharge the capacitor of the VCC pin through the external startup resistor. When the voltage of the VCC pin is higher than 17V, the chip will turn on PWM again. If the output is always in a short-circuit state, the chip will intermittently turn on the power tube. At this time, the EG1163 chip will be in current limiting and short-circuit protection mode.

8.7 Output Inductance

EG1163 has two working modes: continuous working mode and discontinuous working mode. The value of inductance will affect the working mode of the buck.

When the load is light, EG1163 works in discontinuous working mode. At the same time, the inductance value will affect the ripple of the inductor current. The selection of inductance can be based on the following formula:

$$L=\frac{Vout(Vin\ \ Vout)}{Vin.Fs.Iripple}$$ Where Vin is the input voltage, Vout is the output voltage, Fs is the PWM operating frequency, and Iripple is the current ripple in the inductor.

The peak-to-peak value of the ripple is usually selected so that Iripple does not exceed 30% of the maximum output current.

8.8 Synchronous Rectification **MOS** Tube

The synchronous rectification MOSFET is used to replace the freewheeling diode of the traditional asynchronous converter, thereby greatly improving the power conversion efficiency; synchronous rectification The MOSFET is selected with low internal resistance and low junction capacitance to provide good performance for the EG1163 buck.

8.9 Output Capacitor

The output capacitor Co is used to filter the output voltage so that the DC-DC buck outputs a relatively stable DC power to the load. When selecting this capacitor, try to select a capacitor with a low ESR. The value of the capacitor is mainly determined by the ripple requirement of the output voltage, which can be determined by the following formula:

ÿ Vo=ÿ ILÿESR+ $\frac{1}{8.Fs.Co}$) where ÿ Vo is the output voltage ripple, ÿ IL is the inductor current ripple, Fs is the PWM operating frequency, and ESR is Output capacitor equivalent series resistance.

8.10 Output Voltage Regulation Settings

The output voltage of EG1163 is set by two voltage-dividing resistors on the FB pin. The internal error amplifier reference voltage is 1.2V, as shown in Figure 8.10a. The output voltage Vout = (1 + R1/ R2) * 1.2V. To set the output voltage to 12.12V, set R1 to 9.1K and R2 to 1K. The output voltage Vout = (1 + 9.1/1) * 1.2V = 12.12V.

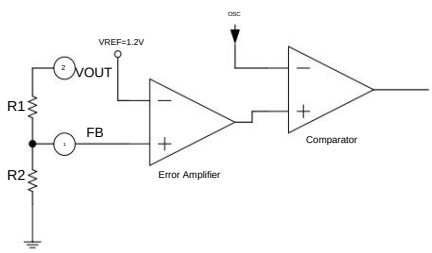

Figure 8.10a EG1163 output voltage adjustment circuit

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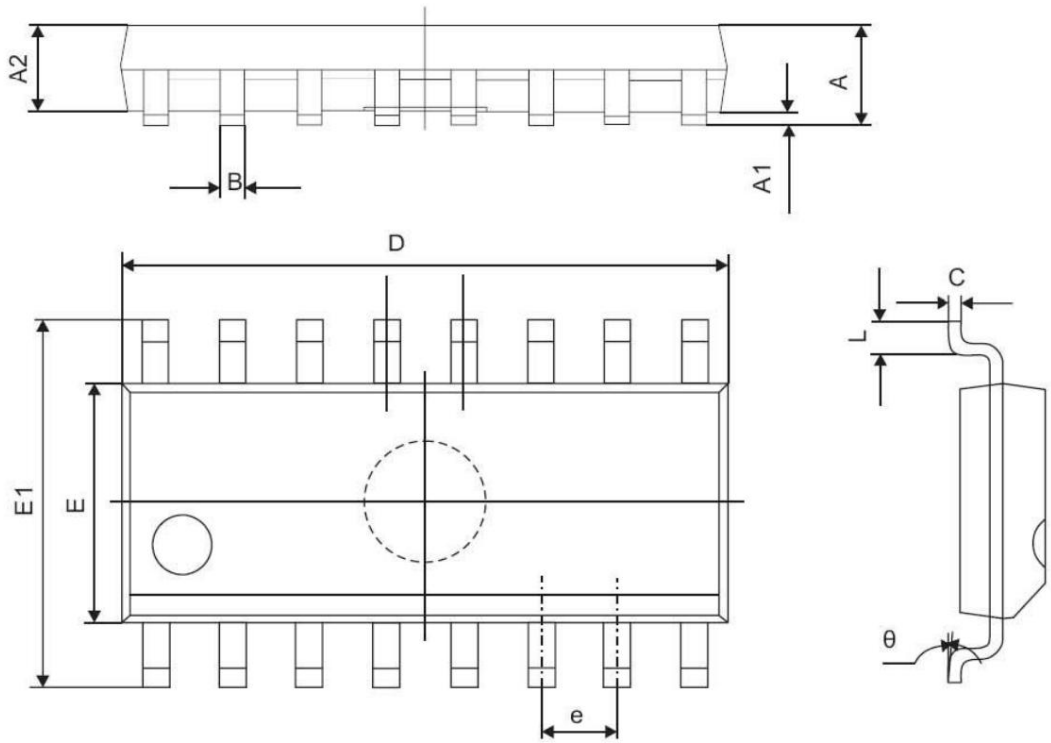
9. Package size

9.1 SOP16 Package Dimensions



symbol	Dimensions (mm)	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
B	0.330	0.510
C	0.190	0.250
D	9.800	10.000
AND	3.800	4.000
E1	5.800	6.300
and	1.270ÿTYPEÿ	
L	0.400	1.270
Th	0°	8°

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