



a Modular Battery Management System for LFP Batteries

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Report presented in partial fulfilment of the requirements for the degree of Electrical Engineering in the Faculty of Engineering at Stellenbosch University.

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Executive Summary

The project “A Modular Battery Management System for LFP Batteries” concerns the design, develop, and test a modular Battery Management System (BMS) for Lithium Iron Phosphate (LFP) batteries to optimize cell management. Current BMS solutions face issues like wire overload and inaccurate voltage measurements in high voltage banks due to extended wiring to a single controller. This project presents a BMS design where each cell has a monitoring module with its micro-controller, ensuring precise voltage measurements and module-to-module communication. The improved BMS aims to boost efficiency and accuracy in high voltage banks, benefiting renewable energy, electric vehicles, and energy storage. Potential challenges include logistical, practical constraints, and technical hurdles. However, rigorous testing and the system’s adaptability predict success. Future work can expand on this BMS design, adapting it for other batteries or systems. The project’s continuation plans comprise thorough documentation, sharing results with academia, and collaboration opportunities for advanced battery management system research.

Afrikaans:

Die projek ”’n Modulêre Battery Bestuurstelsel vir LFP Batterye“ handel oor die ontwerp, ontwikkeling, en toetsing van ’n modulêre Battery Bestuur Stelsel (BBS) vir Litium Yster Fosfaat (LFP) batterye om sel bestuur te optimaliseer. Huidige BBS oplossings ondervind probleme soos draad oorlading en onakkurate spanning metings in hoë spanning banke as gevolg van verlengde bedrading na ’n enkele beheerde. Hierdie projek bied ’n BBS ontwerp waar elke sel ’n moniterings module met sy eie mikroverwerker het, wat akkurate spanning metings en module-tot-module kommunikasie verseker. Die verbeterde BBS beoog om effektiwiteit en akkuraatheid in hoë spanning banke te verhoog, ten voordeel van hernubare energie, elektriese voertuie, en energie stoor. Potensiële uitdagings sluit logistieke, praktiese beperkinge, en tegniese struikelblokke in. Nietemin, deeglike toetsing en die stelsel se aanpasbaarheid voorspel sukses. Toekomstige werk kan voortbou op hierdie BBS ontwerp, deur dit aan te pas vir ander batterye of stelsels. Die projek se voortsettings planne sluit in deeglike dokumentasie, die deel van resultate met die akademie, en samewerkings geleenthede vir gevorderde battery bestuur stelsel navorsing.

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Nomenclature

Variables

V	Voltage
I	Current
R	Resistance
P	Power
t	Time
C	Capacitor
V_s	Supply Voltage
V_{CC}	Voltage Common Collector
V_{IN}	Input Voltage
V_{OUT}	Output Voltage
V	Volt
mV	Milli-Volt
A	Ampere
mA	Milli-Ampere
R_{th}	Thevenin Resistance
R_s	Sense Resistance
R_{sh}	Shunt Resistance
Ω	Ohm
$k\Omega$	Kilo-Ohm
W	Watts
mW	Milli-Watts
s	Seconds
μF	Micro-Farad
nF	Nano-Farad
S	Sensitivity
β	Temperature Coefficient
T_0	Nominal Temperature

Acronyms

BMS	Battery Management System
Op-Amp	Operational Amplifier
LFP	Lithium Ferro-Phosphate
ADC	Analog-to-Digital Converter
DFR	Drive the Future ROBOT
EV	Electric Vehicle
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NC	Not-Connected
NOPB	Lead-free Component
NTC	Negative Temperature Coefficient
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
SCL	Serial Clock Line
SDA	Serial Data Line
SOC	State of Charge
SOH	State of Health
SPS	Samples per Second
LCD	Liquid Crystal Display
CAD	Computer-Aided Design
IDE	Integrated Development Environment
DC	Direct Current
GND	Ground
LED	Light Emitting Diode
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver/Transmitter
GPIO	General Purpose Input/Output

Chapter 1: Introduction

1.1. Synopsis

The research and design in this technical report is focused on advancing energy storage solutions through the development of an innovative Battery Management System (BMS) for Lithium Ferro Phosphate (LFP or LiFePO₄) batteries. The initiative seeks to redefine energy storage management paradigms by employing novel methodologies and a distinct architecture, enhancing interactions with comprehensive energy storage mechanisms. This is pivotal for sectors including renewable energy, electric vehicles, bulk energy storage, emergency backup power, and long-term high voltage DC storage.

Battery Management System:

a BMS is an electronic system that manages and safeguards a rechargeable battery (cell or battery pack), ensuring optimal performance, prolonged life, and safety. The BMS monitors and regulates various attributes, such as charging and discharging rates, voltage, and temperature. It provides crucial insights and notifications regarding the state of the battery, such as State of Charge (SOC) and State of Health (SOH), while also ensuring the battery operates within safe parameters, thereby protecting against scenarios like overcharging, overheating, or deep discharging which could be detrimental to the battery's lifespan and performance. In applications like electric vehicles, grid storage, and portable electronics, a BMS plays a pivotal role in ensuring efficient energy utilization, reliability, and safety of the battery usage. [24]

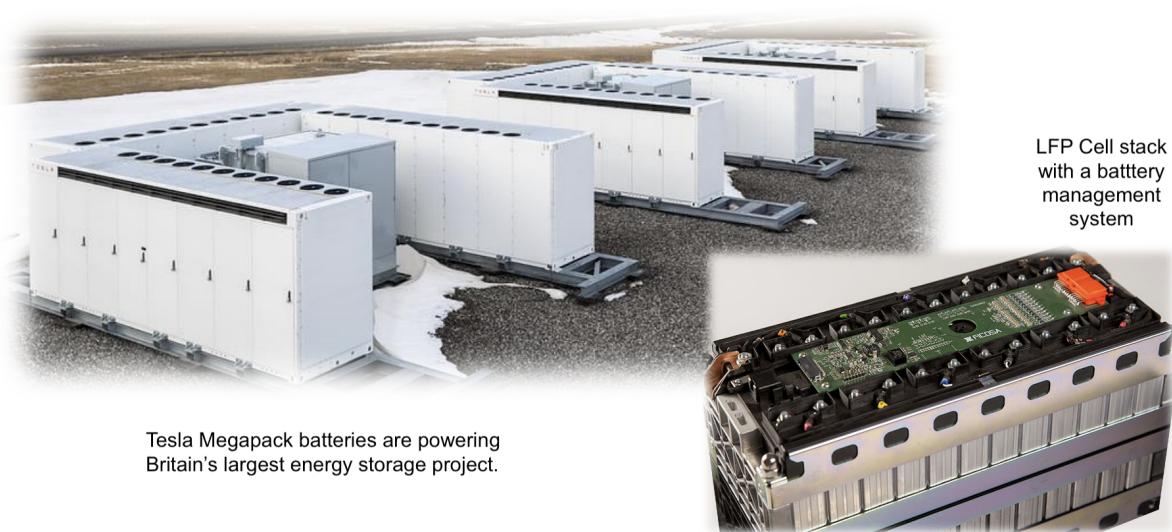


Figure 1.1: High Voltage Battery Bank & a BMS [1]

1.2. Problem Statement

In the pursuit of developing high voltage battery banks, comprising about 250 cells arranged in series to achieve an approximate voltage of 800V, several significant challenges emerge when interfacing with standard battery management systems (BMS). The primary challenge emanates from the extensive cell strings which, upon connection to a conventional BMS, induce wire overload and inaccurate voltage measurements due to the long wires leading to a single controller, which is ill-suited for precise monitoring across such a vast array of cells.

This issue is accentuated by inherent design hurdles associated with high voltage battery banks, such as the imperative need for isolation of communications and transient protection within the BMS to prevent voltage spikes and other transient events, alongside undesirable interactions that could jeopardize system integrity. Accurate state of charge (SOC) and state of health (SOH) estimation of each cell are paramount for safe and efficient battery bank operation.

Furthermore, electrical threats like overcurrents, surges, and electrostatic discharge pose additional challenges that the BMS must robustly guard against. The cumulative effect of these challenges elucidates the inadequacy of a single-controller BMS in efficaciously managing and monitoring the numerous cells in high voltage battery banks. Thus, a suitable architecture, that is highly scalable, is desired for the development of high voltage battery banks to overcome the wire overload and inaccurate monitoring predicaments inherent in existing BMS configurations.

1.3. Project Description

To address the aforementioned challenges, an innovative design is proposed: deploying a small module with monitoring components and its own micro-controller atop each cell, thereby establishing an individual BMS for each cell. This alternative design significantly mitigates the problem of inaccurate voltage measurements encountered with long wires to a single controller, ensuring a more reliable and robust monitoring system.

With voltage measurements taken in close proximity to each cell and facilitated by serial communication between the monitoring modules, a high degree of measurement accuracy is achieved. Initially, the design prototype will be applied to four cells. However, the inherent modular design facilitates seamless scalability, making it adaptable to the high voltage battery bank's requirements by simply augmenting more cells with modules, fostering a flexible and easily expandable battery management solution.

Although realized through individual module analysis due to logistical and practical constraints, the project's design is fundamentally scalable, allowing for integration into complex, high-voltage systems. The modular BMS, detailed in this report, encompasses hardware design, software development, and performance testing, forming a comprehensive overview of the proposed system.

Its modular and adaptable nature guarantees applicability across various domains, positing it as a versatile solution for diverse energy storage requirements, thereby potentially playing a pivotal role in the future energy sector. Through rigorous testing, the superior performance and scalability of the Modular BMS are underscored, demonstrating its potential as a robust and reliable solution for managing Lithium Iron Phosphate (LFP) batteries, and laying a robust foundation for further research and development in battery management technology.

1.4. Report Brief

This report presents a detailed review of the project, focusing on the fundamentals of battery management systems and the specifics of the prototype. It covers concepts, design principles, implementation methods, and evaluations, summarizing the project's outcomes and recommendations for future improvements. The flow diagram below provides a structured overview of the report's content.

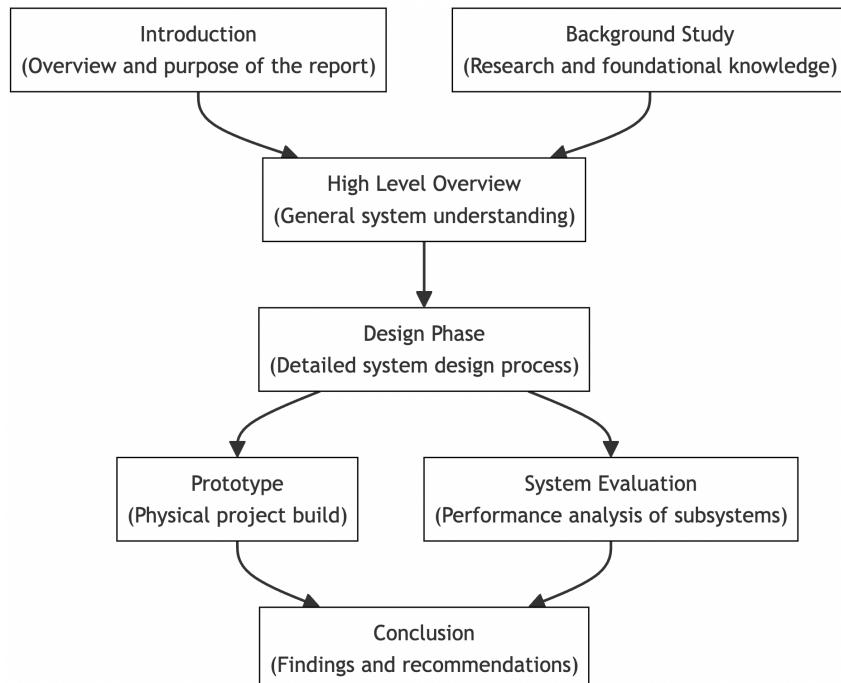


Figure 1.2: Report Structured Overview [2]

Chapter 2: Background Study

2.1. Trending Literature

The landscape of battery technology has been rapidly evolving to meet the escalating demands for energy storage solutions, primarily driven by the global transition towards electric vehicles (EVs) and renewable energy. The heart of this evolution lies in the Battery Management Systems (BMS) that ensure safe and efficient operation of batteries, forming a critical component of high voltage battery banks in EVs and grid storage.

Recent trends spotlight the shift towards designing scalable modular systems in BMS to accommodate the high voltage requirements. The modular BMS segment, for instance, is projected to register the highest growth rate owing to its ability to connect in series or parallel circuits, thereby augmenting the power/voltage output with the fringe benefit of lower maintenance costs [25]. This indicates a move towards developing flexible and scalable BMS architectures that can seamlessly adapt to varying voltage requirements, essential for high voltage battery banks.

In the quest for more affordable and safer electric vehicles, continuous innovation in BMS architectures is pivotal. It's not just about managing existing battery chemistries, but also about being prepared for new and emerging ones. Solid-state batteries, for example, promise more energy in a smaller space, faster charging times, and enhanced safety, which BMS designs need to accommodate [26].

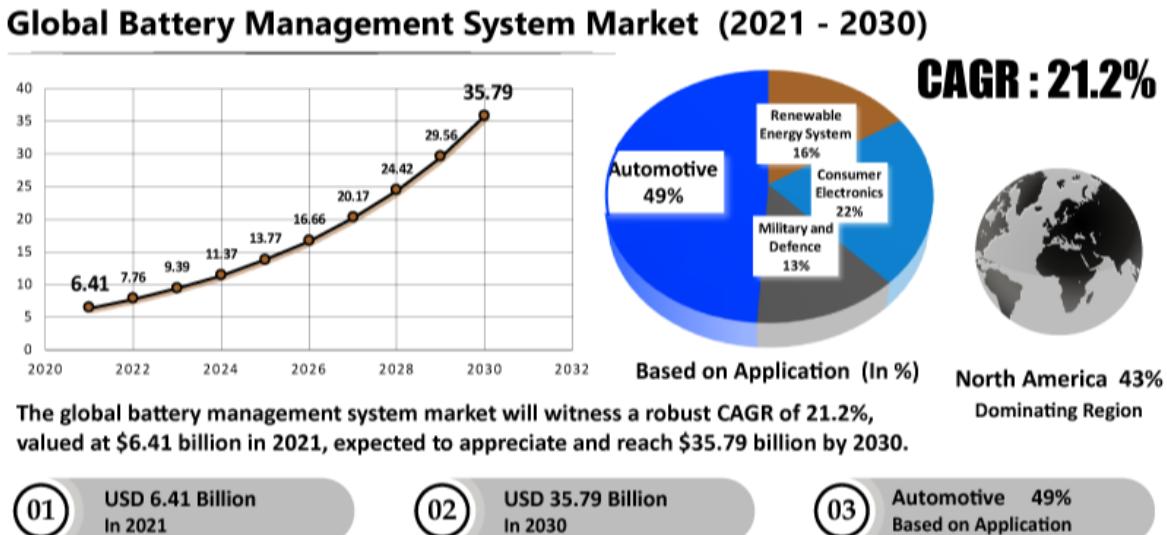


Figure 2.1: Projected Forecast of the BMS Market [3]

The market's trajectory further corroborates the booming interest in BMS technologies. The global BMS market size, which stood at USD 7.8 billion in 2022, is on a steep ascent, poised to touch USD 55.1 billion, driven by the quest for reducing the cost of battery electronics and simplifying designs to cut down on hardware and wiring costs [27].

Moreover, the technological advancements by companies like Vitesco Technologies underscore the industry's momentum. With orders worth over 2 billion euros for its innovative BMS, the future seems propitious for further ingenuity in BMS designs, underlining the importance of BMS in the broader narrative of renewable energy solutions [28]. This burgeoning sector has caught the attention of various stakeholders, invigorating a flurry of activities around BMS technologies, whether it's about reducing costs, enhancing safety, or accommodating new battery chemistries. As this trend continues, the evolution of BMS is deemed to play a cardinal role in propelling the broader adoption of electric vehicles and renewable energy systems, making it a focal point of interest among industry players, researchers, and policymakers.

2.2. High Voltage DC systems

High voltage DC battery storage systems operate at voltages exceeding 96V, with potential levels up to 384V or even 800V [29]. With cell modules or individual cells in series, the system achieves the desired operational voltage, each unit incrementing the total voltage. The advantage of high voltage configurations lies in the reduction of $I^2 \cdot R$ losses, as a higher voltage level lowers the current required for a specific power output, enhancing system efficiency. High voltage systems simplify design by reducing parallel strings and current ratings, lowering component costs and easing battery management, which may enhance reliability and lifespan. To comprehend the simplification for a design, I evaluated examples of HV systems and saw that in principle a design can be formulated using straightforward calculations with equations 2.1, 2.2 & 2.3, adjusting the variables below.

Table 2.1: Example Parameters for a HV Battery Bank Design [21]

Parameter	Symbol	Typical Value
Nominal voltage of cell/module	V_{nom}	48V
Number of cells/modules in series	n	Variable
Total System Voltage	V_{total}	$n \cdot V_{\text{nom}}$
Nominal Capacity	C_{nom}	50Ah
Maximum Charging Current	I_{charge}	50A
Maximum Discharging Current	$I_{\text{discharge}}$	50A
Charge Cut-off Voltage	$V_{\text{charge,cutoff}}$	438V
Discharge Cut-off Voltage	$V_{\text{discharge,cutoff}}$	300V

$$V_{\text{total}} = n \cdot V_{\text{nom}} \quad (2.1)$$

$$C_{\text{total}} = C_{\text{nom}} \quad (2.2)$$

$$E_{\text{total}} = V_{\text{total}} \cdot C_{\text{total}} \quad (2.3)$$

These equations form the basis for designing high voltage battery banks. The modularity of the design allows for scalability; additional modules can be connected in series to increase the voltage or in parallel to increase the capacity, thereby accommodating varying energy storage needs. The operational parameters like maximum charging and discharging currents are crucial to ensure the safety and efficiency of the system. [30]

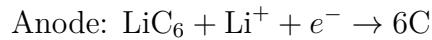
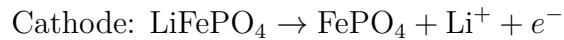
In summary, the theoretical formulation of a high voltage battery bank hinges on the series connection of cells/modules, with the total system voltage and capacity governed by the nominal voltage and capacity of individual cells/modules. This modular and scalable design is fundamental to meeting the diverse energy storage requirements across different applications.

2.3. Lithium Ferro Phosphate Technology

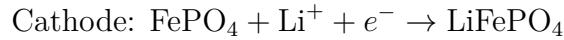
Chemistry of LFP Cells

Lithium Iron Phosphate (LiFePO₄ or LFP) cells function through the process of lithium ions moving from the cathode to the anode and vice versa during discharge and charge cycles, respectively. This movement, termed intercalation (insertion) during discharge and deintercalation (extraction) during charge, facilitates the storage and release of electrical energy. The primary components of an LFP cell are its cathode, composed of lithium iron phosphate, its anode made of graphite, and the electrolyte, a lithium salt dissolved in an organic solvent. The cathode serves as the source and sink of lithium ions, enabling the reversible electrochemical reactions crucial for the cell's energy storage and delivery. [31]

Discharge



Charge



Typical Data Specs

- Nominal Voltage: 3.2V
- Energy Density: 90Wh/kg - 120Wh/kg
- Cycle Life: > 2000 cycles (80% DoD)
- Charge/Discharge Efficiency: 95% - 98%
- Operating Temperature Range: -20°C to 60°C

C Rating

The C rate denotes the rate at which a battery is charged or discharged, calculated as:

$$\text{C Rate} = \frac{\text{Current (A)}}{\text{Capacity (Ah)}}$$

Discharge Current

For a 100Ah cell with a 1C rate, the current capability for 1 hour of constant discharge is:

$$\text{Current (A)} = \text{C Rate} \times \text{Capacity (Ah)} = 100A$$

Charge Current

Selection of charge current, guided by manufacturer specifications, affects charging time, heat generation, and cell lifespan.

Cells in Series

In series connections, voltage accumulates while capacity remains constant, necessitating careful management to prevent overcharge or over-discharge.

Cell Balancing

Balancing ensures equal state of charge (SoC) in series-connected cells, employing active or passive techniques to prevent overcharge or over-discharge.

Cell Comparison

Table 2.2: Cell Types [22] [23]

Aspect	LFP (LiFePO4)	NMC (LiNiMnCoO2)	LCO (LiCoO2)
Energy Density	~90-120 Wh/kg	~150-220 Wh/kg	~200 Wh/kg
Safety	Higher	Lower	Lower
Lifespan	>2000 cycles	~1000-2000 cycles	~500-1000 cycles
Cost	Less Expensive	More Expensive	Expensive
Thermal Range	-20°C to 60°C (-4°F to 140°F)	-20°C to 55°C (-4°F to 131°F)	-40°C to 70°C (-40°F to 158°F)
Industry Usage	31%	N/A	N/A

2.4. Battery Cell Monitor and Control

Battery Management

Battery management is pivotal to the evolution and efficiency of battery-operated systems, marking a significant stride from the invention of the first true battery by Alessandro Volta in 1799, to the modern rechargeable batteries pioneered by Gaston Plante in 1859 [32]. The burgeoning rise of electric vehicles (EVs) and the global shift towards carbon neutrality underscored the imperative for adept battery performance monitoring and management for enhanced efficiency, safety, and user satisfaction [33].

Historically, the nascent forms of battery management were rudimentary, primarily encompassing basic protection circuits for discharge current tripping, which were unstable. The evolution of electronic protection circuits, integrated into comprehensive battery management systems (BMS), marked a significant advancement, catering to a myriad of battery chemistries [34]. Passive cell balancing emerged as a technique to equalize the State of Charge (SoC) among cells in a battery stack, particularly focusing on cells with lower capacity to ensure balanced performance [35].

With the proliferation of onboard batteries across various applications, the exigency for advanced management burgeoned, precipitating the development of centralized and distributed battery management systems aimed at bolstering battery performance and user experiences [36]. The evolution of batteries was inextricably tied to the products and systems that employed them. The burgeoning demand for improved portable power sources, propelled by the ubiquity of mobile computing and communication, spearheaded innovations in battery management technology [37].

Controller Topology

The controller topologies in Battery Management Systems (BMS) are quintessential for efficient monitoring and regulation of battery packs. These topologies are crafted to meet specific requirements and applications, thereby ensuring the safety and reliability of battery operations.

Centralized Topology:

In a centralized topology, a singular control unit is interfaced with each cell in the battery pack through separate wiring. This control unit is pivotal for monitoring and managing the battery cell parameters, thereby ensuring the safe and reliable operation of the overall battery pack [38].

Modular Topology:

The modular topology encompasses a master controller, multiple slave controllers, and an electric meter. The master controller orchestrates communication with the slave controllers, each accountable for a subset of battery cells, while the electric meter furnishes pack-level readings. This topology is employed to manage larger battery packs efficiently, offering a scalable solution for battery management [39].

Distributed Topology:

In a distributed topology, dedicated control units are allocated at a central control unit, each tethered to individual battery cells. This setup facilitates granular control and monitoring of each cell, ensuring swift identification and rectification of any discrepancies in cell performance. Although the control units are dedicated, they are centrally located, not positioned atop each cell, which augments the monitoring efficacy while maintaining a structured control hierarchy [40].

The choice of topology is contingent on the application, size, and configuration of the battery pack, and the requisite level of control and monitoring. The broad spectrum of applications with different voltage classes, necessitates divergent controller topologies to align with the hardware requirements of BMS for a given application. Understanding these topologies and their ramifications on the BMS performance is instrumental for engineers to design and implement efficacious and reliable BMS controllers.

2.5. Module Communication Methodology

Communication is crucial for the effective functionality of the envisioned system, as it facilitates the transfer of data and enables interaction between individual cells through their respective monitoring modules. A comprehensive investigation was undertaken to discern a communication methodology that aligns seamlessly with the project's overarching objectives. Initial evaluations delved into the Canbus design orchestrated by Stuart Pittaway [41] and the isoSPI design conceived by Mark Wolf [42], yet both methodologies were deemed incompatible with the project's requirements. Subsequently, the isolated UART serial communication design emerged as a suitable solution, rendering compatibility with the smaller microcontrollers envisaged for the project, and permitting isolation between differing voltage levels across the communication pathway, ensuring a robust communication framework [43].

Two principal communication configurations were meticulously explored: the daisy-chain and all-call UART connection configurations, as illustrated in Figures 2.2 and 2.3, respectively. The daisy-chain configuration links devices in a series, each connected to

the next device's RX and TX pins, forming a closed loop, as further elucidated by a reference design from Texas Instruments specifically tailored for battery management applications [44]. On the other hand, the all-call configuration establishes a parallel connection of devices to a single communication line, with all devices interfacing directly with the master controller's RX and TX pins, thereby centralizing the communication system.

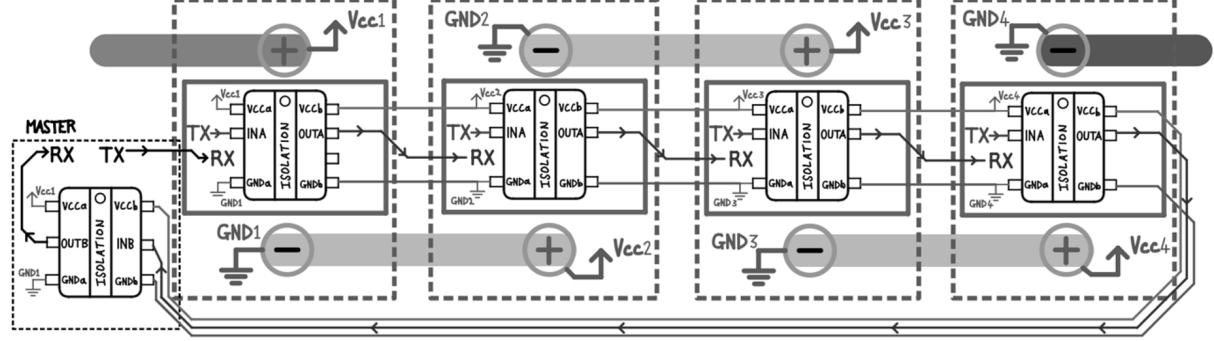


Figure 2.2: Daisy-chain configuration.

The depicted diagram above illustrates a daisy-chain architecture among a stack of microcontrollers, where each device transmits messages sequentially, initiating a new cycle upon completion of the loop. Each device in the chain transmits only after successful reception. This allows the modules to receive messages from the other modules within one full cycle.

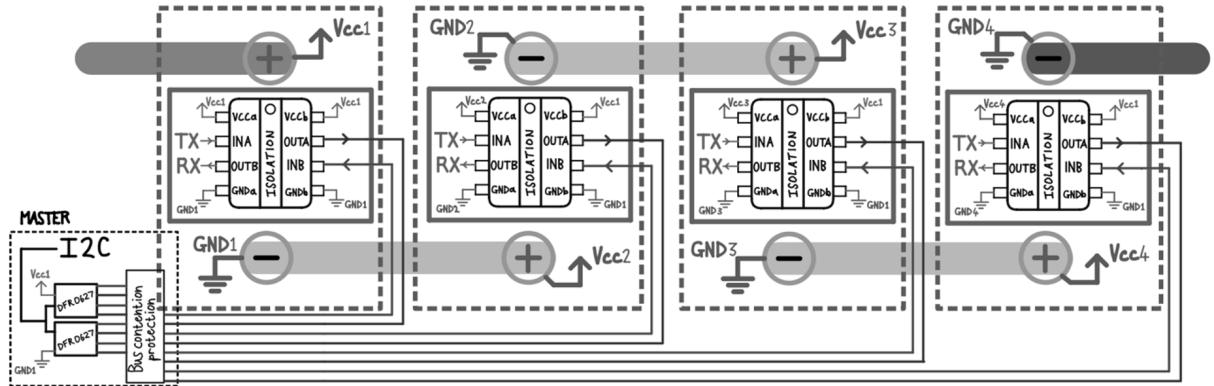


Figure 2.3: All-call configuration.

In the all-call configuration, modules communicate exclusively with the main controller, which operates in parallel with the slave modules. System data exchange among all modules now necessitates two cycles, albeit expedited due to the main controller's broadcast capability.

A comparative analysis of these configurations is presented in Table 2.3, delineating various aspects like hardware and wiring complexity, transmission delay, data rate, software complexity, and fault tolerance.

Table 2.3: UART Hardware Configuration Comparison

Feature	Daisy-Chain Configuration	Bus Configuration
Definition	Devices are connected in a series, with each device connected to the next device's RX and TX pins, forming a closed loop	Devices are connected in parallel to a single communication line, with all devices connected to the same RX and TX pins of the master controller
Hardware Complexity	Simple, each device requires only two connections for RX and TX	More complex, requires additional hardware components, such as pull-up resistors and line drivers, to ensure reliable communication
Wiring Complexity	Increases with the number of devices in the chain, requires more connections between devices	Simplifies wiring, reduces number of connections required, all devices are connected to the same lines
Transmission Delay	Each device must wait for the previous device to complete its transmission before transmitting data, limiting the data rate	Devices can transmit data at any time, without waiting for other devices, potentially increasing the data rate
Data Rate	Limited by the transmission delay between devices, which increases with the number of devices in the chain	Potentially higher, depending on hardware and software design, can support higher data rates
$DataRate_{MAX}$	$DR_{max} = \frac{baudrate \times (\#databitsperbyte)}{10 \times (\#devices)}$	$DR_{max} = \frac{baudrate}{10 \times (\#databits+paritybits+stopbits)}$
Software Complexity	Higher, requires time delay programming for each device to ensure data is transmitted in sequence	Simpler, devices can transmit data at any time, without waiting for other devices
Fault Tolerance	Communication can be disrupted if any device fails, since it breaks the closed loop	Communication can continue as long as at least one device remains functional, since all devices are connected in parallel
Advantages	Simple hardware design, suitable for small-scale systems with a few devices	Simplifies wiring, can support higher data rates, suitable for larger systems with multiple devices
Drawbacks	Limited data rate, requires time delay programming for each device, may be disrupted if any device fails	More complex hardware design, requires additional components, may be more expensive, may require higher software complexity to manage communication

Based on the analysis, a hybrid solution amalgamating elements from both configurations was devised. This hybrid solution encapsulates the communication methodology aimed for this project, offering a balance of simplicity, reliability, and scalability. More discussion on the communication system and its detailed hardware design is done in section 4.3, where the diagram for the hybrid solution is also presented in Figure 4.13.

Chapter 3: High Level Overview

3.1. Summary

This chapter offers a high-level overview of the project. The "Concept Investigation" section explores the methodology underpinning the project's core idea. The "Design Requirements" section outlines critical specifications and constraints guiding the design. The "Scalable Architecture" section examines the design's adaptability to varying scales and configurations. Lastly, the "Hypothesis & Potential Drawbacks" section discusses assumptions and possible challenges encountered in the design process.

3.2. Concept Investigation

The mainstream approach towards Battery Management Systems (BMS) for large battery banks in the industry has traditionally hinged on robust BMS controllers adept at managing long series cell strings. These systems are generally designed with a fixed cell management capacity, thereby lacking inherent scalability. The prevalent paradigm encapsulates a fixed number of cells within a module, each equipped with its dedicated BMS. These modules can then be arranged in series, with each BMS capable of inter-module communication, facilitating a level of scalability as depicted in the following diagram:

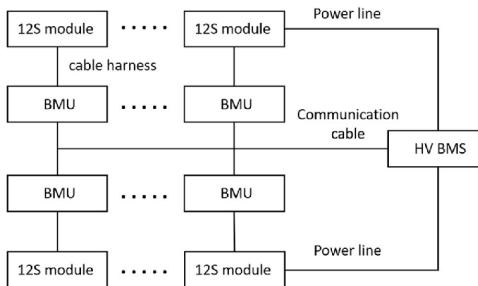


Figure 3.1: Conventional BMS approach for a high voltage battery bank [4]

However, this conventional methodology manifests certain limitations upon scaling, primarily due to the introduction of inaccurate measurements and control constraints. The inaccuracies might stem from the cumulative error propagation and latency in communication as the number of series-connected modules escalates. Moreover, the fixed design poses a barrier to seamless scalability and flexibility in system expansion.

To transcend these limitations and achieve enhanced accuracy in cell monitoring, a novel concept is proposed. Rather than modularizing a group of cells with a shared BMS, each cell is envisioned to be accompanied by its individual monitoring system. The core of this innovative design lies in stacking cells each endowed with its own monitoring

system, thereby circumventing the scalability constraints imposed by traditional designs. The scalability in this scenario is principally governed by the communication bandwidth and line impedance between the monitoring systems.

The proposed design envisages a miniature module atop each cell, housing monitoring components and a dedicated micro-controller, thereby rendering an individualized BMS for every cell. While the prototype is tailored for four cells, the intrinsic design flexibility enables scaling up to accommodate high voltage battery banks by merely augmenting the system with additional cells and modules.

This modular BMS design essentially mirrors the architecture of a conventional BMS but miniaturizes it to fit atop each cell independently. Consequently, every cell in the series string is furnished with a parallel-connected monitoring module. Each of these modules, equipped with its micro-controller, is tasked with processing measurements and relaying the data to a central master device for either storage or further dissemination. The interconnection among all boards facilitates seamless communication, thereby fostering a comprehensive understanding of the battery pack's state across all modules. This collective insight empowers each module to evaluate the global state of the battery pack and fine-tune its respective cell's variables accordingly. The following diagram elucidates the conceptual design of this novel BMS architecture:

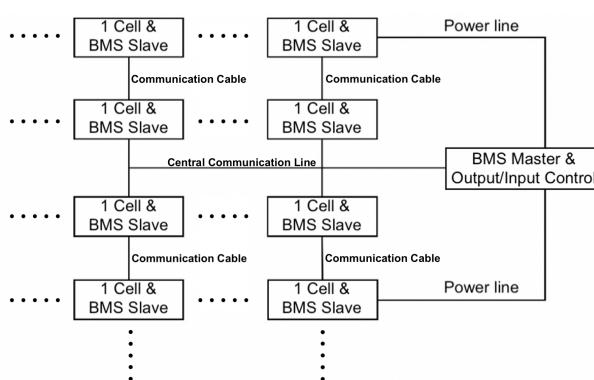


Figure 3.2: Concept Design for a modular BMS

3.3. Design Requirements

The concept design investigated above will be developed in the hardware design of the system to meet requisites for the Battery Management System (BMS) aimed at ensuring modularity, scalability, and reliable performance.

- **Modularity and Scalability:** The BMS is designed to independently monitor an extendable number of cells through dedicated subsystems for each cell. The

initial prototype will monitor four cells, with scalability being a core attribute to accommodate a potentially indefinite number of cells.

- **Communication:** Serial communication via Universal Asynchronous Receiver/Transmitter (UART) protocol will be established among cell monitoring modules and between the modules and the master controller. Isolation in communication is required to handle different voltage levels across the string of cells.
- **Safety Features:** Essential safety features include cell temperature monitoring, cell voltage monitoring, cell balancing, string current monitoring, a reliable relay disconnect mechanism for anomaly detection, force reset functionality for non-responsive scenarios, and over-current protection facilitated through fuses.
- **Cell Monitoring:** Optimized for 105 Ah LFP cells, the design targets maintaining cell terminal voltage within 3.35V to 3V for operational longevity. Accurate voltage monitoring is required, with a preliminary accuracy of around $\pm 0.05\%$. Although cell temperature monitoring does not necessitate high accuracy, exceptional reliability is mandatory.
- **Cell Balancing:** Passive balancing will be employed, with each monitoring module hosting a dedicated dump load circuit targeting a balancing current of around 1A per cell, aligning with the good practice of 1% of the cell's current capacity.
- **Power Supply:** Cell monitoring modules will be powered individually by the respective cells they are monitoring, with cell voltage boosted to a constant 5V for logic level optimization. The master controller will be powered from the series string of four cells through a buck supply delivering 5V.
- **Physical Constraints:** The monitoring modules' PCB dimensions are constrained to approximately 40mm x 40mm to fit between the cell terminals and edges of the cell.
- **Data Rate:** While there is no specific requirement for the data rate, a fairly fast rate is desired. The precise data rate will be determined during the serial communication design phase, and data integrity assurance is not a priority as the design will be used prototype-based.

3.4. Scalable Architecture

The proposed BMS architecture employs individual cell monitoring modules in parallel with each cell in a battery bank, addressing key scalability issues:

1. **Wiring Complexity:** Utilizes four short wires per module for communication and cell terminal connections, minimizing wiring harness and failure risks.
2. **Switching and Sizing:** Independent monitoring and dedicated balancing load per module ensure precise switching and optimal sizing.
3. **Single-Cell Focus:** Individualized monitoring eliminates multicell complications, with inter-module communication ensuring coherent system understanding.
4. **Scalable BMS Architecture Pathway:** The modular design inherently scales with battery bank expansion, promoting a seamless, scalable BMS architecture.

This architecture significantly mitigates conventional scalability challenges, warranting further research and development for efficient, scalable BMS solutions.

3.5. Hypothesis & Potential Drawbacks

This project aims to advance high voltage battery management system (BMS) innovations by designing and evaluating a modular cell monitoring system. The goal is to explore a novel BMS architecture that could inspire future models and enhance the management of LFP cells at high voltages. Although the initial design iteration may not be ready for real-world application, it will provide a foundation for understanding the principles and configurations fundamental to a modular BMS for LFP batteries. The initial phase will focus on experimental design and analysis.

The development will involve a comprehensive process of design and conceptualization to establish a foundational evaluation framework. Given the complex nature of electronic design, encountering unforeseen challenges is expected and listing all potential drawbacks would be impractical. The project's scope may expand due to its multidimensional nature, necessitating strict adherence to a research, design, develop, and evaluate cycle to maintain focus. The timeline is structured to permit only a single design iteration, provided there are no deviations from the planned path.

Component availability and procurement delays are anticipated to affect the schedule, potentially compressing the time available for evaluation. Given the project's scale and timeframe, debugging and design reviews will likely proceed in parallel. Strategies to mitigate time delays include task overlapping, which aims to streamline the project's workflow and minimize disruptions.

Chapter 4: Detailed Design

4.1. Introduction

In this chapter, we delve into the comprehensive design process for the proposed scalable modular Battery Management System. Initially, the design processes for the independent monitoring modules and the main controller are explored separately. Subsequently, the communication system combines the designs of these entities as the main controller serves to collect and process the data monitored by the cell modules. The systematic approach for the design process entails the circuit designs, component selection, and the printed circuit board layout. Afterwards a merged design review of the system is done.

4.2. System Overview

As illustrated in figure 4.1 below the modular BMS design essentially has the same setup as a traditional BMS but the whole system is fitted to each cell independently. As a result, every cell in the series string is equipped with a monitoring module connected in parallel, enabling us to acquire more accurate and precise measurements from each cell. These modules feature their own microcontroller, responsible for processing the measurements and transferring the data to a master device for storage or sharing. Additionally, all the boards are interconnected, allowing for seamless communication and establishing a global view of the battery pack. This collective understanding enables each module to assess the state of the entire pack and make necessary adjustments to its respective cell's variables.

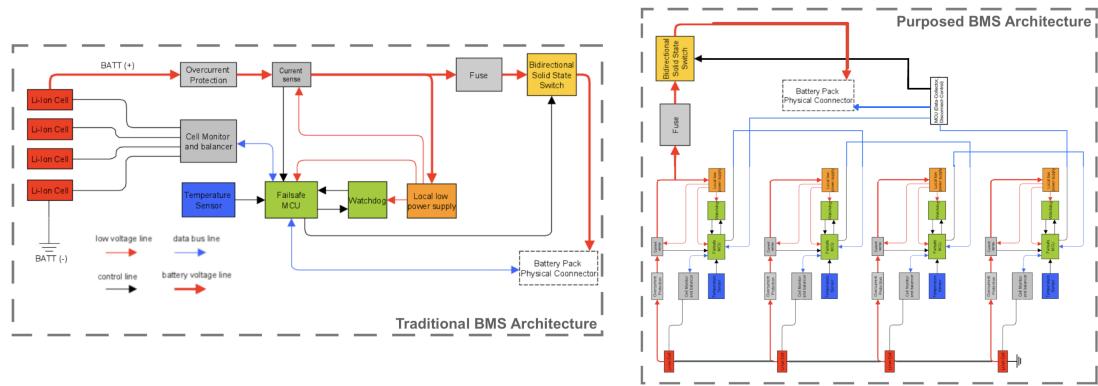


Figure 4.1: Envisioned Architecture of the Proposed BMS

The BMS monitoring boards will be attached to each cell in the battery pack. Their sole wired connection will be the communication line linking the cells, which significantly reduces the use of extensive wiring in the system. The primary (master) controller, located externally, interfaces with the battery pack and facilitates connections to either the load or charger.

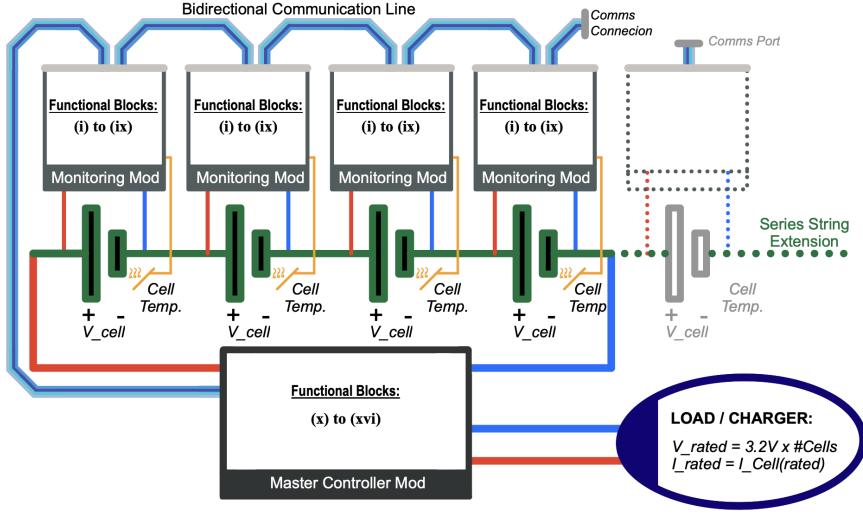


Figure 4.2: System Design Functional Blocks

The design of the BMS is organized into distinct functional blocks, each associated with specific subsystems. For a detailed breakdown of these blocks as depicted in figure 4.2, refer to the subsequent table outlining the primary components of the design.

Table 4.1: Functional Blocks and Subsystems

	Functional Block	Subsystems
	<i>4.3 Monitoring Module:</i>	
i	Cell Connection	Parasite hookup & Inline fuse protection
ii	Voltage Regulation	5V Boost power supply
iii	Supply Jumper & Force Reset	Programmmer mode & Mosfet hard reset
iv	Monitoring Microcontroller	DFR(ATmega32U4) Arduino-Based System
v	Onboard Diagnostics	Internal temperature sensor & Debug LEDs
vi	Cell Voltage Measurement	Analog to digital converter & precision reference
vii	Cell Balancing	Mosfet passive dump load
viii	Cell Temperature Measurement	External sensor for ambient temperature
ix	Isolated Module Communication	UART isolation & transceiver logic
	<i>4.4 Master Controller:</i>	
x	Terminals & Fuse Protection	Battery & load/charger connection
xi	Power Supply	5V Buck converter
xii	Master Microcontroller	ESP32 DevKitCv4 Arduino-Based System
xiii	Battery Current Measurement	Series connected sensor
xiv	System Information Display	LCD and I2C interface
xv	Load/Charge Disconnect	Latching DC contactor
xvi	Scalable Isolated Communication	Broadcast UART isolation

The development process of each element in Table 4.1 will be presented in the subsections: 4.3 & 4.4. A holistic and comprehensive design process was adopted, where the PCB design, circuit element design, and design calculations were performed simultaneously. This approach ensured a seamless integration between the circuitry and the PCB layout, resulting in an optimized hardware design. Each step of the design process involved

meticulous attention to detail, considering factors such as component specifications, performance requirements, and manufacturability. Component selection played a pivotal role in achieving the desired functionality and reliability of the system. Extensive research was conducted, sifting through a vast array of datasheets to identify the most suitable components for each specific application.

4.3. Monitoring Modules Design

Design Outline

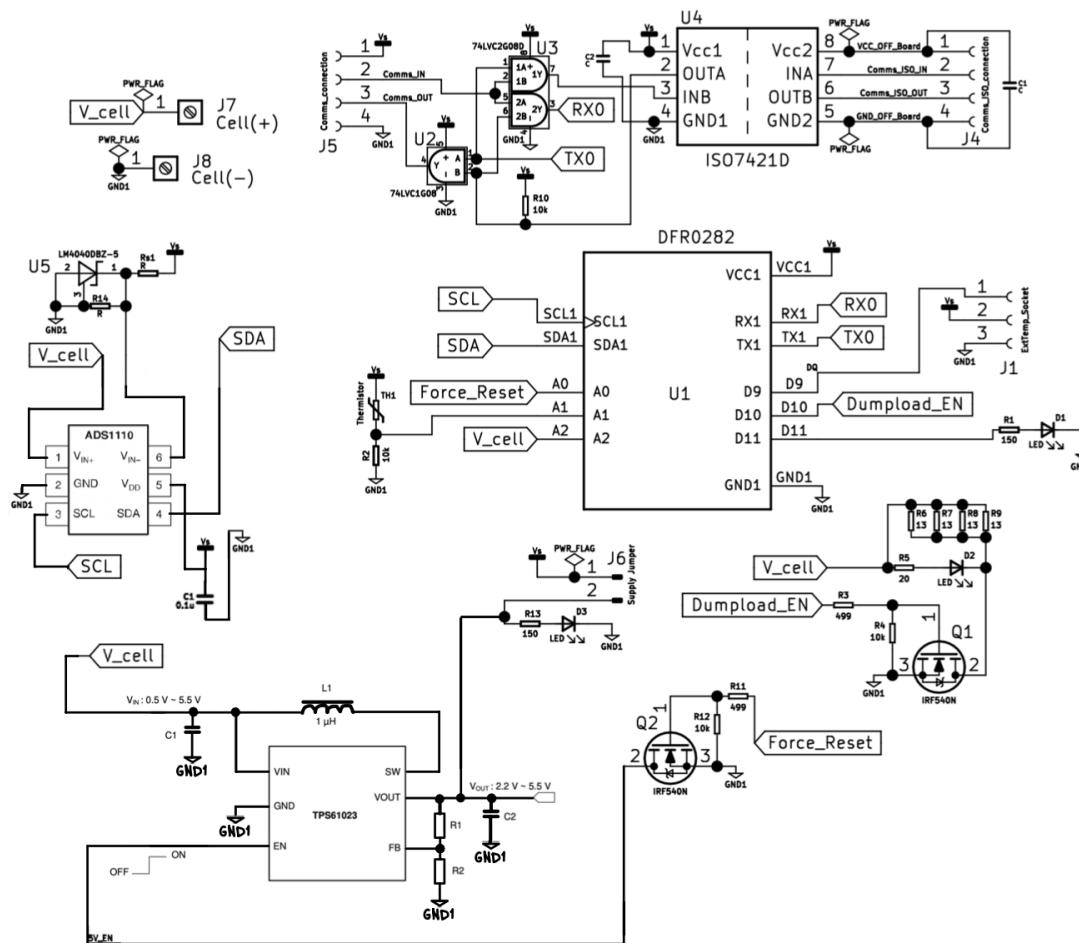


Figure 4.3: Monitoring Module Schematic Diagram

Refer to Figure 4.3 above for the comprehensive schematic of the monitoring system modules. As delineated in the system overview, the design comprises distinct subsystems working in tandem to form a precise measurement and control platform. A thorough examination of each subsystem's circuit design and component selection is presented in the subsequent section. The PCB design further demonstrates the system's adherence to the design requirements to fit on top of a prismatic LFP cell.

Circuit Designs & Component Selection

Cell Connection

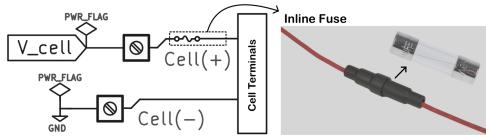


Figure 4.4: Monitoring Mod Terminals and Fuse Protection [5]

A two-pin through-hole PCB connector facilitates cell connection, employing a METZ Connect terminal block rated at 15A to ensure reliable connection beyond peak current demands. The monitoring boards, connecting in parallel to each cell within a series, enable module data acquisition and power draw from the data line, negating external power supply needs. Over-current protection is implemented with a 5mm x 20mm glass fuse, rated at 1.5A, linking the cell's positive terminal to the module, allowing safe 1A discharge by the balancing load during monitoring. While resettable fuses could improve future designs, they are not essential for the current prototype.

Voltage Regulation

To ensure the high precision monitoring system functions optimally, it is crucial to guarantee a stable and accurate power supply to the board. While the system's microcontroller can operate with voltage as low as 3V, it can't reach its full functionality. Hence, the voltage level of the 3.2V LFP cell is insufficient to power the board correctly. The voltage is also fluctuating when the cell is being discharged and the ADC used to measure the cell voltage needs a high precision fixed reference voltage to obtain accurate measurements. For a solution we require a voltage step up to 5V, this will also provide a higher logic level for better resolution in the measurements.

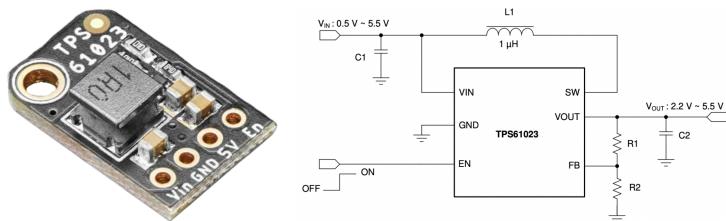


Figure 4.5: MiniBoost 5V [6]

a Mini-booster utilizing a charge-pump topology with the TPS61023 chip from Texas Instruments is used to perform the voltage regulation. The booster can supply up to 1A current at 5V with a 1% precision making it the optimal design chosen for this purpose.

Supply Jumper & Force Reset

A power supply jumper is integrated in the battery cell-based system to safely disconnect it

from the power source during microcontroller programming, as depicted in figure 4.6. This jumper serves a dual purpose: it establishes a "programmer mode" for safe microcontroller programming and enables reconnection to the power source post-programming, ensuring operational flexibility and system protection during firmware updates.

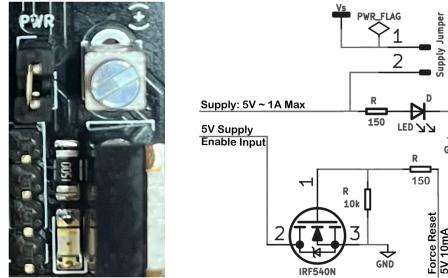


Figure 4.6: Power Supply Connection & Force Reset

An emergency reset circuit is included, utilizing a mosfet as a low-side switch to momentarily ground the enable pin of the TPS61023 chip, thereby initiating a system restart. This force reset functionality is vital for addressing unforeseen microcontroller errors, glitches, or transient faults, enabling a quick system return to a known, stable state without manual intervention.

Monitoring Microcontroller

The DFR0282 microcontroller, chosen for its compact size fitting aptly between cell terminals, facilitates on-the-fly programming alterations via its micro-USB feature. Its compatibility with Arduino Leonardo simplifies rapid code modifications in the Arduino environment, meeting the project's technical requisites efficiently.

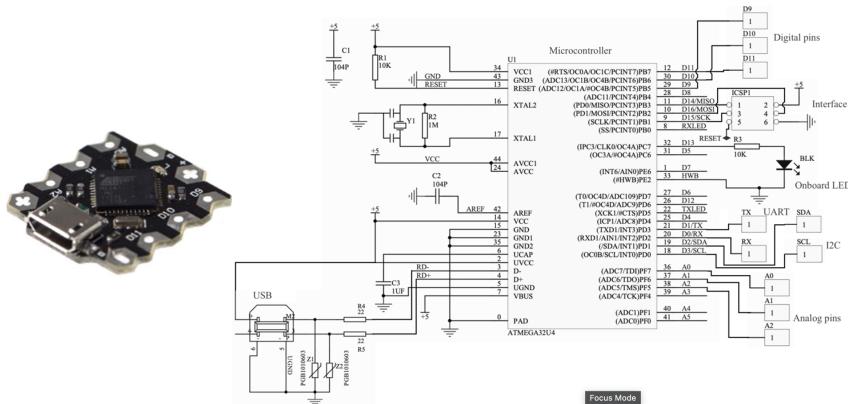


Figure 4.7: DFR0282 - (ATmega32U4) Microcontroller [7]

Equipped with the ATmega32U4 chip and accompanying conditioning circuitry, the DFR0282 module provides six General Purpose Input/Output (GPIO) pins, I2C, and UART pins. This pin configuration aligns with system requirements, ensuring full utilization of available pins for designated functions as detailed in the subsequent table, thereby enhancing the system's functional efficacy.

Table 4.2: Monitoring Microcontroller Pin Out

DFR0282-Pin	Configuration	Utility
0	RX	Serial communication receive channel
1	TX	Serial communication transmit channel
2	SDA	I2C data channel for external ADC
3	SCL	Clock channel for I2C sampling
9	Digital GPIO	External temperature sensor digital input
10	Digital GPIO	Cell balancing dump-load enable pin
11	PWM Channel	LED for system debug messages
A0	Digital GPIO	Force reset enable pin
A1	Analog Channel	Internal temperature sensor analog input
A2	Analog Channel	Cell voltage analog input

Onboard Diagnostics

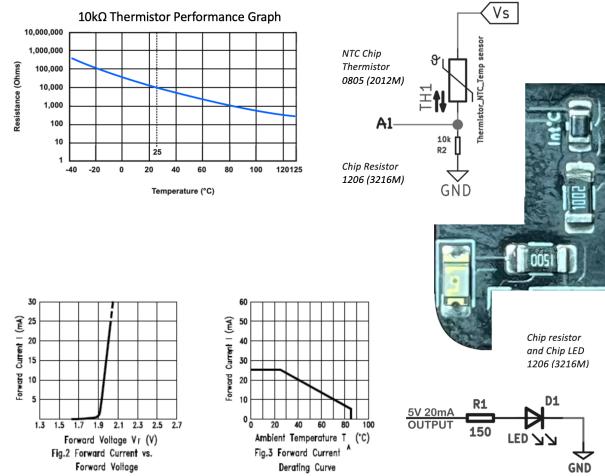


Figure 4.8: NTC Temperature Sensor [8] & Debug LED [9]

Internal Temperature Measurement:

An on-board temperature sensor is crucial for real-time thermal management, ensuring operational safety and optimizing performance. The circuit employs a TE Connectivity Thermistor in a voltage divider configuration with a fixed $10k\Omega$ resistor. The thermistor's resistance (R_{th}) varies with temperature (graph presented in figure 4.8), affecting the voltage (V_{out}) at the microcontroller's analogue input pin as per the following equations.

$$R_{th} = R_0 \cdot \exp \left(\frac{\beta}{T} - \frac{\beta}{T_0} \right) \quad \& \quad V_{out} = 5V \cdot \left(\frac{R_{th}}{R + R_{th}} \right)$$

System Debug LED:

An LED indicator is instrumental for providing immediate, visible feedback regarding system debug messages, aiding in swift diagnosis and rectification of operational issues.

$$R_{limiting} = \frac{V_s - V_f}{I} = \frac{5V - 2V}{0.02A} = 150\Omega$$

Cell Voltage Measurement

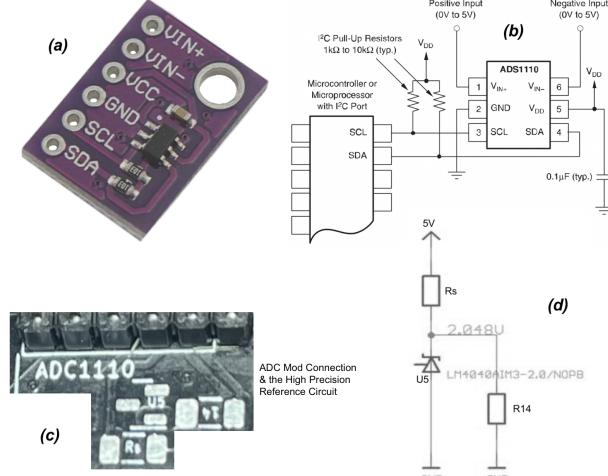


Figure 4.9: (a)16bit ADC (b)ADS1110 Design [10] (c)2.048V Ref. (d)LM4040 Design [11]

Accurate cell voltage measurement is crucial for cell monitoring. While the DFR0282 microcontroller has an onboard 8-bit ADC for backup measurement, a high-precision measurement is achieved using an external 16-bit ADC, the ADS1110. As depicted in figure 4.9(a), the ADS1110 interfaces with the microcontroller via 2K2 pull-up resistors on its I²C lines, operating at a baud rate of 9600. Powered by the microcontroller's 5V and ground lines, the ADS1110, with a sample rate of 240 SPS, offers a resolution of approximately 0.00003125V, as calculated by the formula below.

$$\text{Resolution} = \frac{V_{\text{ref}}}{2^N} = \frac{2.048V}{2^{16 \text{ bits}}} = 31.25\mu$$

A stable external 2.048V reference is essential for maintaining the ADC's precision, as depicted in figure 4.9(c). The circuit, as shown in figure 4.9(d), utilizes the LM4040AIM3-2.0/NOPB shunt voltage reference chip, a 750Ω series resistor (R_s), and a 10 kΩ shunt resistor (R_{sh}). The anode and NC pin of the LM4040AIM3-2.0/NOPB are grounded, while the cathode pin connects to a junction, also connected to R_s and R_{sh} .

$$I_{\text{ref}} = \frac{V_{\text{supply}} - V_{\text{ref}}}{R_s} = \frac{5V - 2.048V}{750 \Omega}$$

The formula above determines the current through the LM4040AIM3-2.0/NOPB chip (I_{ref}), and the total current through R_s is given by the following equation.

$$I_{R_s} = I_{\text{ref}} + I_{sh} = I_{\text{ref}} + \frac{V_{\text{ref}}}{R_{sh}}$$

This design ensures a stable reference voltage across various operating conditions, thus preserving the accuracy of the 16-bit ADC for precise cell voltage measurement.

Cell Balancing

Cell balancing is crucial for managing LFP battery packs where series-connected cells exhibit variations in capacity, internal resistance, and charge characteristics, leading to voltage imbalances that affect battery life and safety. It aims to equalize the SOC across cells. Two prevalent techniques exist: active and passive balancing. Active balancing employs switches and capacitors for charge transfer, presenting efficiency albeit at higher complexity and cost. Conversely, passive balancing dissipates excess charge through resistors, offering simplicity, cost-effectiveness, and reliability, often making it a preferred choice in robust system designs over the marginal efficiency benefits of active balancing.

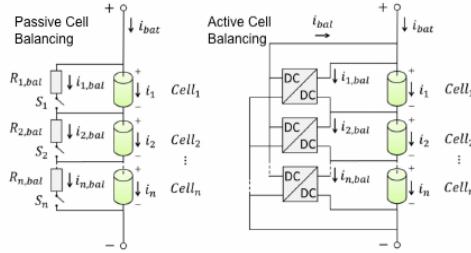


Figure 4.10: Activate vs Passive Balancing [4]

A passive balancing circuit was chosen for the cell modules, with balancing current as a pivotal factor. To ascertain the dump load size for each cell in a 105Ah 3.2V LFP series-connected battery pack, it's necessary to consider both the maximum charging current and the required balancing current for effective balancing. The EVE Energy cell datasheet [45] recommends a maximum charging current of 1C (105A) for the battery pack, thus a balancing current of about 1% of the maximum charging current, or approximately 1A, is deemed suitable for the dump load design per cell.

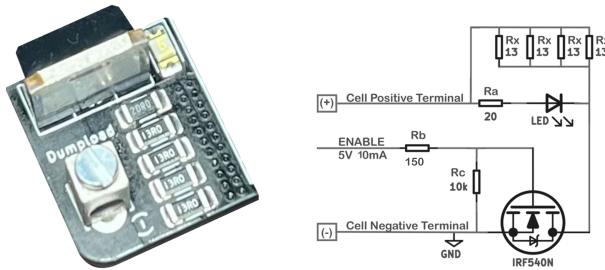


Figure 4.11: Balancing Dump-load Design

The load is made up of four 13Ω chip resistors in parallel.

$$R_{\text{Dump-Load}} = \left(\frac{1}{13\Omega} \cdot 4 \right)^{-1} = 3.25\Omega \quad (4.1)$$

This resistance value results in a balancing current just below 1A.

$$I_{\text{Balancing}} = \frac{3.2V}{3.25\Omega} = 0.985A \quad (4.2)$$

To ensure that the resistors are thermally capable of handling the balancing current we need to look at their power rating.

$$P_{\text{Dump-Load}}(\text{Min.}) = (0.985A)^2 \cdot 3.25\Omega = 3.153W \quad (4.3)$$

Since the resistors are connected in parallel the power rating for the dumpload is given by the equation below.

$$P_{\text{Dump-Load}} = P_{13\Omega-\text{Resistor}} \cdot 4 \quad (4.4)$$

Therefor a high power thin film 13Ω chip resistor from SUSUMU [46], with a power rating of $1W$ was chosen for safe operation of the load.

Low-side Switch:

The dump-load is controlled by a microcontroller with a desire output of $20mA$ on its gpio pins. a High signal of $5V$ on the pin is used to switch a Power Mosfet. The mosfet is used in a low-side switch configuration and has a gate threshold voltage of $2V$. The following calculation was done to select the appropriate gate current limiting resistor [47].

$$R = \frac{\Delta V}{I_{\text{Gate}}} = \frac{5V - 2V}{20mA} = 150\Omega \quad (4.5)$$

A $10k\Omega$ resistor is typically used as a pull-down resistor in a $5V$ system due to its balance of limiting current, reducing power consumption, and ensuring reliable logic level interpretation.

Cell Temperature Measurement

Designed to be positioned at the cell's negative terminal (current entry & exit point), the external temperature sensor, DS18B20, facilitates effective cell thermal monitoring crucial for detecting temperature alterations under heavy loads or charging, thereby enhancing battery safety and efficiency.

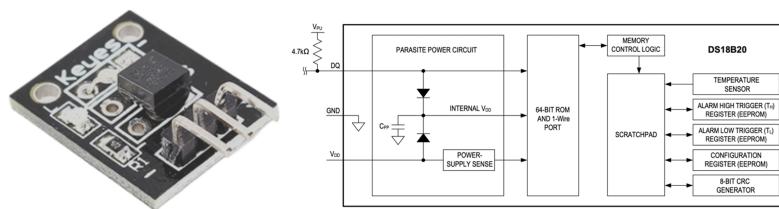


Figure 4.12: External Temperature Sensor [12]

The DS18B20 ensures $\pm 0.5^\circ\text{C}$ accuracy within a -20°C to $+85^\circ\text{C}$ range, extendable to -55°C to $+125^\circ\text{C}$. Operating at $5V$ with a 9 to 12-bit resolution range and "parasite power" capability, the DS18B20 eliminates the need for external power, making it a proficient choice for ambient cell temperature monitoring.

Isolated Module Communication

As delineated in the background study's section 2.5, a comprehensive analysis guided the design choice of the ISO7421D (low-power dual-channel digital isolator chip) from Texas Instruments [48] to isolate UART communication lines. Unlike optocouplers that requires external components for operation, the ISO7421D solely requires two bypass capacitors for supply decoupling. The devised architecture diverges from conventional series-connected isolated daisy-chain or parallel-connected isolated bus lines. Instead, ISO7421D chips are serialized, creating a communication line segmented by isolated barriers, each with two channels: one facilitating data transmission down the stack, and the other, upwards.

This arrangement creates a bidirectional communication bus, wherein between each isolating barrier, signals are either tapped off using a receiver or tapped into the communication line via a transmitter, adhering to an asynchronous serial system protocol. Consequently, all modules along the communication line attain broadcast channel read and write access throughout the system. This configuration mitigates the limitations of common all-call and daisy-chain setups, which encounter scalability constraints due to the elevated output impedance on serial communication, attributed to parallel-arranged digital isolator chips. Such impedance escalation prompts the integration of output drivers to ensure proficient message transmission across the communication line. The novel communication system is illustrated in figure 4.13 below.

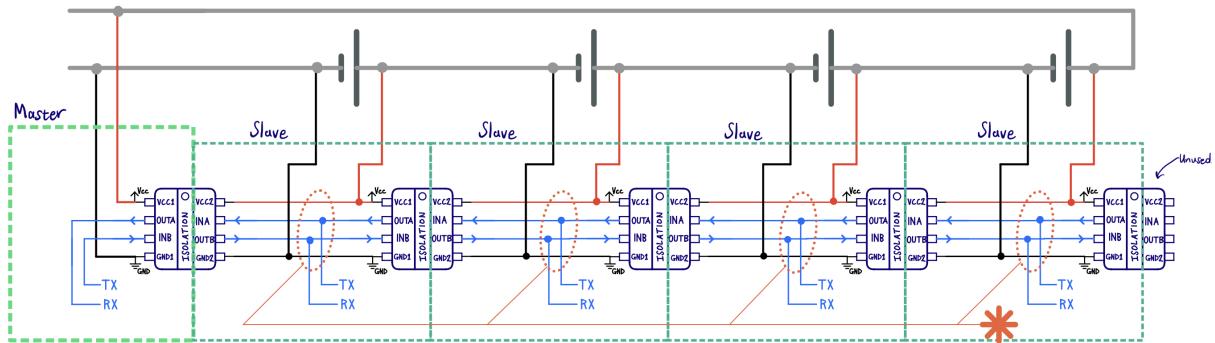


Figure 4.13: Isolated Communication Configuration

The design configuration above may incur bus contention (*) during simultaneous data transmission by multiple transceivers, resulting in signal interference and data corruption. Addressing this issue involves the utilization of an asynchronous software protocol with sequential program timers, which allocates specific time slots for each transceiver to transmit data, thus eliminating overlap and resolving bus contention. To fortify against unforeseen simultaneous data transmission potentially harmful to the system, a communication bit control logic system, employing SN74LVC2G08 AND-gates from Texas Instruments [48], was developed, as depicted in figure 4.14 on the next page.

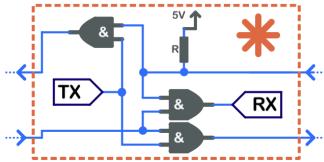


Figure 4.14: Protection Logic Circuit

The final design equipped to each cell monitoring module is presented below in figure 4.15, highlighted pathways represent the data flow of the communication system.

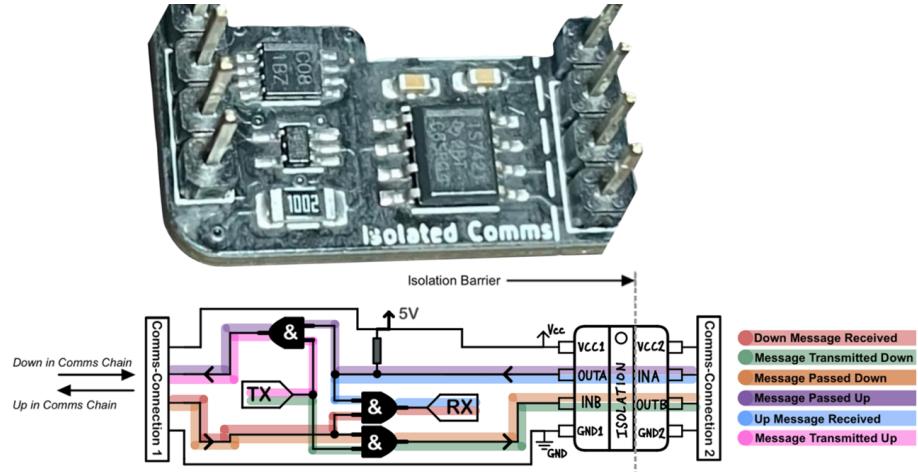


Figure 4.15: Isolated Communication System Design

Printed Circuit Board Design

In the figure below, the left illustrates the PCB design encompassing all copper layers and component footprints selected during the design process of the cell monitoring module. Despite size constraints posing a challenge, the design, as depicted on the right, successfully accommodates a 3D representation of the module between the cell's terminals. Refer to Appendix C for the complete CAD assembly design.

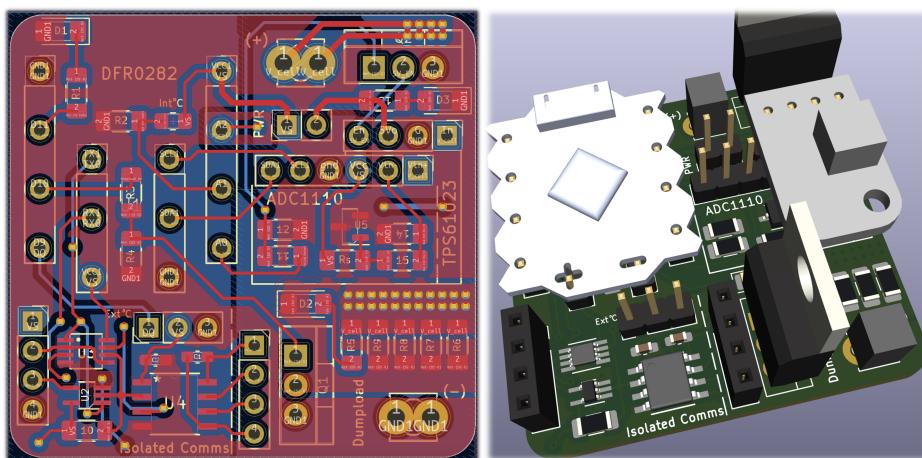


Figure 4.16: KiCad Software Monitoring Module Design [13]

4.4. Master Controller Design

Design Outline

The main controller, serving as the master device in the communication system, solely monitors the current flowing into or out of the battery bank, while other battery parameters are relayed to it. It conducts real-time analysis to determine the connectivity of the battery to the load/charger, processes, and logs the data, primarily aiming to ensure battery safety and manage the state of cells within the battery bank. A meticulous inspection of the circuit design and component selection for each subsystem on the master controller board is delineated in the following section, with the PCB design further substantiating the system's compliance with the design requisites for power line control.

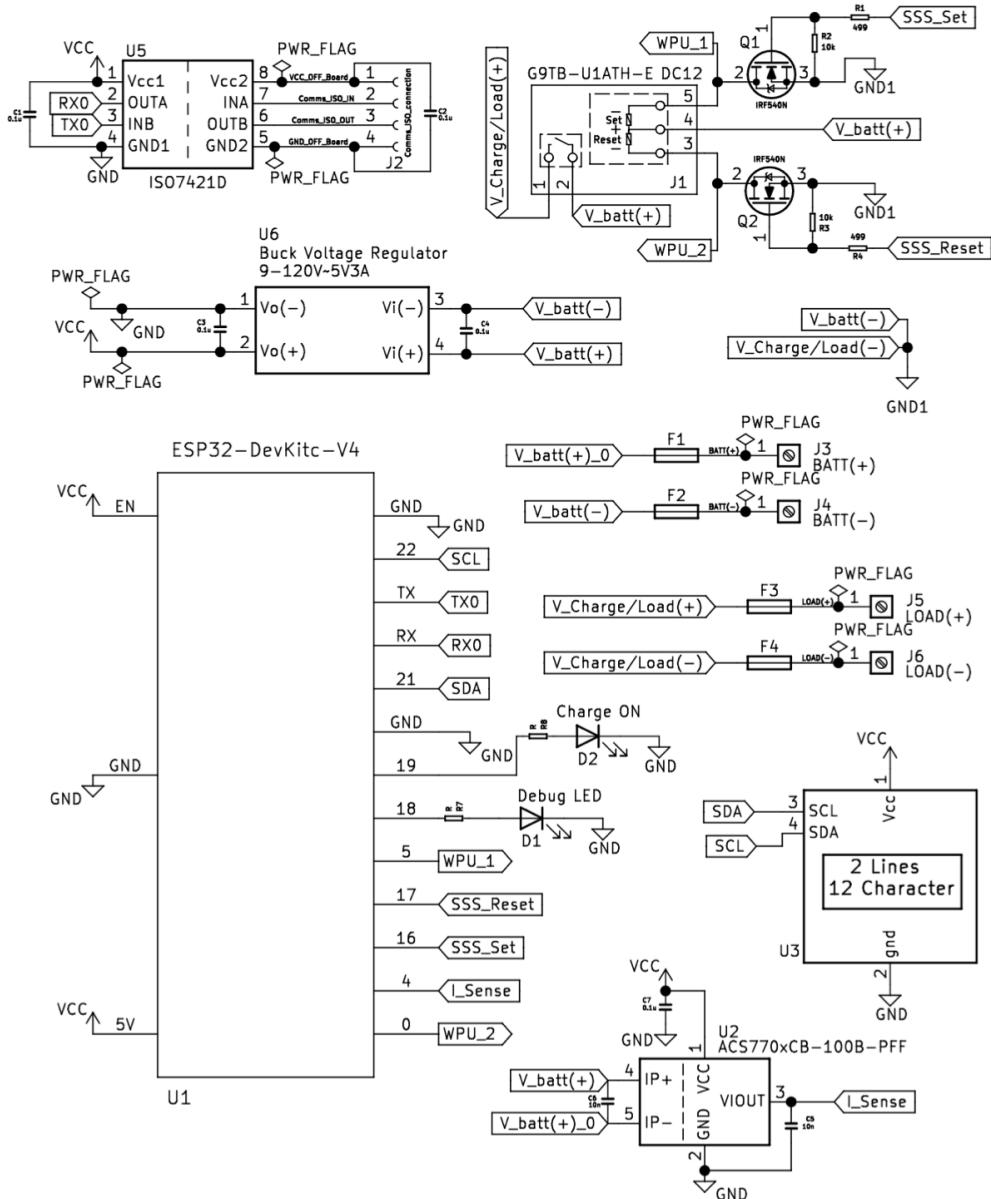


Figure 4.17: Main Controller Schematic Diagram

Circuit Designs & Component Selection

Terminals & Fuse Protection

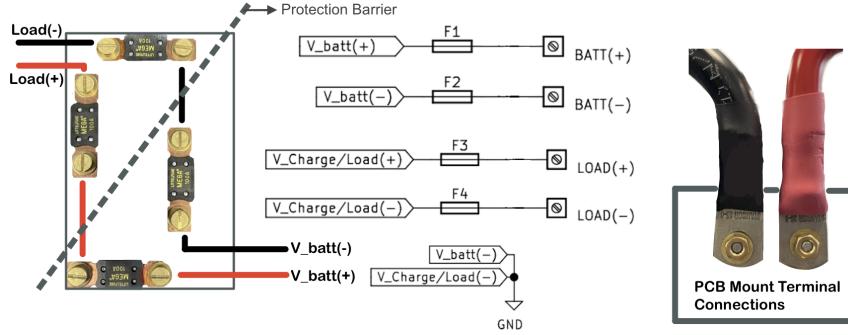


Figure 4.18: Power Line Isolation & Connections [14]

Figure 4.18 illustrates the interconnection of the positive and negative lines of a battery pack and a load/charger via 130A PCB mount through hole screw terminals from Würth Elektronik [49]. To enhance safety, the controller employs 100A fuses [14] on both lines, achieving complete isolation between the battery pack and the load/charger. This dual fusing strategy is essential in high voltage DC systems for mitigating risks associated with insulation failure that could lead to line-to-line DC short-circuit fault conditions. In a controlled setup like this power line control board, such fusing on both sides of the circuit safeguards the system against overcurrent conditions, thereby bolstering the reliability and safety of the control system. The incorporation of 100A fuses on both lines aligns with the best practices in high voltage DC system design, demonstrating a diligent approach to safety and protection.

Power Supply

The choice of employing the Buck Voltage Regulator VIN 9-120V VOUT 5V3A [15] is dictated by the necessity for a stable 5V reference to power the control circuitry on the master board, similar to the monitoring module. For high scalability in the battery pack, this regulator provides a voltage range of 9V to 120V. This regulator not only caters to the maximum current demand of the system but also offers a surplus, ensuring a reliable power supply. The 5V logic level derived from this regulator facilitates a high resolution range, crucial for achieving precision in measurement processing within the system.

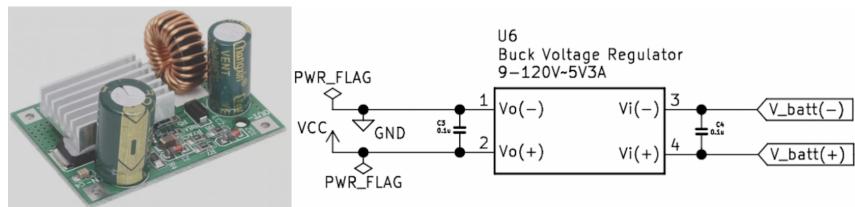


Figure 4.19: Buck Voltage Regulator [15]

Master Microcontroller

The ESP32 DevKitC V4 microcontroller by Espressif [16] is tailored for system controller applications, demonstrating adept handling of UART communication protocols for real-time interaction with slave monitoring devices. It processes data from series string cells efficiently and uploads it to the cloud via integrated Wi-Fi functionality, enabling real-time monitoring and system analysis.

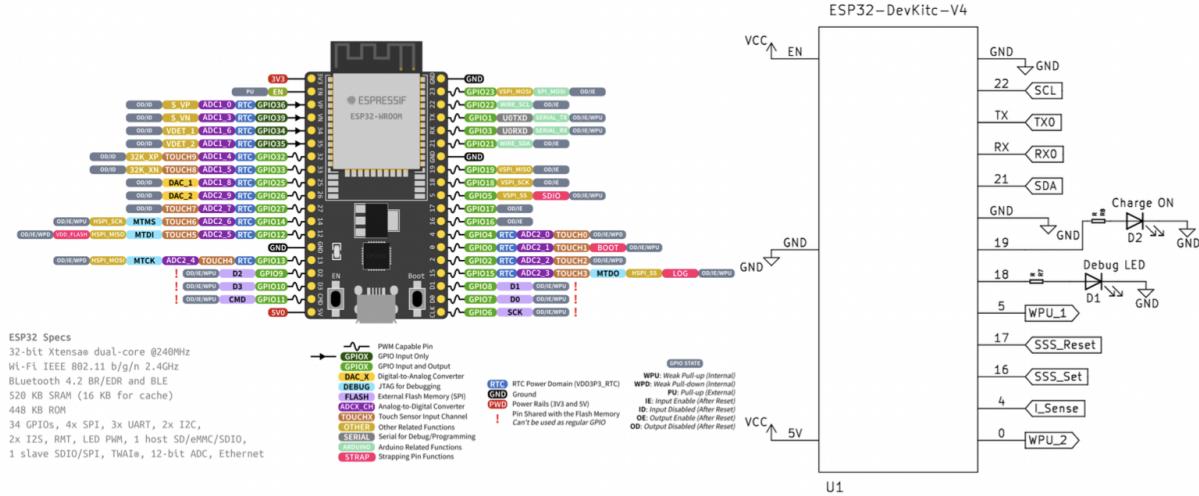


Figure 4.20: ESP32DevKitCv4 Master Microcontroller [16]

This microcontroller is cost-effective compared to alternatives like the Raspberry Pi, yet provides a rich feature set. The on-board Wi-Fi ensures real-time data transmission and remote monitoring. Its compatibility with Arduino IDE facilitates effortless interfacing with DFR0282 slave modules for cell monitoring, simplifying development and accelerating deployment of monitoring and control logic. The ESP32 DevKitC V4 is mounted on the master controller board, featuring an on-board micro-USB port for program updates. Below is a table detailing the pin configurations and utilities on the master controller board.

Table 4.3: Master Microcontroller Pin Out

ESP32-Pin	Name	Configuration	Utility
3	IO22	Arduino Wire-Lib SCL	I2C clock for LCD
4	TX	UART Protocol	Serial transmit channel
5	RX	UART Protocol	Serial receive channel
6	IO21	Arduino Wire-Lib SDA	I2C data for LCD
8	IO19	Digital Output	Charge/Load ON indication
9	IO18	PWM Channel	System debug messages LED
10	IO5	GPIO State	Internal weak pull-up 1
11	IO17	Digital Pulse	Lacthing relay RESET
12	IO16	Digital Pulse	Lacthing relay SET
13	IO4	Analog Channel	Current sensor input
14	IO0	GPIO State	Internal weak pull-up 2

Battery Current Measurement

The ACS770LCB-100B current sensor from Allegro Microsystems [17] is utilized to measure the current flowing from the battery's positive terminal to the load/charger. Accompanying the sensor are a $0.1\mu F$ decoupling capacitor between its 5V supply lines, a $10nF$ bypass capacitor at its output, and another $10nF$ capacitor between the current path's positive and negative terminals for noise mitigation. The sensor's output delivers a voltage signal representative of the battery pack's current to the microcontroller, within a measurement range of -100A to 100A and a corresponding output voltage range of 0V to 5V.

The linear transfer characteristic of the sensor is given by the formula below.

$$V_{out} = V_{zero} + (S \cdot I)$$

Where $V_{zero} = 2.5V$ (sensor output at zero current) and S the sensitivity, is calculated.

$$S = \frac{5V}{200A} = 0.025 \text{ V/A}$$

The accuracy of the measurement is evaluated considering a sensor accuracy specification of 0.5%. For a measured current of 50A, the error and its corresponding voltage error are calculated as follows:

$$\text{Error} = 0.5\% \cdot 50A = 0.25A \quad (4.6)$$

$$V_{error} = 0.025 \text{ V/A} \cdot 0.25A = 0.00625V \quad (4.7)$$

Table 4.4: Sensor Voltage Output for Various Current Values

Current (I)	Expression	Output Voltage (V_{out})
50A	$2.5V + (0.025 \text{ V/A} \cdot 50A)$	3.75V
-50A	$2.5V + (0.025 \text{ V/A} \cdot -50A)$	1.25V
100A	$2.5V + (0.025 \text{ V/A} \cdot 100A)$	5V

The design, shown in figure 4.21, leverages the ACS770LCB-100B to translate battery current to a voltage signal for microcontroller interpretation, with capacitors employed for noise suppression, thus bolstering system reliability and measurement accuracy.

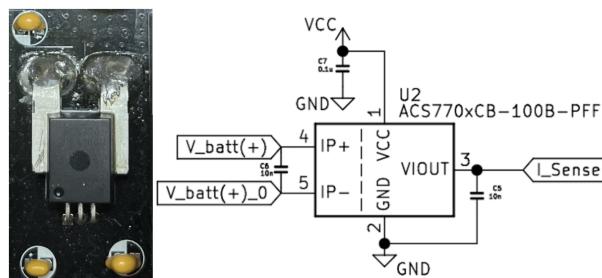


Figure 4.21: Battery Current Sensor [17]

System Information Display

The generic LCD 16x2 Character Display, White on Blue Background, 5V, along with the I2C Interface Module for LCD, 3.3/5V Ready, from Microrobotics [18], are integrated on the control board. This setup facilitates communication between the microcontroller and the LCD via the I2C protocol. The I2C Interface Module simplifies the connection requiring only four wires: VCC, GND, SDA, and SCL. Through this setup, the microcontroller can dispatch summarized system messages to the LCD, providing a succinct insight into the state of system variables, ensuring a user-friendly interface for real-time system monitoring.

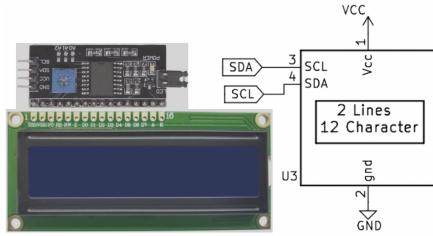


Figure 4.22: LCD with I2C Module [18]

Load/Charge Disconnect

The Omron G9TB-K1ATH-E DC12 relay, positioned in series between the battery pack and the load/charger, serves as a switch for power flow, safeguarded by fuse protection on both sides for a maximum current of 100A.

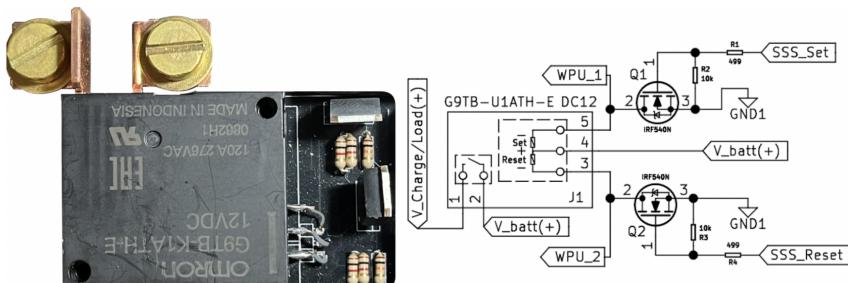


Figure 4.23: Latching Power Relay [19]

The relay requires a 12V amplitude pulse for state transition, yet the ESP32 microcontroller outputs a maximum amplitude pulse of 5V. To bridge this voltage gap, external circuitry, depicted in figure 4.23, is designed. Two identical MOSFETs from the dump-load circuits of the cell monitoring modules are integrated in low-side switch configurations, simplifying the design for gate limiting and pull-down resistors as per subsubsection 4.3.

The gates of these MOSFETs are connected to distinct microcontroller pins labeled SET and RESET, enabling a 25ms pulse for the relay's operation. The common pin of the relay coils is tied to the positive battery voltage (12V), while the set and reset pins on the relay are linked to a MOSFET's drain pin and an internal pull-up pin of the microcontroller, ensuring the relay pins float high when MOSFETs are non-conductive.

The source pins of each MOSFET are connected to the negative battery voltage (0V), enabling a 12V potential across the relay's set or reset coil upon a 5V, 25ms pulse from the microcontroller. A hardcoded protocol in the microcontroller ensures that SET and RESET pins are not pulsed concurrently, preventing erroneous relay actuations.

Scalable Isolated Communication

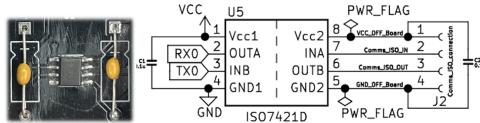


Figure 4.24: Master Controller Isolated Communication

The master controller's communication lines are isolated using the ISO7421D chip, identical to the one used in the cell monitoring modules as referenced in subsubsection 4.3. Being at the start of the communication line, the master device is shielded against bus contention by the logic circuit on the first slave device in the stack.

Printed Circuit Board Design

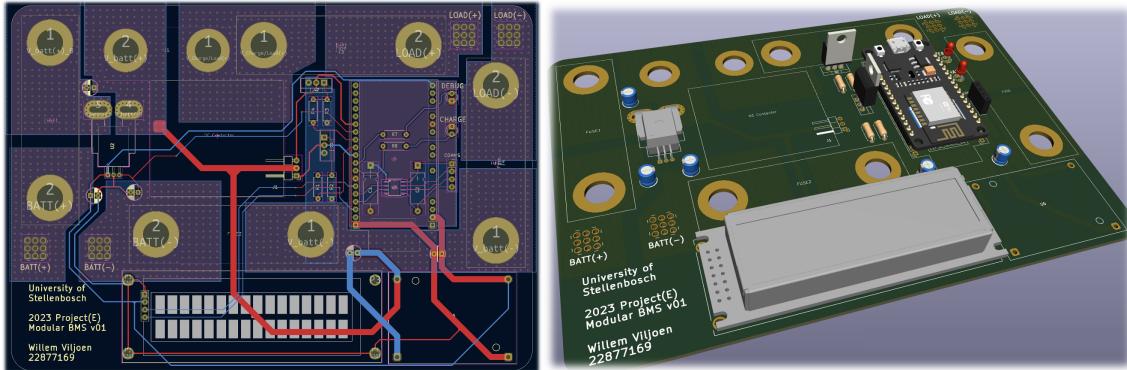


Figure 4.25: KiCad Software Master Controller Design

In the figure above, the left illustrates the PCB design, showcasing all copper layers and component footprints selected during the design process of the master controller board. To accommodate a high current of 120A on the battery power lines flowing through the master controller board, filled copper layers and via stitching techniques were employed. These design approaches enhance the current-carrying capacity and thermal management of the PCB. A thermal test for the current capability of the master controller board is slated for evaluation in Section 5.4. As depicted on the right, the design successfully integrates a 3D representation of the board, fitting perfectly to the side of the first cell in the series stack at the battery bank's input/output. Refer to Appendix C for the complete CAD assembly design.

4.5. Design Review

The diagram below succinctly illustrates the system solution for a *Modular Battery Management System for LFP Batteries*, showcasing the independent yet compatible monitoring modules and the master controller. These units, while autonomous, are interconnected through a communication network to form a cohesive BMS ecosystem for a battery bank. The design underscores the synergy between the controller, cell modules, and communication system, functioning both individually and collectively to ensure system integrity.

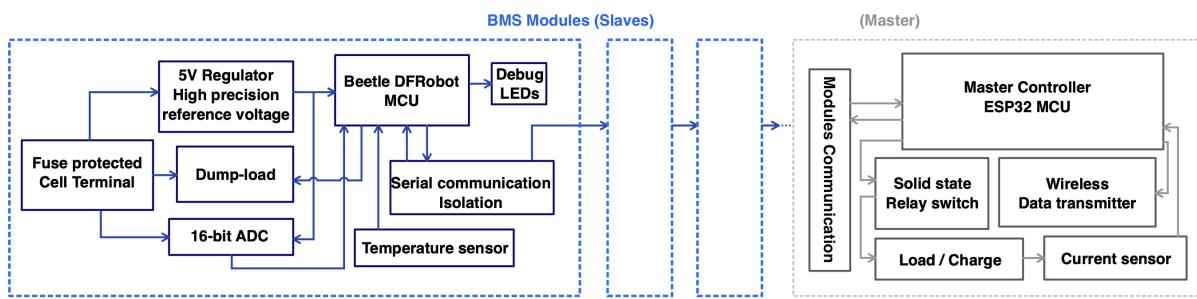


Figure 4.26: Complete System Design

The modular BMS topology features cell-level monitoring modules and a central controller, marking a significant evolution in energy management. It achieves precise, real-time data collection and enhances system-wide awareness. Embedded microcontrollers within each module process data locally, reducing latency and improving accuracy, which simplifies the system's complexity and improves reliability.

The central controller is pivotal, managing data flow and system communications with a focus on power control and resilient PCB design. It synthesizes cell data, supporting informed energy management decisions. In sum, the BMS melds modular design with centralized oversight, offering scalability and adaptability to meet evolving battery management needs, and is poised to set new industry benchmarks.

Design Tools Acknowledgment:

The subsequent figure presents a curated selection of icons representing the sophisticated design and development software applications instrumental to the engineering and design processes of this project.

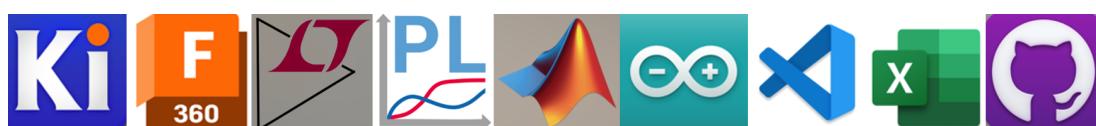


Figure 4.27: Design Software Packages

Chapter 5: System Evaluation

5.1. Design Outcomes

The design review, constrained by the timing of PCB and component procurement and subsequent prototyping, served primarily as a reference for future enhancements rather than immediate project revisions, aligning with the limitations outlined in the Hypotheses & Potential Drawbacks section. The prototype and debugging phases surfaced several design outcomes, including both the successful implementation of subsystem designs and an identified critical flaw: the malfunction of the UART communication between cell monitoring modules.

The communication issue originated from the complex hardware interactions within the Arduino Beetle (DFR0282) microcontrollers, particularly affecting the hybrid daisy-chain serial communication setup. The challenges included maintaining a stable 16 MHz clock for precise UART timing, implementing effective flow control, and ensuring accurate pin configuration. These factors, both individually and collectively, compromised the UART system, as further detailed through exhaustive debugging and analysis.

Despite this setback, the communication hardware was independently verified as functional, isolating the issue to the microcontrollers used. All other systems and subsystems performed optimally and will be discussed in this chapter. Chapter 6 will propose future actions for multi-module communication and alternative microcontroller recommendations for the cell monitoring boards.

5.2. Valuation Prospect

This chapter presents a thorough evaluation of the designed modular Battery Management System, ensuring subsystem compliance with key performance and safety standards. We will conduct exhaustive testing of each subsystem in simulated operational environments to verify performance within optimal thresholds. Tests include electrical, thermal, and fault response assessments to establish reliability, state-of-charge accuracy, and overall system integrity. Additionally, we will analyze performance under variable load conditions to evaluate module adaptability and robustness. Our systematic evaluation aims to provide a detailed understanding of subsystem operation and integration within the BMS, guaranteeing cohesive operation, battery longevity, and user safety upon final assembly. This strategy underpins the BMS's integrative success by confirming the efficacy of individual subsystems.

5.3. Prototyping

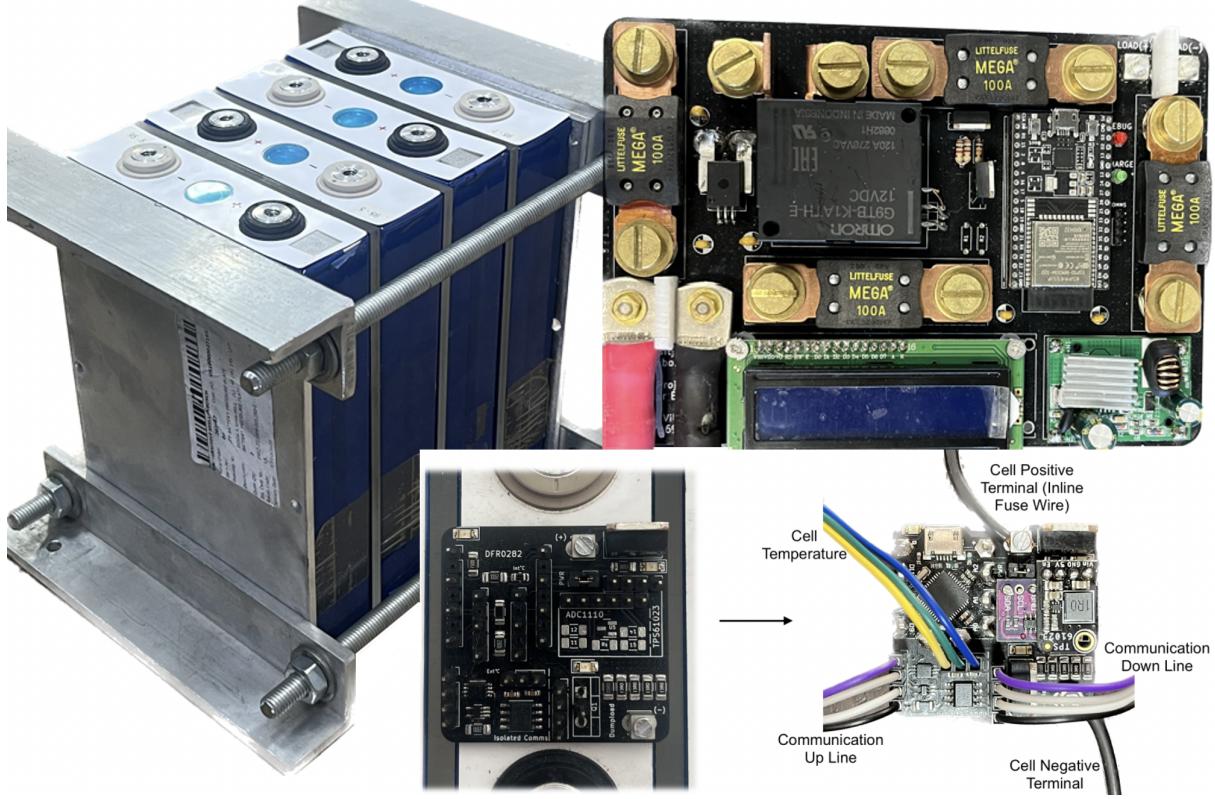


Figure 5.1: Design & Evaluation Prototype Builds

The provided figures showcase a constructed battery pack for experimental testing (left), an engineered main controller (top right), and a cell monitoring module prototype (bottom right). The assembly uses 100Ah 3.2V LFP cells, secured by corner profiles, threaded rods, and aluminium end plates, which, along with Perspex spacers, enforce cell compression to mitigate expansion and maintain cell integrity during discharge cycles. This technique safeguards against delamination from mechanical stress, essential for LFP cell performance. The main controller is optimized for current handling, while the monitoring modules focus on precision and compact design, serving to assess the performance of the Modular BMS systems in the project.

5.4. Performance analysis

This section elaborates on the experimental procedures conducted to assess the performance of the engineered system and its component subsystems under controlled conditions. It encompasses a description of individual tests and includes accompanying subsections that present flow diagrams, result graphs, and model configurations for a comprehensive analysis.

General

The master controller and cell monitoring modules were assessed for functionality using flag-based test programs, which confirmed the onboard Debug LED system operated as intended. Calibration of the NTC sensor on the cell monitoring modules was achieved by referencing an external digital temperature sensor for internal temperature measurements. Validation of these measurements was conducted against the precise readings from a Fluke TiS20 thermal tool. Additionally, an emergency restart test was successfully executed on the cell monitoring module by transmitting a UART force reset flag, causing a momentary power loss in the microcontroller before a successful reboot.

Communication Circuitry

The isolated communication system was tested utilizing an ESP32 microcontroller, wherein four GPIO pins were configured as digital outputs to simulate UART transmission (TX) for distinct cell monitoring modules. Correspondingly, four digital input pins on the ESP32 were employed to represent the reception (RX) points within the communication network, ensuring bi-directional connectivity between the microcontroller and each monitoring module's communication subsystem.

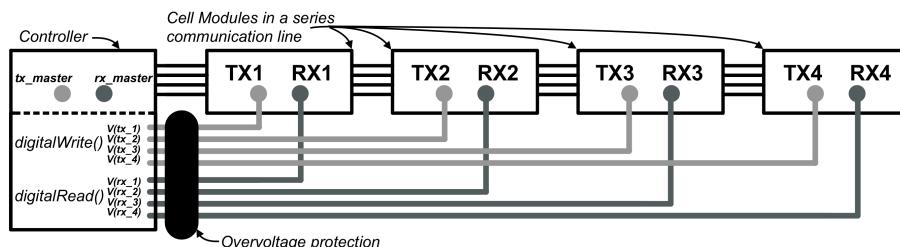


Figure 5.2: Communication System Test Setup

Figure 5.3 on the next page displays a serial plotter graphing both transmitted and received pulse signals. Over-voltage protection modules safeguarded the ESP32's GPIO pins, with a threshold set slightly above 5V, to mitigate bus contention risks, which didn't occur. Thus, the monitoring modules' communication circuitry operated effectively, incorporating protection logic gates that successfully prevented bus contention. This was confirmed during tests where simultaneous pulsing of two transmit pins (tx2 and tx3) occurred between 40ms and 70ms, with the received signal voltage capped at 5V. This scenario resulted in message corruption but precluded hardware damage, demonstrating the isolated communication system's resilience to potential malfunctions.

It is important to note that the logic gates also serve the purpose of eliminating transmission-echo in the communication system, as we can see on the graphs now RX receives a signal transmitted from its corresponding TX. Overall, the communication circuitry integrated into each cell monitoring module functioned as expected.

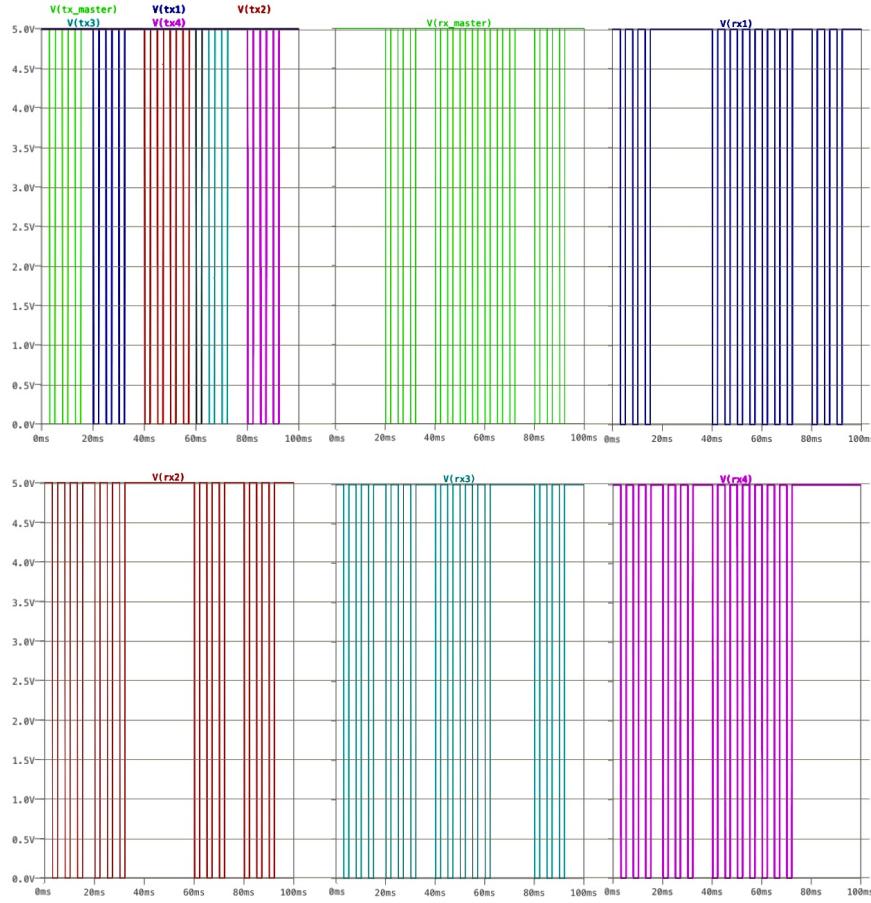


Figure 5.3: UART Representative Logic Pulses Measured by ESP32

UART, Voltage measurement & Cell Balancing

These three monitoring module functions were validated using a test program, as illustrated in the subsequent flow diagram. The module received UART messages while concurrently measuring the cell's live voltage through its microcontroller. This integration enabled the system to activate the balancing dump-load, aligning the cell's discharge to the specified voltage level in comparison with the ADC voltage readings.

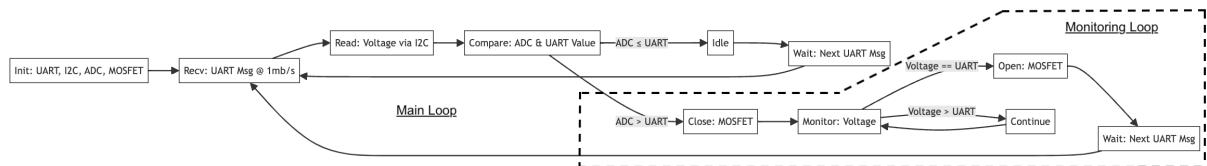


Figure 5.4: Cell Balancing Test Code Program Flow

The test conducted on the monitoring module affirmed that the system performed in accordance with expectations. The behavior of the system aligned precisely with anticipated outcomes. The ADC provided measurements with a high degree of accuracy, and upon activation, the dump-load circuitry effectively operated at a current of 1A, successfully maintaining the cell voltage at the correct levels throughout the duration of the experiment.

Controller Current Capability

With assistance from Mr. Petzer, we conducted an experiment using a high-capacity DC power supply and a low-impedance, high-power resistive load. The setup involved connecting the power supply to the main controller board's battery terminals, and the load to the load/charger terminals. The DC isolator successfully separated the power supply side from the load side upon initiation. Engaging the main controller board's relay allowed for a significant 100A current flow. Thermal behavior under these conditions was observed with a Fluke TiS20 thermal camera, as shown in Figure 5.5.

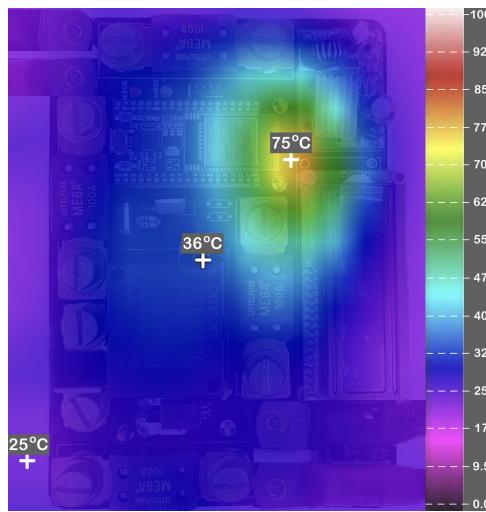


Figure 5.5: Thermal Imaging with Fluke TiS20

The thermal image verifies the controller's adequacy in managing the current for both battery and load/charger applications, with a single expected hotspot identified. This hotspot aligns with a known design limitation of the PCB, where a routing constraint for the negative terminal fuses impacted the thermal layout. The current single-sided filled zone with non-connecting vias was a result of this constraint, which was acceptable for the current application. For future enhancements, it is recommended to redesign the PCB to include dual-sided filled zones with via stitching to improve thermal management for high-current operations.

Pulsed Cell Discharge

The experiment assessed a single 3.2V 100Ah cell's discharge characteristics by connecting it to a $90m\Omega$ load through the main controller, inducing a 35A discharge at 0.33C. The controller executed 17 switch cycles of the DC power relay with a 10-minute pulse width and 25% duty cycle, to minimize temperature fluctuations and maintain cell stability. Cell voltage and current were meticulously recorded by the monitoring module and logged serially. The collected data was graphically represented to analyze the discharge behavior, as illustrated in Figure 5.6.

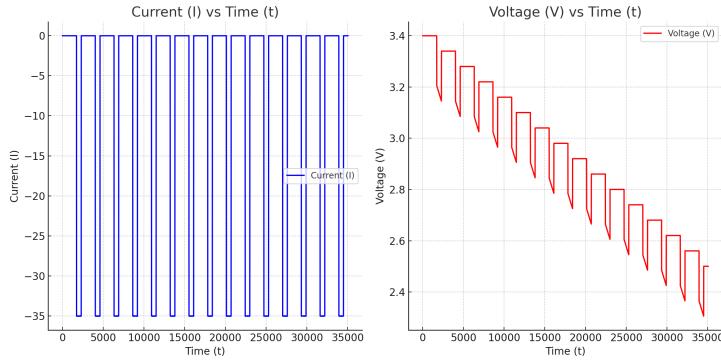


Figure 5.6: 100Ah 3.2V LFP cell - Pulsed Discharge Current & Voltage Measured

The graphical data from above was imported into MATLAB and analyzed using Javier Gazzarri's battery parameterization model in Simulink [20]. This facilitated dynamic battery analysis from pulsed discharge data. A modular Battery Management System (BMS) was then developed and simulated in Simulink, utilizing derived parameters to assess system performance. Figure 5.7 illustrates the Simulink models and corresponding simulation results. This methodology provided a detailed system evaluation, closely replicating actual battery cell behavior, and confirmed the BMS's operational effectiveness, underscoring Simulink's value in battery system analysis and design.

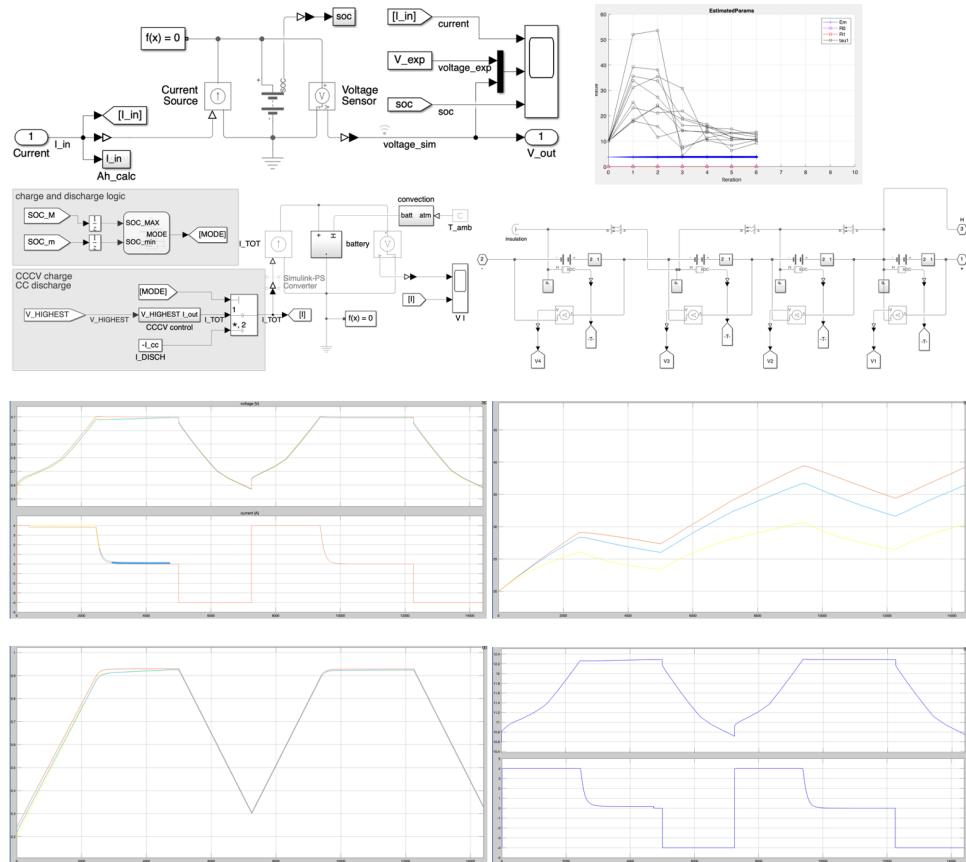


Figure 5.7: Simulink Battery Modeling & Simulated Results [20]

Chapter 6: Conclusion

6.1. Retrospective Overview

The crux of a modular BMS is its three core components: the Main Controller's power rating, linking the battery pack with external power lines, the scalable monitoring offered by Cell Modules, and the Module Communication System. Together, they form the heartbeat of the BMS, each playing a pivotal role in the system's overall performance and adaptability. The Main Controller has proven pivotal in integrating energy storage systems with power infrastructures. Cell Modules have brought unparalleled scalability, adapting to diverse energy demands. The Communication System has acted as the crucial link, ensuring cohesive operation and real-time responsiveness.

6.2. Recommendations and Forward Look

Future Work: Moving forward, design iterations are essential to reinforce the BMS's robustness and establish a fundamental communication system. The encountered UART communication issues underscore the need for a protocol that scales with the increasing number of microcontrollers. Future enhancements should focus on a scalable protocol, improved user interfaces for diagnostics, and sophisticated algorithms for charge balancing and health assessments, to drive the BMS towards technological and user-centric excellence.

6.3. Denouement

Iterative design methodology is key to achieving a communication system capable of supporting the highest number of cell module microcontrollers. Calculating the power ratings for extensive cell networks and designing a controller for series string disconnect/connect are crucial steps. The design, boxed in unit cell string modules, must be fortified at every layer—starting from the main controllers to the high voltage pinnacle. Each iterative layer adds to the robustness of the foundation, making the cell monitoring module integral in a Modular Battery Management System for LFP Batteries, paving the way for an energy-resilient future.

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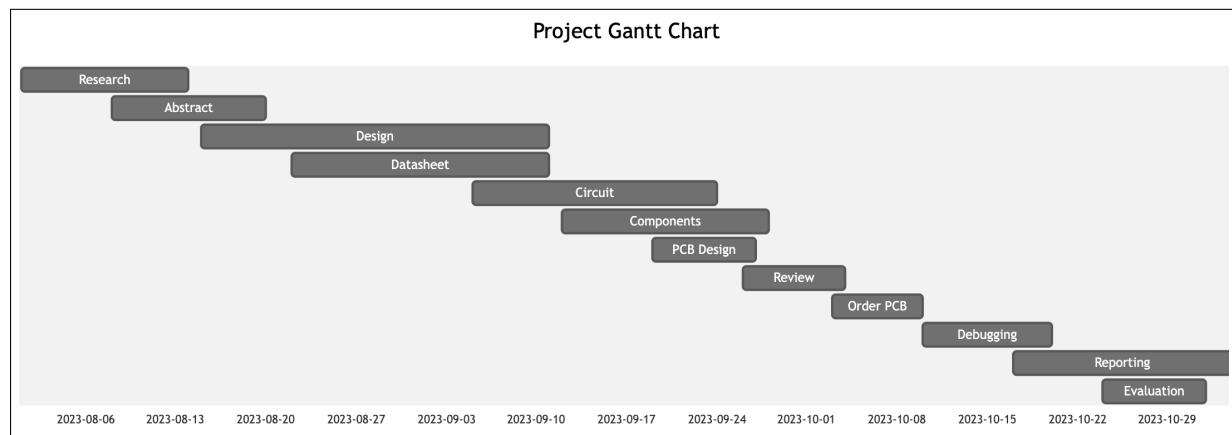
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Project Planning Schedule

Week	Work Planned to Start	Gantt Chart Ref.
1	Conduct Detailed Research on BMS Topology	Research
2	Draft Abstract Report	Abstract
3	Initiate System Design Process	Design
4	Conduct Extensive Datasheet Consultations	Datasheet
5	Execute Circuit Designs	Circuit
6	Source Components & Initiate Ordering Process	Components
7	Engage in Printed Circuit Board Design Process	PCB Design
8	Review & Revise Circuit and PCB Designs	Review
9	Place Order for Printed Circuit Board	Order PCB
10	Solder Components & Conduct Module Debugging	Debugging
11	Design Reporting & System Analysis Testing	Reporting
12	Evaluation & Conclusion Reporting	Evaluation

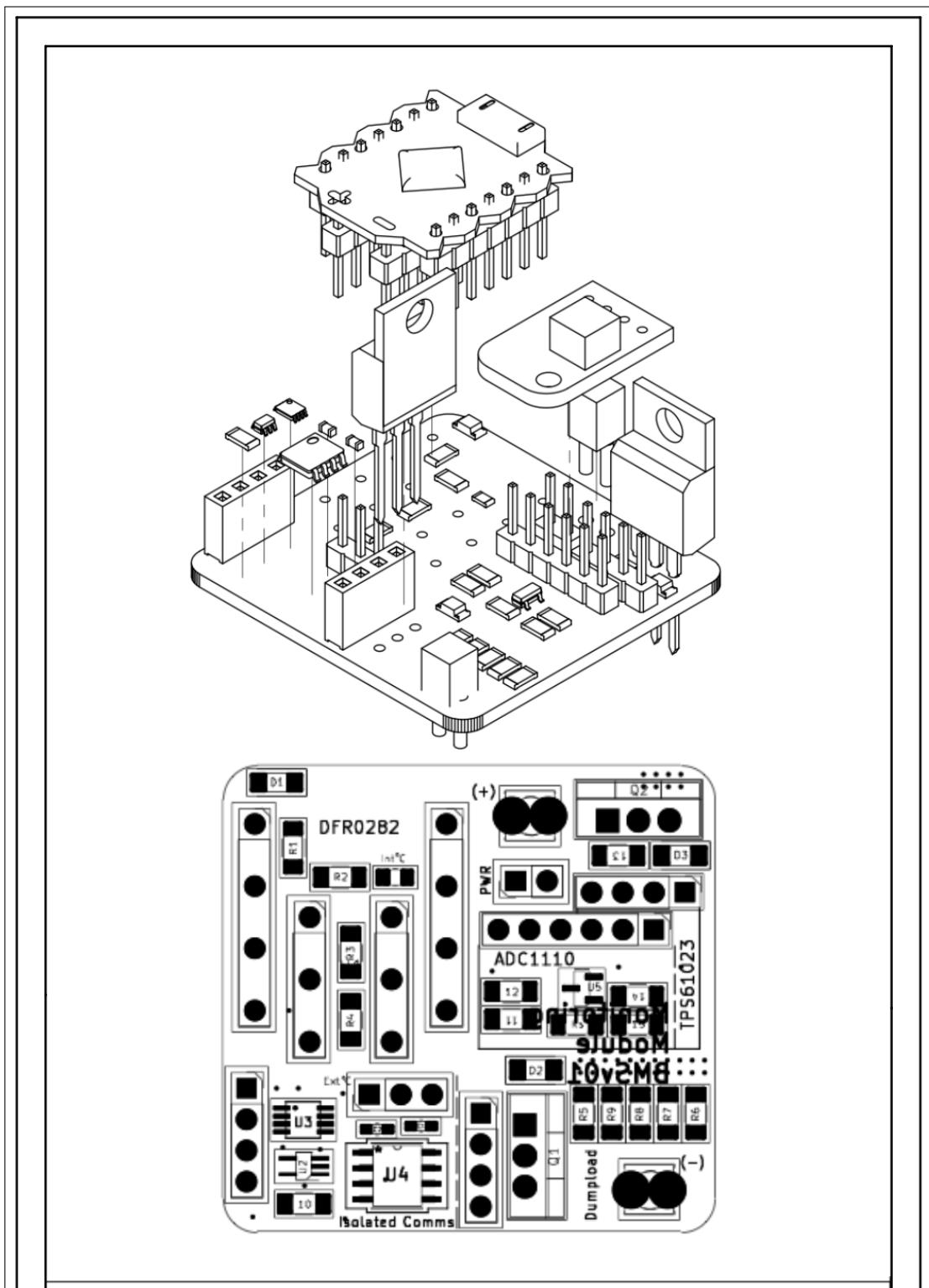


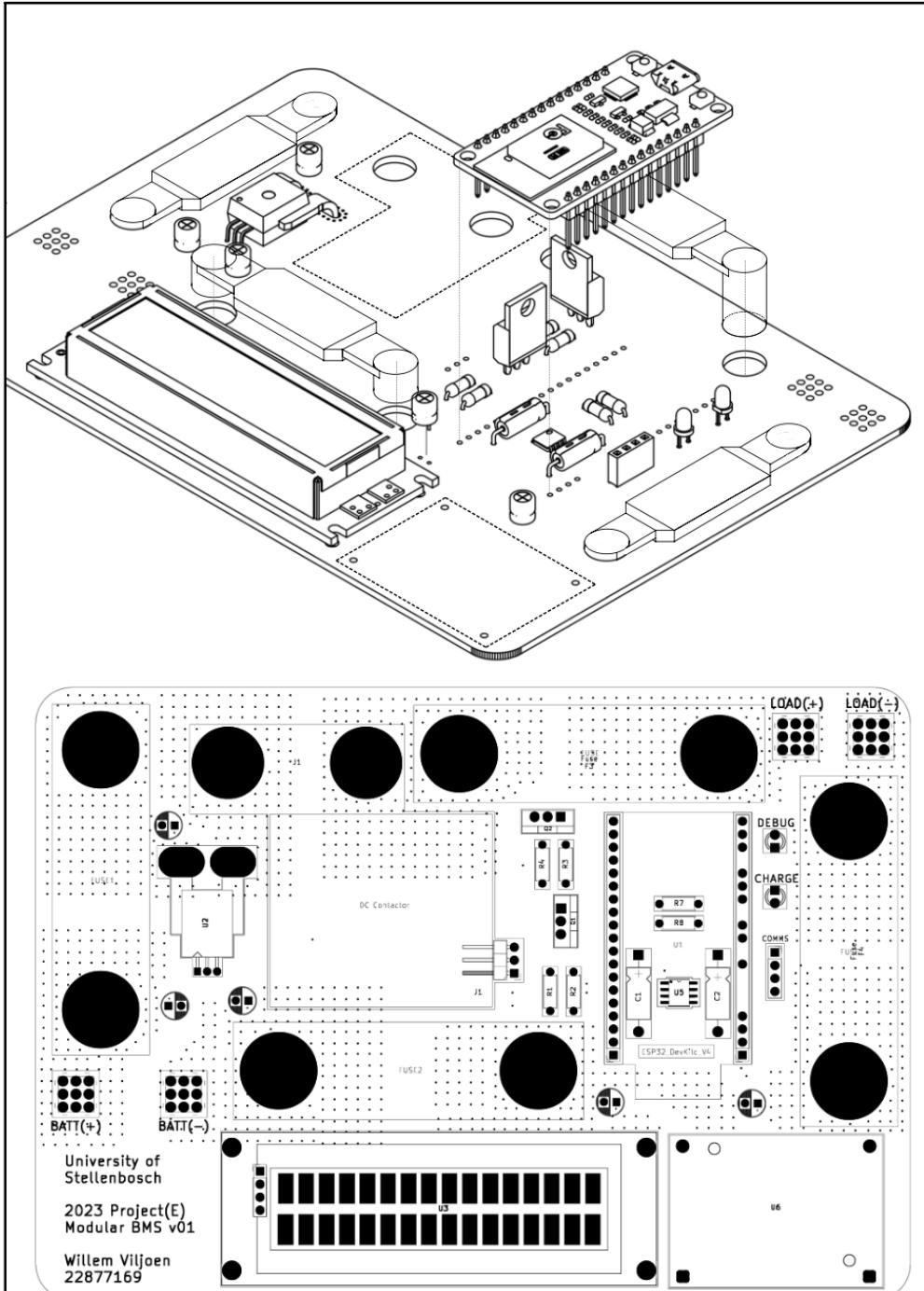
Outcomes Compliance

Table B.1: ECSA expected learning outcomes (ELO): Descriptions and chapters

ECSA Outcome	Ch.	Motivation
ELO 1. Problem solving: Identify, formulate, analyse and solve complex engineering problems creatively and innovatively.	1, 3, 4, 5	Chapters 1 and 3 introduce and conceptualize the problem, Chapter 4 details the design process, and Chapter 5 discusses problem resolution through system evaluation.
ELO 2. Application of scientific and engineering knowledge: Apply knowledge of mathematics, natural sciences, engineering fundamentals and an engineering specialty to solve complex engineering problems.	All	Every chapter contributes to applying scientific and engineering knowledge to develop and refine the BMS.
ELO 3. Engineering Design: Perform creative, procedural and nonprocedural design and synthesis of components, systems, engineering works, products or processes.	3, 4	Chapter 3 sets the design requirements, while Chapter 4 provides an in-depth look at the creative and procedural design process.
ELO 4. Investigations, experiments and data analysis: Demonstrate competence to design and conduct investigations and experiments.	5	Chapter 5 is dedicated to the evaluation of the system, which includes conducting experiments and analyzing data.
ELO 5. Engineering methods, skills and tools, including Information Technology: Demonstrate competence to use appropriate engineering methods, skills and tools, including those based on information technology.	All	The integration of engineering methods, skills, and IT tools is evident throughout the report.
ELO 6. Professional and technical communication: Demonstrate competence to communicate effectively, both orally and in writing, with engineering audiences and the community at large.	6	The conclusion chapter demonstrates the ability to communicate the project's findings and implications effectively.
ELO 8. Individual work: Demonstrate competence to work effectively as an individual.	All	The report, as a whole, is indicative of the author's ability to work independently on a complex engineering project.
ELO 9. Independent Learning Ability: Demonstrate competence to engage in independent learning through well-developed learning skills.	All	The successful completion of the report showcases the author's independent learning abilities throughout the project.

PCB Cad Assemblies





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Sheet:

Monitoring Board & Mstr Controller Board

Title: BMS Skripsi Master Controller Board

Size: A4	Date:	Rev: v01
KiCad E.D.A. kicad (7.0.0-0)		Id: 1/1

Bill of Materials

Modules	Label or Nickname	Product Name or Code	Detailed Description	Unit Cost	Quantity	Function	Socket
1	Arduino Beetle Board	DFRobot0282	ATmega32U4 Beetle AVR® ATmega AVR MCU 8-Bit Embedded Evaluation Board	R 194.64	4	BMS monitoring module MCU.	J1, J2, J3, J4 1x7pin, 1x5pin, 1x5pin, 1x7pin
2	TPS61023 5V Mini-Booster	4654	The TPS61023 is a thermally efficient chip that integrates dual 3A MOSFET switches. This mini-booster operates at $\pm 2.5\%$ reference voltage accuracy over -40°C to $+125^\circ\text{C}$ temperature range.	R 69.34	4	5V system supply.	J8, 1x4pin
3	16-bit ADC	ADS1110 Module	ADS1110 High Precision A/D Converter, 16-Bit, I2C, Low Power	R 88.00	4	High resolution cell voltage measurement.	J27, 1x6pin
4	External Temp sensor	18B20 Temperature Module	Electronic thermometer which has high accuracy over a wide range (accurate to $\pm 0.5^\circ\text{C}$) Cover the range of -10°C to $+85^\circ\text{C}$.	R22.00	4	Cell temperature measurement	J16, 1x3pin
PCB components	Tag	Product Name or Code	Detailed Description	Unit Cost	Qty	Function	KiCad
							Ref Qnty Val Dscrpt
1	0.1µF Capacitor	C1608X7R1E104K080A	0.1 µF $\pm 10\%$ 25V Ceramic Capacitor X7R 0603 (1608 Metric)	R0,51	8	Filter comms isolated supplies.	C1, C2 2 0.1µF Unpolarized capacitor
2	Red LED	LTST-C150KRKT	Red 631nm LED Indication - Discrete 2V 1206 (3216 Metric)	R3,45	5	System debug indicator.	D1 1 20mA 2V LED Light emitting diode
3	Green LED	LTST-C150KGKT	Green 470nm LED Indication - Discrete 3.3V 1206 (3216 Metric)	R3,45	4	Indicate module power on.	D2 1 20mA 2V LED Light emitting diode
4	Blue LED	LTST-C150TBKT	Blue 470nm LED Indication - Discrete 3.3V 1206 (3216 Metric)	R3,45	4	Indicate when dumpload is active.	D3 1 20mA 2.8V LED Light emitting diode
5	Fuse	021701.6TXP	FUSE GLASS 1.6A 250VAC 5X20MM	R6,49	4	Overcurrent protection.	F1 1 Fuse 1.6A. Glass fuse
6	NMOS	IRF540NLPBF	N-Channel 100 V 33A (Tc) 130W (Tc) Through Hole TO-262	R20,35	8	High-side switch.	Q1, Q2 2 IRF540 N 33A Id, 100V Vds, HEXFET N-Channel MOSFET
7	Comms isoChip	ISO7421D	General Purpose Digital Isolator 2500Vrms 2 Channel 1Mbps 25kV/us CMTI 8-SOIC (0.154", 3.90mm Width)	R54,34	4	Isolates module different voltage levels on comms line.	U1 1 ISO742 1 25kV isolating voltage coupler
8	2channel ANDgate	SN74LVC2G08DCTR	Texas Instruments SN74LVC2G08DCTR, Dual 2-Input AND Logic Gate, 8-Pin SSOP	R13,94	4	Communication logic hardware.	U2 1 SN74LV C2G08D CTR Dual channel and gate
9	LM4040AI M2 Vref IC	Texas Instruments Fixed Shunt Voltage Reference 2V $\pm 0.1\%$ 3-Pin SOT-23, LM4040AIM3-2.0/NOPB	Precision Fixed and Adjustable Voltage Reference ICs utilising series, shunt or series/shunt topologies and available in both through-hole and surface mount packages. Voltage References are available with initial accuracies of ± 0.02 to $\pm 2\%$. NTC chip thermistors offering a high thermal sensitivity. Suitable for temperature compensating circuits and other applications requiring a resistance that varies according to the ambient temperature	R58,64	4	Provide high precision reference voltage for ADC module.	U3 1 LM4040 DBZ 2.000V Precision Micropower Shunt Voltage Reference
10	Thermistor	TE Connectivity Thermistor, 10kΩ Resistance, NTC Type, 0805 (2012M), 2 x 1.25 x 0.5mm	10kOhm $\pm 1\%$ 0.5W, 1/2W Chip Resistor 1206 (3216 Metric) Pulse Withstanding Thick Film	R23,79	4	Used to measure the module's internal temperature.	TH1 1 Thermis tor_NT C Temperature dependent resistor, negative temperature coefficient
11	150Ω Resistor	CRGP1206F150R	150 Ohm $\pm 1\%$ 0.5W, 1/2W Chip Resistor 1206 (3216 Metric) Pulse Withstanding Thick Film	R4,99	8	Limit current to LED.	R1, R5 2 150Ω Chip resistor
12	10kΩ Resistor	RNCP1206FTD10KO	10 kOhm $\pm 1\%$ 0.5W, 1/2W Chip Resistor 1206 (3216 Metric) Anti-Sulfur Thin Film	R1,56	16	Pull up, pull down resistors.	R2, R4, R7, R13 4 10kΩ Chip resistor
13	499Ω Resistor	ERABAEB4990V	Panasonic 499Ω, 1206 (3216M) Thin Film SMD Resistor $\pm 0.1\%$ 0.25W	R9,18	8	Limit mosfet's gate current.	R3, R6 2 499Ω Chip resistor
14	20Ω Resistor	CRCW120620R0FKEAH P	Vishay 20Ω, 1206 (3216M) Thick Film SMD Resistor $\pm 1\%$ 0.5W	R5,12	4	Limit current to LED.	R8 1 20Ω Chip resistor
15	13Ω Resistor	HRG3216Q-13R0-D-T1	13 Ohms $\pm 0.5\%$ 1W Chip Resistor 1206 (3216 Metric) Anti-Sulfur, Automotive AEC-Q200, Moisture Resistant Thin Film	R9,74	16	Dumpload resistors.	R9, R10, R11, R12 4 13Ω Chip resistor
16	1kΩ Resistor	CRCW12061K00FKEA	Vishay 1kΩ, 1206 (3216M) Thick Film SMD Resistor $\pm 1\%$ 0.25W	R1,52	4	Pull-down	R14 1 1kΩ Chip resistor
17	2.2kΩ Resistor	ERABAEB222V	Panasonic 2.2kΩ, 1206 (3216M) Metal Film SMD Resistor $\pm 0.1\%$ 0.25W	R8,36	8	ADC pull-up resistors.	R15, R16 2 2.2kΩ Chip resistor
18	1µF Capacitor	C1608X7R1E105K080A B	1 μF $\pm 10\%$ 25V Ceramic Capacitor X7R 0603 (1608 Metric)	R1,41	4	ADC supply filter.	C3 1 1µF Filter capacitor
19	Terminal connector s	360272	Terminal Block MetzConnect 360272 1x1 Screw M2.6	R8,88	8	Connects module to cell terminals.	J5, J6 2 Screw Terminal 1x1 Generic screw terminal, single row
20	Current sensor.	Allegro Microsystems ACS770LCB-100U-PFF-T, Current Sensor IC 5-Pin, PFF	Allegro Current sensor IC, conductor resistance of 100 $\mu\Omega$ typical for ultra-low power loss, Hall Effect Current Sensor.	R157.61	1	Measures the battery current at master controller.	- - - -
21	1 Channel AND gate	SN74LVC1G08DCKR	Texas Instruments 2-Input AND Logic Gate, 5-Pin SC-70	R16.15	4	Communication logic hardware.	U4 1 74LVC1 G00 Single channel and gate

Special thanks:

I would like to take this opportunity to express my deepest gratitude to my Lord and my family for their unwavering support throughout my undergraduate studies. All my success and all my failures belongs to the Lord who gives me strength, thank You for Your grace upon my life. I am particularly grateful to my father for believing in me and funding my undergrad studies, which gave me the opportunity to pursue my dreams. My mother's constant encouragement and support have been invaluable. I would also like to thank my partner for helping me overcome the challenges that I faced during my studies and for having faith in me every step of the way. To everyone who was apart of this 5 year journey of mine, your support has been instrumental in helping me achieve my goals and for that I am grateful.