AN5967

Application note

Getting started with hardware development for STM32N6 MCUs

Introduction

This document demonstrates how to use the STM32N6 MCUs and details the minimum hardware resources required to develop an application. It provides an overview of the development board hardware implementation, focusing on features such as power supply, package selection, clock management, reset control, boot mode settings, and debug management.

This document also includes reference design schematics, describing the main peripherals, interfaces, and power modes. It may refer to STM32N6 microcontrollers as STM32N6x5 and STM32N6x7 product lines.

1 General information

This document applies to the STM32N6 Arm®Cortex®-M55-based microcontrollers.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Reference documents

The table below contains the main reference documents.

Table 1. Reference documents

Document type	Document reference	Document title
Datasheet	DS14791	Arm® Cortex®-M55, ST Neural-ART Accelerator, H264 encoder, Neo-Chrom 2.5D GPU, 4.2 Mbyte-contiguous SRAM (STM32N6 datasheet)
Errata sheet	ES0620	STM32N6 errata sheet
Reference manual	RM0486	STM32N6 advanced Arm®-based 32-bit MCUs
Programming manual	PM0273	STM32 Cortex®-M55 MCUs programming manual
User manual	UM3234	How to proceed with boot ROM on STM32N6 MCUs
Application note	AN5946	How to optimize low-power modes on STM32N6 MCUs
Application note	AN2867	Guidelines for oscillator design on STM8AF/AL/S and STM32 MCUs/MPUs
Application note	AN1709	EMC design guide for STM8, STM32, and legacy MCUs
Application note	AN6000	How to build the discrete power supply for STM32N6 MCUs

2 Terminology

The table below defines the acronyms and other terms mentioned in this application note.

Table 2. Acronyms

Acronym	Definition
ADC	Analog-to-digital converter
AHB	Advanced high-performance bus
AXI	Advanced extensible interface bus; by extension, the interconnect matrix based on AXI
BKPSRAM	Backup SRAM
BSEC	Boot and security controller (OTP interface)
CM55	Cortex®-M55 processor
CSI	Camera serial interface
CSS	Clock security system
DCMI	Digital camera interface (parallel interface)
DLYBSD	Delay block for SDMMC; compensates external signal timings to reach the highest data rates
DMA	Direct memory access; bus master that autonomously transfers data between peripheral and memory or between memories
EMC	Electromagnetic compatibility
ETH	Ethernet controller
ESD	Electrostatic discharge
EMI	Electromagnetic interference
EXTI	Extended interrupt and event controller
FDCAN	Controller area network with flexible data-rate; can also support time-triggered CAN
FMC	Flexible memory controller
GPIO	General-purpose input/output
GPU	Graphic processing unit
HDMI	High-definition multimedia interface
HDP	Hardware debug port
HSE	High-speed external crystal oscillator
HSI	High-speed internal oscillator
I2C	Inter-IC bus
I3C	Improved I2C
I2S	Inter-IC sound
IWDG	Independent watchdog
JTAG	Joint test action group (debug interface)
LCD	Liquid crystal display
LPTIM	Low-power timer
LSE	Low-speed external crystal oscillator
LSI	Low-speed internal oscillator
MLCC	Multi-layer ceramic capacitor
MSI	Multispeed internal oscillator
XSPI	Hexadata serial peripheral interface

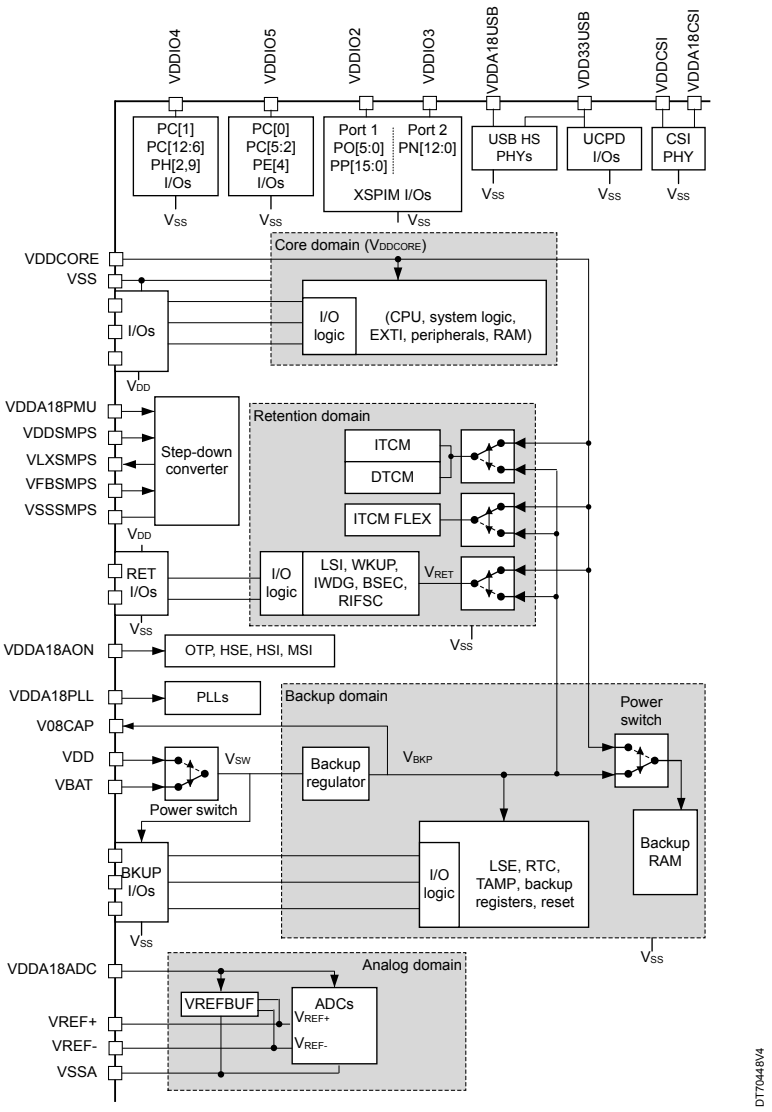
Acronym	Definition
XSPIM	XSPI IO manager
LTDC	LDC TFT display controller
NVIC	Nested vector interrupt controller
OTP	One-time programmable memory
PCB	Printed circuit board
PCI	PCI interface
PHY	Mixed-signal physical interface; adapts the internal logical level to a specific interface standard
PWR	Power control
RCC	Reset and clock control
RETRAM	Retention SRAM
RNG	Random number generator
ROM	Read-only memory
RTC	Real-time clock
SAI	Serial audio interface
SDMMC	Secure digital and multimedia card interface; supports SD, MMC, eMMC, and SDIO protocols
SMPS	Switched-mode power supply
SPDIF	Sony/Philips digital interface format
SPI	Serial peripheral interface
SRAM	Static random access memory
SW	Software
SWD	Serial wire debug
SWO	Single wire output; trace port
SYSCFG	System configuration
TAMP	Tamper detection IP
TIM	Timer
UART	Universal asynchronous receiver transmitter
UCPD	USB Type-C® power delivery controller
USART	Universal synchronous/asynchronous receiver/transmitter
USB	Universal serial bus
USB HS USB Hi-Speed	USB 2.0 at 480 Mbit/s half-duplex
USBPHYC	USB physical interface control
VREFBUF	ADC voltage reference buffer
WWDG	Window watchdog

3 Power supplies

The device is powered by multiple power supplies that must be connected to external decoupling capacitors. The system always requires a power supply on V_{DD} and $V_{DDA18AON}$.

Depending on the SMPS configuration mode, $V_{DDA18PMU}$ and V_{DDSMPS} must be provided to start V_{DDCORE} and to allow all other independent supplies to power up ($V_{DDA18ADC}$, $V_{DDA18CSI}$, $V_{DDA18PLL}$, $V_{DDA18USB}$, V_{BAT}, $V_{DD33USB}$, V_{DDIO2}, V_{DDIO3}, V_{DDIO4}, and V_{DDIO5}).

Figure 1. Power supply overview



3.1 Main power supplies

The main power supplies are the following:

- **V_{DD}**: external power supply for I/Os (can be 1.8 V or 3.3 V typical)
- **$V_{DDA18AON}$**: external power supply for analog blocks, such as reset, power management, and oscillators, and OTP memory (always needed ON) – 1.8 V typical

Table 3. Main power supplies

Symbol	Parameter	Operating conditions	Min.	Typ.	Max.	Unit
$V_{DDA18AON}$	Internal analog supply voltage		1.71	1.8	1.935	V
V_{DD}	I/Os supply voltage	1.8 V range	1.62	1.8	1.98	V
		3.3 V range	3	3.3	3.6	V

The V_{DDCORE} is the third power supply to run functional hardware on STM32N6 devices.

V_{DDCORE} is generated by SMPS, internally or externally. The power supplies are:

- **V_{DDSMPS}**: external power supply for the SMPS step-down converter.

Note: This power supply must be tied to VSS when the SMPS is not used.

- **$V_{DDA18PMU}$**: external analog power supply for the SMPS step-down converter - 1.8 V typical. This power supply can be connected to V_{DDSMPS} through an inductor-based filter.

Note: This power supply must be tied to VSS when the SMPS is not used.

- **V_{LXSMPS}**: step-down converter supply output
- **V_{FBSMPS}**: step-down converter sense feedback
- **V_{SSSMPS}**: separate step-down converter ground
- **V_{DDCORE}**: digital core domain supply - 0.8 V typical; dependent on V_{DD} supply. V_{DD} must be present before V_{DDCORE}.

Note: V_{DDCSI} must be connected to V_{DDCORE} as 0.8 V typical power.

3.2 Secondary power supplies

STM32N6 devices have the following secondary power supplies:

- **V_{BAT}**: optional external power supply for backup domain when V_{DD} is not present (V_{BAT} mode). When no battery is used, this power supply must be connected to V_{DD}.
- **V_{DDIO2}**: external power supply for 22 I/Os (PO[5:0] and PP[15:0]); independent from any other power supply; dedicated to powering the XSPIM1 16-bit interface(1).
- **V_{DDIO3}**: external power supply for 13 I/Os (PN[12:0]); independent from any other supply; dedicated to the XSPIM2 8-bit interface(1).
- **V_{DDIO4}**: external power supply for 10 I/Os (PC[1], PC[12:6], and PH[9,2]); independent from any other supply; dedicated to the SDMMC1(eMMC) interface(1).
- **V_{DDIO5}**: external power supply for six I/Os (PC[0], PC[5:2], and PE[4]); independent from any other supply; dedicated to the SDMMC2 *(SD-Card)* interface(1).
- **USB** power supply:
  - **$V_{DD33USB}$**: external power supply for USB2 HS PHYs and USB Type-C® (CC1 and CC2 pins); independent from any other supply - 3.3 V typical.
  - **$V_{DDA18USB}$**: external analog power supply for USB HS PHYs - 1.8 V typical.
- **$V_{DDA18CSI}$:** external analog power supply for CSI D-PHY - 1.8 V typical.
- **V_{DDCSI}:** CSI PHY digital supply input - 0.8 V typical.
- **$V_{DDA18PLL}$:** external analog power supplies for PLLs - 1.8 V typical.
- **$V_{DDA18ADC}$:** external analog power supply for ADCs and voltage reference buffers; independent from any other supplies (1.8 V only).

Note: The ADC interface is 1.8 V only.

- **V_{REF+}:** external reference voltage for ADCs, independent from any other supplies.
  - When the voltage reference buffer is enabled, the internal voltage reference buffer delivers VREF+ and VREF-.
  - When the voltage reference buffer is disabled, V_{REF+} is delivered by an independent external reference supply.

- **V_{SS}:** common ground for all supplies except the step-down converter and analog peripherals.
- **V_{SSA}:** separate analog and reference voltage ground; must be connected externally to the same supply ground as V_{SS} (1.8 V only).

1. *V_{DDIO2}, V_{DDIO3}, V_{DDIO4}, and V_{DDIO5} are independent. This means that each supply voltage can take any of the following voltage values at any time : 0 V (off), 1.8 V, or 3.3 V.*

Note: All ground pins (VSS, VSSA) must be connected to power planes. The following table must be used as a guideline only. Real count and values of capacitors can be adapted. This is dependent on various parameters, such as capacitor size and dielectric, PCB technology, and product power integrity simulations.

Decoupling power figures

The table below does not include capacitors on supply sources (such as LDO or SMPS) or external devices (such as SD-Card, eMMC, or flash memories).

Table 4. Power supply pins

Supply pin	Ground reference pin	Decoupling and filtering	Comments
VDD	VSS	n x 100 nF (MLCC, 10V, X5R, ±10%)	-
VBAT	VSS	100 nF (MLCC, 10V, X5R, ±10%)	No decoupling cap if VBAT connected to VDD
VDD33USB	VSS	1 µF (MLCC, 6.3 V, X5R, ±20%)	-
VDDA18PMU	VSSAPMU	100 nF (MLCC, 10V, X5R, ±10%)	VSSAPMU must be connected to VSS plane
VDDSMPS	VSSSMPS	2 x 10 µF (MLCC, 4V, X5R, ±20%) + 2 x 1 µF (MLCC, 6.3V, X5R, ±20%) + 2 x 100 nF (MLCC, 10V, X5R, ±10%)	VSSSMPS must be connected to VSS plane
VLXSMPS	VSSSMPS	1 µH ±20%, 1 MHz, I_{Sat} > 3000 mA DC, resistance < 0.06 Ω (DFE201612P-1R0M or TFM322512ALVA1R0MTAA) + 2.2 nF (MLCC, 50V, X7R, ±10%) + 4 x 15 µF (MLCC, 6V3, X5R, ±20%)	VSSSMPS must be connected to VSS plane
V08CAP	VSS	4.7 µF (MLCC, 6V3, X5R, ±20%)	Internal backup regulator output pin
VDDIO2	VSS	n x 100 nF (MLCC, 10V, X5R, ±10%)(1)	-
VDDIO3	VSS	n x 100 nF (MLCC, 10V, X5R, ±10%)(1)	-
VDDIO4	VSS	n x 100 nF (MLCC, 10V, X5R, ±10%)(1)	-
VDDIO5	VSS	n x 100 nF (MLCC, 10V, X5R, ±10%)(1)	-
VDDA18CSI	VSS	100 nF (MLCC, 10V, X5R, +/-10%)	-
VDDA18USB	VSS	100 nF (MLCC, 10V, X5R, ±10%)	-
VDDA18ADC	VSSA	100 nF (MLCC, 10V, X5R, ±10%)	VSSA must be connected to VSS plane
VDDA18AON	VSSAON	100 nF (MLCC, 10V, X5R, ±10%)	VSSAON must be connected to VSS plane
VDDA18PLL	VSS	100 nF (MLCC, 10V, X5R, ±10%)	-
VREFP	VSSA	1 µF (MLCC, 6.3V, X5R, ±20%) + 100 nF (MLCC, 10V, X5R, ±10%)	VSSA must be connected to VSS plane
VDDCORE	VSS	n x 1 µF (MLCC, 6.3 V, X5R, ±20%)(2)	-
VDDCSI	VSS	1 µF (MLCC, 6.3V, X5R, ±20%)	Usually connected to VDDCORE

1. *n is the number of VDDIOx pins.*
2. *n is the number of V DDCORE pins.*

For further details on package features, select Section 4: Package selection.

3.3 Independent ADC supply and reference voltage

To improve the conversion accuracy and dynamic range, the ADC and reference have an independent power supply that can be filtered separately, and shielded from noise on the PCB.

The analog operating voltage supply ($V_{DDA18ADC}$) is 1.8 V typical.

- The **ADC/VREFBUF voltage supply** input is available on a separate VDDA18ADC pin.
- **External VREF**: the user can connect a separate external reference voltage ADC input on VREF+. The voltage on VREF+ may range from 1.10 V to $V_{DDA18ADC}$.
- **Internal VREF**: the user can enable an internal reference voltage on VREF+ in the VREFBUF block. The voltage on VREF+ can be selected from either 1.21 V or 1.5 V. With internal VREF available on the VREF+ pin, it can be used externally (for example, for analog comparator references), if loading is kept within datasheet values.

3.4 System pins

The table below describes all the system pins.

Table 5. System pins

System pin	Description	Comments
PA13	JTMS/SWDIO	JTAG/SWD SIGNALS
PA14	JTCK/SWCLK	
PA15	JTDI	
PB4	NJTRST	
PB5	JTDO/TRACESWO	
PWR_ON	Output	This is the core supply enable output. This pin can be used to enable some secondary supplies.
PDR_ON	Input	This pin is used during ST production tests. It must always be connected to VDDA18AON in the final application.
PA5	PWR_CSTOP	This pin can be used to monitor the entry/exit to/from Stop mode.
PA10	PWR_CSLEEP	This pin can be used to monitor the entry/exit to/from Sleep mode.
BOOT0	BOOT0	This pin can be used to choose the boot scheme.
PA6	BOOT1	
PG10	BOOTFAIL	This pin is switched on or toggled by the boot ROM during a serial boot, dev boot, or blocking failure. It is used by the boot ROM to send a minimal UART text trace in case of blocking failure (multiplexed with UART5_TX).
PC13	TamperIN1/TamperOUT2	This is the only active tamper in VBAT mode. This pin is supplied by V_{SW}.
NRST	Input/Output	This is the application pad reset input/output.

3.5 USB supplies

The USB supplies must be connected to the same source with independent decoupling whenever possible.

- $V_{DD33USB}$: USB Hi-Speed PHY supply (3.3 V typical)
- $V_{DDA18USB}$: external analog power supply for USB HS PHYs (1.8 V typical)

3.6 Specific IO constraints related to voltage settings

V_{DD}, V_{DDIO2}, V_{DDIO3}, V_{DDIO4}, and V_{DDIO5} must respect specific register settings and control sequences when used at 3/3.3 V or 1.8 V typical.

For further information, refer to the PWR section in the reference manual RM0486.

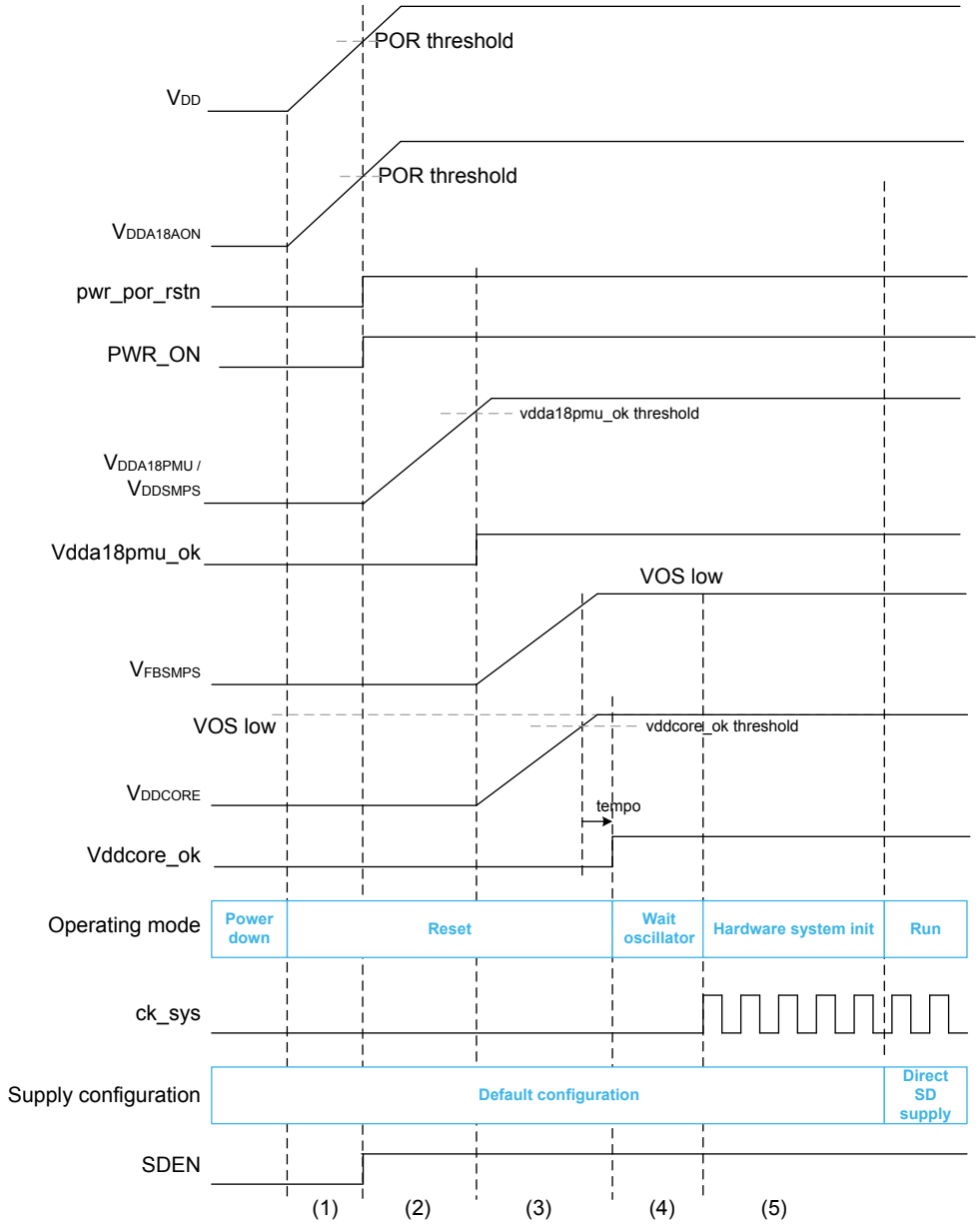
3.7 System startup

The startup system is different from other STM32 MCU architectures that need only V_{DD}/$V_{DDA18AON}$ to start up. Multiple voltage supplies must be applied with a specific sequence to start the device.

Figure 2 and Figure 3 demonstrate the system startup sequence from power-on in different supply and SMPS configurations.

V_{DDCORE} supply from SMPS step-down converter (internal SMPS configuration)

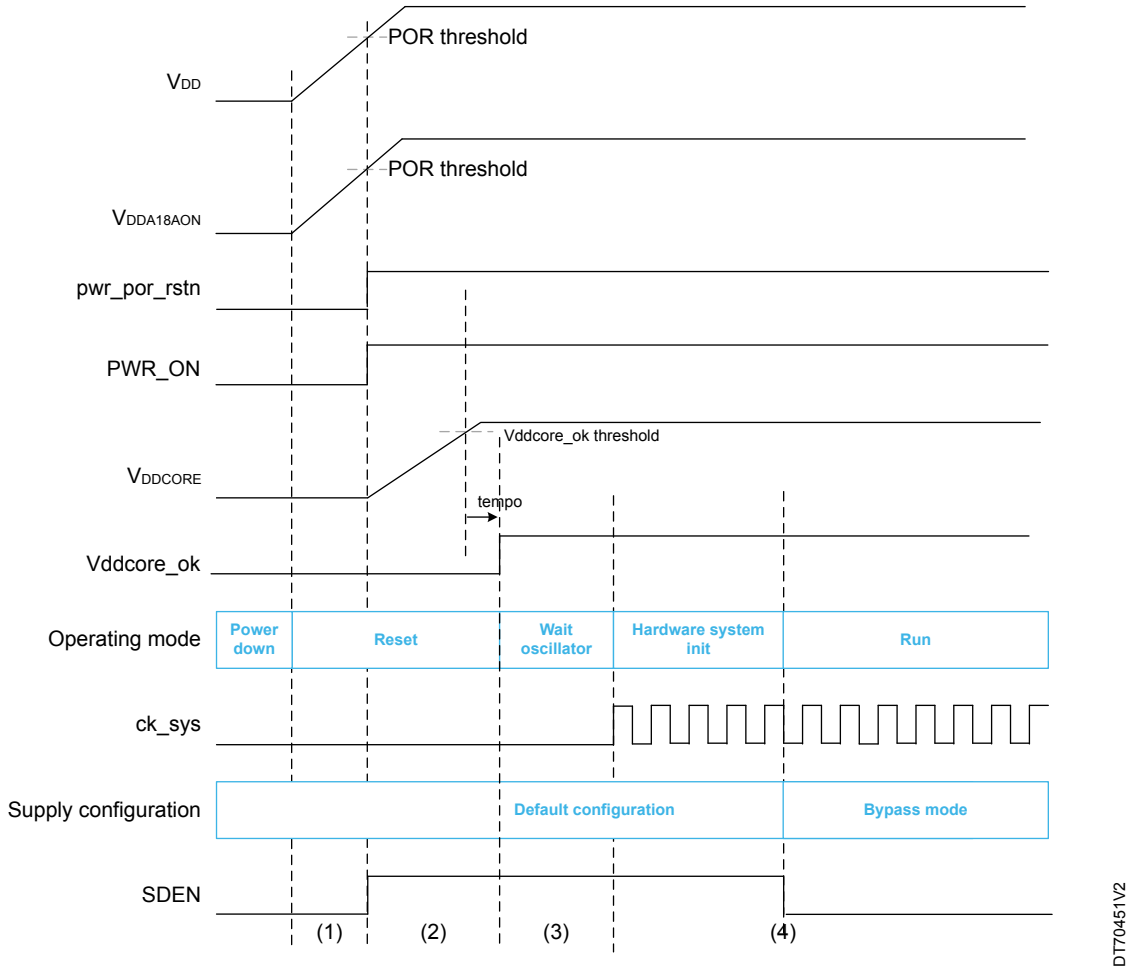
Figure 2. Device startup with V_{DDCORE} supplied directly from SMPS step-down converter



1. When the system is powered on, the POR monitors V_{DD} and $V_{DDA18AON}$ supplies. Once the supplies are above the POR threshold level, the external voltage regulator providing $V_{DDA18PMU}$ and V_{DDSMPS} supplies is enabled via the PWR_ON signal.
2. The SMPS step-down converter is kept in reset as long as $V_{DDA18PMU}$ and V_{DDSMPS} are not stable.
3. Once $V_{DDA18PMU}$ and V_{DDSMPS} supplies are above the vdda18pmu_ok threshold level, the SMPS step-down converter is taken out of reset, and the output level is set by default at 0.8 V (VOS low). The system is kept in reset mode as long as V_{DDCORE} is stable.
4. Once V_{DDCORE} supply surpasses the vddcore_ok threshold level, the system is taken out of reset, and the HSI oscillator is enabled.
5. Once the oscillator is stable, the system is initialized: option bytes are loaded, and the CPU starts in Run mode.

V_{DDCORE} supply in bypass mode (external SMPS configuration - SMPS off)

Figure 3. Device startup with V_{DDCORE} supplied from an external regulator



The devices featuring the SMPS can also be used in bypass mode.

1. When the system is powered on, the POR monitors V_{DD} and $V_{DDA18AON}$ supplies. Once the supplies are above the POR threshold level, the external voltage regulator providing the V_{DDCORE} supply is enabled via the PWR_ON signal.
2. The system is kept in reset mode as long as V_{DDCORE} is not stable.

3. Once V_{DDCORE} supply surpasses the vddcore_ok threshold level, the system is taken out of reset, and the HSI oscillator is enabled.
4. Once the oscillator is stable, the system is initialized: option bytes are loaded and the CPU starts in run mode. The software must disable SMPS bit clearing SDEN in PWR_CR1 as soon as possible.

STM32N6 power-up sequence

Follow the steps below:

1. Apply V_{DD}, V_{BAT}, and $V_{DD18AON}$.
2. If V_{DDCORE} is supplied from an external SMPS step-down converter, apply V_{DDCORE} when the PWR_ON signal is high. Otherwise, V_{DDCORE} is internally generated (refer to the section *System supply startup and core domain* of the PWR section in the reference manual RM0486).
3. Then, apply the remaining power supplies in whatever order: $V_{DDA18USB}$, $V_{DD33USBCC}$, $V_{DDA18CSI}$, V_{DDCSI}, $V_{DDA18ADC}$, V_{REF+}, and V_{DDSMPS}.

Note: The domains can be grouped together as follows to simplify the power supply design:

- *V_{DDCSI} and V_{DDCORE}.*
- *$V_{DDA18PLL}$, V_{DDIO2}, V_{DDIO3}, V_{DDIO4}, V_{DDIO5}, and $V_{DDA18AON}$.*
- *$V_{DDA18USB}$, $V_{DDA18CSI}$, $V_{DDA18ADC}$, V_{REF+}.*
- *$V_{DD33USBCC}$ and $V_{DD33USB}$.*

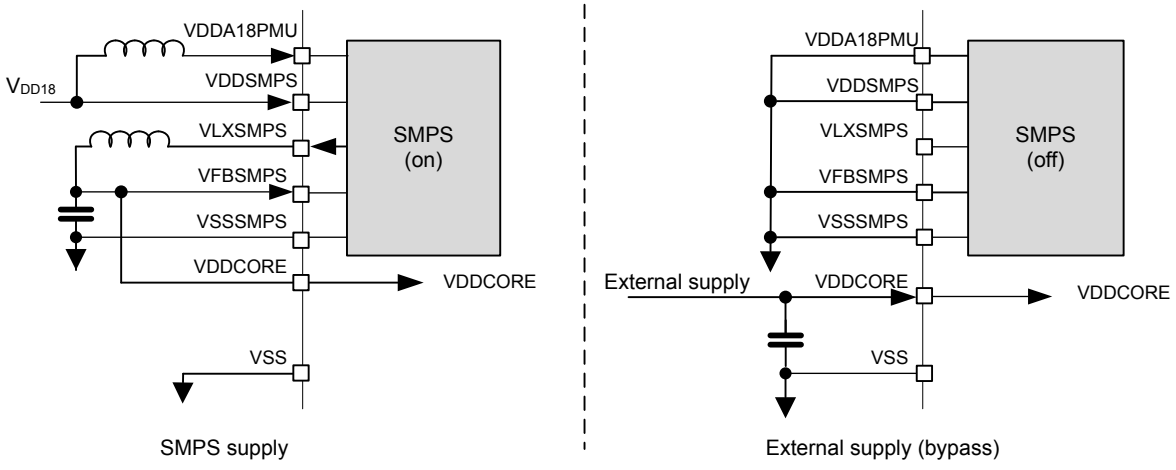
STM32N6 power-down sequence

Apply the steps described from the power-on sequence in reverse order.

3.8 SMPS configuration

The V_{DDCORE} domain is supported. The configuration is controlled through the SDEN bit in the PWR_CR1 register.

Figure 4. System supply configurations



4 Package selection

The package must be selected by considering the application requirements.

The list below summarizes the most frequent constraints:

- Number of interfaces required. Some interfaces are unavailable on some packages. Some interface combinations are unavailable on some packages. Refer to the product datasheet for details.
- PCB technology constraints: small pitch and high ball density may require more PCB layers and higher PCB classes, requiring stack-up with microvia (laser via) technology.
- Package height.
- PCB available area.
- Thermal constraints (larger packages have better thermal dissipation capabilities).

Table 6. Package summary

Characteristic	Size (mm)[1]					
	14x14	10x10	10x10	12x12	8x8	6x6
Pitch (mm)	0.8	0.5	0.65	0.8	0.5	0.4
Thickness	N/A	N/A	N/A	N/A	N/A	N/A
Number of IOs	165	144	126	106	90	75
Sales number	VFBGA264	VFBGA223	VFBGA198	VFBGA178	VFBGA142	VFBGA169
STM32N6x5	X0	L0	B0	I0	Z0	A0
STM32N6x7	X0	L0	B0	I0	Z0	A0

1. *Typical body size*

Table 7. Package thermal characteristics

Package	θ_{JA}	θ_{JB}	θ_{JC} (top)	Ψ_{JB}	Ψ_{JC} (top)
VFBGA264	30.4	20.4	9.8	20.2	0.2
VFBGA223	31.9	19.5	10.1	19.3	0.2
VFBGA198	32.0	19.7	10.2	19.5	0.2
VFBGA178	27.8	16.5	9.0	16.4	0.1
VFBGA169	40.3	24.5	12.9	24.0	0.2
VFBGA142	36.6	22.3	10.9	22.7	0.2

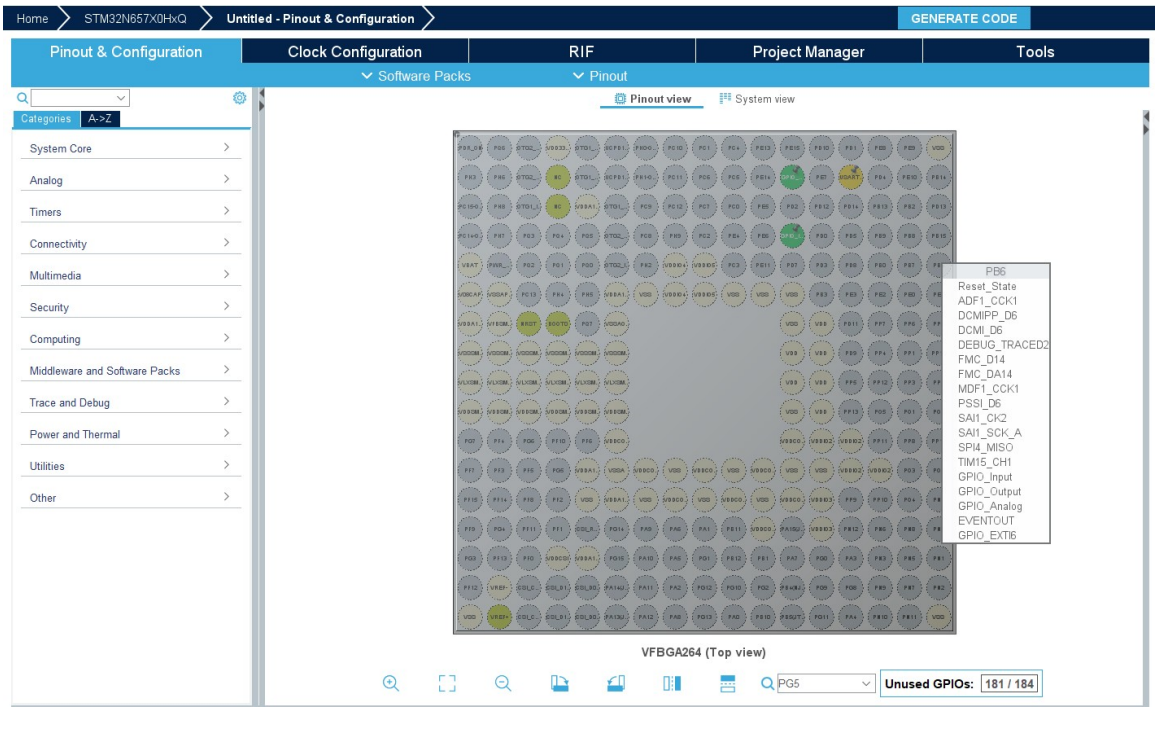
Note: To obtain up-to-date reference availability, refer to the product datasheet.

5 Alternate function mapping to pins

To explore peripheral alternate function mapping to pins easily when using the STM32N6 MCUs, use the STM32CubeN6 tool, available on www.st.com.

Note: The screenshot below is an example only, not specific to STM32N6 MCUs. The look and feel may differ from future CubeMX versions.

Figure 5. STM32CubeMX example screenshot



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6 Clocks

Different clock sources can be used to drive the subsystem clocks:

- Internal clock signal:
  - HSI oscillator clock (high-speed internal clock signal): 64 MHz typical
  - MSI oscillator clock (multispeed internal clock signal): 4 MHz typical
- External clock signal:
  - HSE oscillator clock (high-speed external clock signal): 48 MHz typical

The devices have two secondary clock sources:

- LSI: 32 kHz low-speed internal RC, driving the independent watchdog and, optionally, the RTC used for autowake-up from the Stop and Standby modes.
- LSE (LSE crystal): 32.768 kHz low-speed external crystal, optionally driving the real-time clock (RTCCLK).

The RCC authorizes the access of four PLL clocks with the same features. A typical allocation is:

- PLL1: clock to the CPU, buses, and AXI storage areas
- PLL2: clock to NPU and NPU storage areas
- PLL3: clock to CACHEAXI RAM and Ethernet
- PLL4: clock to display, camera module, FDCAN, and other peripherals

Each clock source can be switched on or off independently when it is not used, to optimize power consumption.

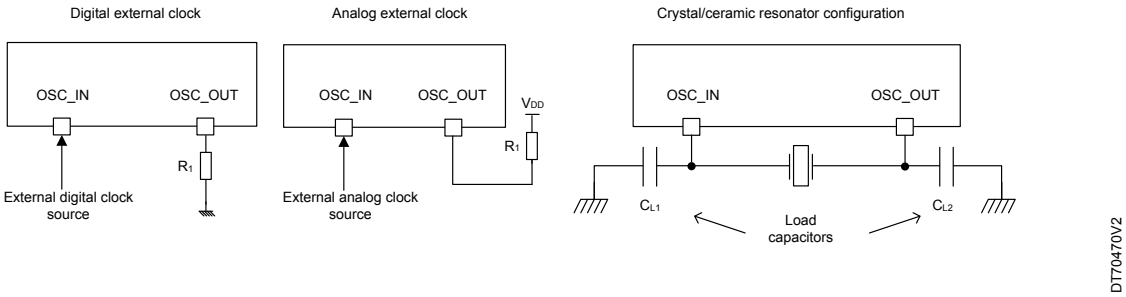
For the description of the clock tree and the details about the possible clock frequencies, refer to the product reference manual and datasheet.

7 HSE oscillator

The high-speed external clock signal (HSE) can be generated from two possible clock sources:

- HSE user external clock
- HSE external crystal

Figure 6. HSE source clock



The possible configurations are:

- OSC_OUT is tied to GND (max 1 kΩ): HSE digital bypass.
- OSC_OUT is tied to VDDA18AON (max 1 kΩ): HSE analog bypass.
- OSC_OUT high-Z or connected to a crystal: HSE crystal mode.

When the bypass is used, PWR_ON can enable the external clock generator to save power (that is, disabled in Standby). In that case, the OSC_IN clock input must be stable within 10 ms after the PWR_ON rising edge occurs.

7.1 External source - HSE bypass mode

In this mode, an external clock source must be provided. It can have a frequency ranging from 8 to 48 MHz. For the actual max value, refer to the product datasheet.

The external digital (VIL/VIH) or analog clock signal, with a duty cycle of about 50%, must drive the OSC_IN pin.

7.2 External crystal - HSE crystal mode

The external oscillator frequency ranges from 8 to 48 MHz. It has the advantage of producing a very accurate rate on the main clock.

Using a 40-MHz crystal frequency is a good choice to get accurate USB and PCIe® high-speed clocks. The oscillator mode is enabled by clearing the HSEBYP bit and setting the HSEON bit.

The crystal and the load capacitors must be connected as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected crystal.

For CL1 and CL2 it is recommended to use NP0/C0G capacitors, selected to meet the load requirements of the crystal. CL1 and CL2 usually have the same value. The crystal manufacturer typically specifies a load capacitance, which is the series combination of CL1 and CL2. The PCB and pin capacitances must be included when sizing CL1 and CL2.

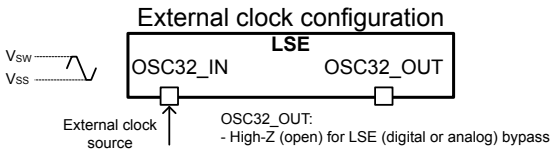
For further information, refer to the electrical characteristics and to the application note AN2867.

8 LSE oscillator

The low-speed external clock signal (LSE) can be generated from two possible clock sources:

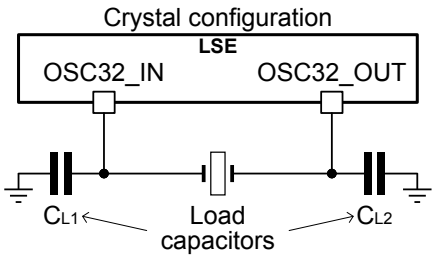
- The LSE user external clock:

Figure 7. LSE external clock



- The LSE external crystal/ceramic resonator:

Figure 8. LSE crystal resonators



8.1 External source - LSE bypass mode

In this mode, an external clock source must be provided. It can have a frequency of up to 40 kHz.

The external digital (VIL/VIH) or analog clock signal, with a duty cycle of approximately 50%, must drive the OSC32_IN pin, while the OSC32_OUT pin must be left high-Z.

The configuration of the bypass mode and the selection between digital and analog is done using the RCC registers (RCC_CR register).

For further details, refer to the reference manual RM0486.

8.2 External crystal - LSE crystal mode

The LSE crystal is a 32.768 kHz low-speed external crystal. It has the advantage of providing a low-power, but highly accurate, clock source to the real-time clock peripheral (RTC) for clock, calendar, or other timing functions.

The resonator and the load capacitors must be connected as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. The load capacitance values CL1 and CL2 must be adjusted according to the selected oscillator.

It is recommended to use a medium-high or high drive on the LSE oscillator.

For further details, refer to the electrical characteristics in the product datasheet and to the application note AN2867.

9 Clock security system

The clock security system (CSS) detects failures of the LSE and HSE oscillators.

For further details, refer to the reference manual RM0486.

9.1 CSS on HSE

The clock security system can be activated by software. In this case, the clock detector is enabled after the HSE oscillator startup delay, and disabled when this oscillator is stopped.

If the CSS detects a failure on the HSE oscillator clock, it can generate an application reset.

9.2 CSS on LSE

The clock security system can be activated by software. In this case, the clock detector is enabled after the LSE oscillator startup delay, and disabled when this oscillator is stopped.

If the CSS detects a failure on the LSE oscillator clock, it stops the RTC/TAMP clock source and signals the failure to the TAMP block for security protection and system wake-up.

10 Boot configuration

The BOOT0 and BOOT1 pins and one OTP word determine the boot mode on STM32N6 devices.

The BOOT1 is a nondedicated boot pin. If flash memory boot is selected, the flash memory device selection is done using OTP fuses. If serial boot is selected, interfaces can be disabled by fuse.

Note:
- *The BOOT1 pin check has priority on the BOOT0 pin check.*
- *If the BOOT1 pin is not set, BOOT0 is checked.*
- *If the BOOT1 pin is selected but not allowed in the current life cycle, the BOOT0 pin is checked.*

Table 8. Boot source description

BOOT0 pin	BOOT1 pin	Boot source	Interface	OTP11 word value
-	1	Development boot	-	-
0	0	Flash memory boot	XSPI serial NOR (in default, SPI, and single)	OTP11 [8:5] = 0x0011
			XSPI HyperFlash™ (8-bit)	OTP11 [8:5] = 0x0101
			eMMC SDMMC1	OTP11 [8:5] = 0x0010
			eMMC™ SDMMC2	OTP11 [8:5] = 0x1000
			SD-Card SDMMC1 (up to SD standard v6.0)	OTP11 [8:5] = 0x0001
			SD-Card SDMMC2 (up to SD standard v6.0)	OTP11 [8:5] = 0x0111
1	0	Serial boot	USB boot: USB 2.0 OTG_HS	OTP11 [16:9] = 0x1111111x x= 0 USB enable, x=1 USB disable
			UART boot (default mode)	OTP11 [16:9] = 0x111111x1 x= 0 UART enable, x=1 UART disable

Note: Default modes correspond to no fused configuration on the OTP11 word.

BOOT0 = 0: OTP11 [8:5] = 0x0000

BOOT0 = 1: OTP11 [16:9] = 0x0000

For further details, refer to the user manual UM3234.

11 Debug management

The host/target interface is the hardware equipment that connects the host to the application board. It consists of three components:

- A hardware debug tool
- A JTAG or SWD connector
- A cable connecting the host to the debug tool

11.1 SWJ debug port (serial wire and JTAG)

The core of the STM32N6 MCUs integrates the serial wire/JTAG debug port (SWJ-DP). It is an Arm® standard CoreSight™ debug port, combining a JTAG-DP (5-pin) interface and an SW-DP (2-pin) interface.

- The JTAG debug port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port.
- The serial wire debug port (SW-DP) provides a 2-pin (clock + data) interface to the AHB-AP port.

The two pins of the SW-DP are multiplexed with two of the five JTAG pins of the JTAG-DP.

11.2 Debug LED

The PG10 (AF11) pin has specific BOOTFAILED behavior:

- During the boot phase, in the case of boot failure, the BOOTFAILED (PG10) pin is set to low open-drain, meaning the debug LED lights up brightly. In most cases, if secure boot is disabled, this fail is invisible as it immediately falls back to a UART/USB boot.
- During the UART/USB boot, the PG10 pin toggles open-drain at a rate of a few hertz until a connection starts; the debug LED blinks fast.
- In development boot mode, the PG10 pin is set to low open-drain, meaning the debug LED lights up brightly.
- In all other cases, the PG10 pin is kept in its reset value (high-Z until further software configuration).

The recommendation is to use this debug pin. The LED connection quickly shows the system activity, making PG10 perfect for quick low-level boot error signaling. In most cases, the LED circuitry does not conflict with usage for other purposes.

For further details, refer to the user manual UM3234.

12 Recommendations

12.1 PCB

For technical reasons, it is mandatory to use a multilayer PCB:

- A separate layer is dedicated to the ground (V_{SS}).
- Another layer is dedicated to power supplies like V_{DD}, V_{DDCPU}, and V_{DDCORE}.

This provides good decoupling and a good shielding effect.

12.2 Component position

A preliminary layout of the PCB must separate the different circuits according to their EMI contribution. This reduces the cross-coupling on the PCB (noisy, high-current circuits, low-voltage circuits, and digital components).

12.3 Ground and power supplies (V_{SSx}, V_{DDx})

Due to the large power and high frequencies involved in STM32N6 devices, it is mandatory to use the PCB with at least four layers, and with dedicated power planes for V_{SSx} and V_{DDx}.

12.4 I/O speed settings

STM32N6 devices are made using a 16 nm technology, which requires MOSFETs transistor gate voltages lower than 1.0 V. As these products are primarily intended to use high frequency external memories (in HEXA/OCTOSPI or SDMMC) and therefore, to be compatible with a wide range of 1.8/3.3V memories, the GPIOs have been designed to tolerate voltages up to 3.3 V (TT structure). This means that each GPIO includes protections, allowing it to operate in TT mode by default after a reset, and with the default factory OTP124 HCONF bit configuration (refer to the Operating conditions section of DS14791) .

The role of bits in OTP124 is to bypass the TT protection (3.3 V tolerant) and to make the I/O levels compatible with voltages below 2.5 V (namely 1.8 V):

- Bit 13: HSLV_VDDIO5
- Bit 14: HSLV_VDDIO4
- Bit 15: HSLV_VDDIO3
- Bit 16: HSLV_VDDIO2
- Bit 17: HSLV_VDD

It is important that, in addition to OTP124, the corresponding VDDIOxVRSEL bits in the PWR_SVMCRx registers are set by firmware:

- PWR_SVMCR1 bit 24 VDDIO4VRSEL: controls PC[1], PC[12:6], and PH[9:2] I/Os in VDDIO4 domain
- PWR_SVMCR2 bit 24 VDDIO5VRSEL: controls PC[0], PC[5:2] and PE[4] I/Os in VDDIO5 domain
- PWR_SVMCR3 bit 26 VDDIO3VRSEL: controls PN[12:0] I/Os in VDDIO3 domain
- PWR_SVMCR3 bit 25 VDDIO2VRSEL: controls PO[5:0] and PP[15:0] I/Os in VDDIO2 domain
- PWR_SVMCR3 bit 24 VDDIOVRSEL: controls PA[15:0], PB[15:0], PC[15:14], PD[15:0], PE[3:0], PE[15:5], PF[15:0], PG[15:0], PH[1:0], and PH[8:3] in VDD I/Os domain

Thanks to these settings the I/Os of the XSPI and SDMMC/eMMC interfaces can reach the frequencies specified in the datasheet.

The GPIOs can be also configured according to the signal frequency and capacitive load. It is important to enable the right output drive on the I/O structure, to have sufficient rise and fall times, and noise effect immunity.

If the I/O is independent from the GPIO voltage domain, and when there are no specific requirements for its speed, the GPIO can be left configured in GPIOx_OSPEEDR Low speed.

Five I/O compensation cells (one for I/Os supplied by VDD, four for I/Os supplied by VDDIO2, VDDIO3, VDDIO4, and VDDIO5) are used to control the current slew-rate in the I/O buffer structure. Their behavior depends upon PVT conditions (such as process, voltage and temperature).

12.5 ESD/EMI protections

Electrostatic discharge (ESD) and electromagnetic interference (EMI) protections must be considered from the start of product development, as it can be very complex and expensive to add them later.

ESD and EMI are driven by global standards (such as IEC 61000 and JESD 22), which require certification in most countries, to allow mandatory marking to be applied on a product (such as CE and FCC). They are also driven by standardized interface certification or requirements (for example, USB).

Although the STM32N6 MCUs embed device-level ESD protection, external components must manage the final product protection, especially on interfaces with external user access in the final product (such as Ethernet, USB, and SD-Card). Some components provide ESD protection, as well as EMI common-mode filtering. For example, ECMF02-2AMX6 used on USB.

Section 13: Reference design examples provides examples of ESD/EMI protections. For further details, refer to the application note AN1709.

12.6 Sensitive signals

When designing an application, the EMC (electromagnetic compatibility) performance can be improved by closely observing the following:

- Signals for which a temporary disturbance affects the running process permanently (such as interrupts and handshaking strobe signals, not the case for LED commands). For these signals, a surrounding ground trace, shorter lengths, and the absence of noisy or sensitive traces nearby (the crosstalk effect) improve the EMC performance. For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (such as clocks).
- Sensitive signals (such as high-Z ones).

For more information, refer to the application note AN1709.

12.7 Unused I/Os and features

The STM32N6 MCUs are designed for a wide range of applications. Often a particular application does not use 100% of the resources.

To increase the EMC performance, unused clocks, counters, or I/Os must not be left free. For example, I/Os must be set to "0" or "1" (external or internal pull-up or pull-down to the unused I/O pins) and unused features must be "frozen" or disabled.

13 Reference design examples

This section provides examples to help the user connect major and critical interfaces to the STM32N6 MCUs.

13.1 Clock

STM32N6 MCUs use two clock sources:

- **LSE**: 32.768 kHz crystal for the embedded RTC
- **HSE**: 8 to 48 MHz (crystal or external oscillator) as the main clock

Refer to Section 6: Clocks for more details.

Table 9. HSE BOM for oscillator or crystal example for NX2016SA - 40 MHz

-	Oscillator (OSC_OUT = logic 0)	Crystal (OSC_OUT = crystal pin)
X1	NZ2016SH 40 MHz	NX2016SA 40 MHz
R1	10 Ω	- (open)
R2	10 kΩ/30 KΩ (1)	- (open)
R3	- (open)/33 kΩ(1)	0 Ω
R4	1 kΩ	- (open)
C1	- (open)	6.8 pF
C2	- (open)	6.8 pF
C3	10 nF	- (open)

1. *For respectively VDD = 3.3 V and VDD = 1.8 V. In case of VDD = 3.3 V, a resistor divider formed by R2/(R3+R4) is required as the oscillator pin 1 (Enable) must be limited to a $V_{DDA18AON}$ (1.8 V) voltage, which supplies the external oscillator.*

13.2 SD card

Note: As boot is always done in "Standard" mode (3-V IOs), if the card is used by the application in UHS-I, a power cycle on the card supply is required after a Reset or Standby mode. NRSTC1MS can be used for this.

Good signal integrity is dependent on the board, GPIO strength settings (GPIO_OSPEEDR registers), and V_{DD} voltage.

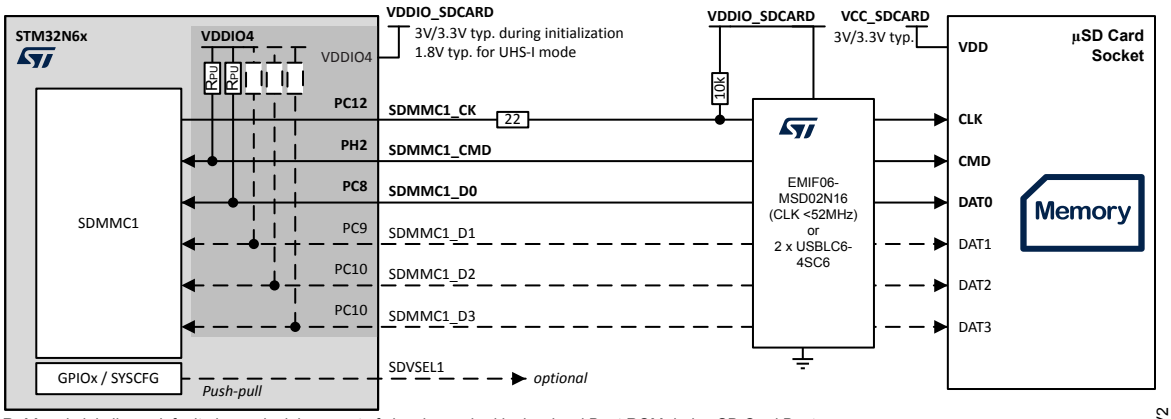
When using V_{DDIO4} = 1.8 V, a setting of VDDIOxVRSEL can be required to ensure the adequate speed on pins used on SDMMC1 outputs. If needed, the impedance matching resistor must be placed as close as possible to the output driver pin. Values in the example below work in most cases, but can be tailored to IO drive strengths and PCB impedance.

Before the V_{CC_SDCARD} shutdown (for example, before entering Standby mode), the SDMMC1 driver must set all signals going to the card to 0 or high-Z. The example is independent of MPU I/O voltage V_{DD} and relies on variable VDDIO4 that can be set either to 3.0/3.3 V, or 1.8 V typical using one of the following:

- SDVSEL1 (0 or high-Z = 3/3.3 V (default), 1 = 1.8 V) connected to an external regulator or other component managing the V_{DDIO4} voltage
- A regular GPIO output connected to an external regulator or other component managing the V_{DDIO4} voltage
- An I²C bus when used with PMIC

If no programmable V_{DDIO_SDCARD} is available on the platform, V_{DDIO4} can be connected to V_{CC_SDCARD}. In this case, UHS-I is not supported.

Figure 9. **SD-Card with embedded level shifter connection**



Bold and plain lines: default pins and minimum set of signals required by low level Boot ROM during SD Card Boot.

DT71888V2

Note: When switching to UHS-I mode (V_{DDIO4} = 1.8 V), VDDIOxVRSEL must be set only when V_{DDIO4} is within the 1.8 V allowed range. In case of a reset of the SD-Card to the legacy 3/3.3V range and to avoid damage to the I/Os, VDDIOxVRSEL must be cleared before the voltage is outside the 1.8 V allowed range.

13.3 USB

Multiple USB options are possible. Examples are listed below:

- 1 × Hi-Speed USB device
- 1 × Hi-Speed USB device + 1 × USB Hi-Speed host (Figure 10. USB hi-speed host example)

The case of multiple Hi-Speed USB hosts using an external USB hub component is not described here.

Note: In the case of on-board flash memory programming using the STM32CubeProgrammer, at least one USB with device capabilities is required.

Table 10. **USB high-speed PCB routing recommendations**

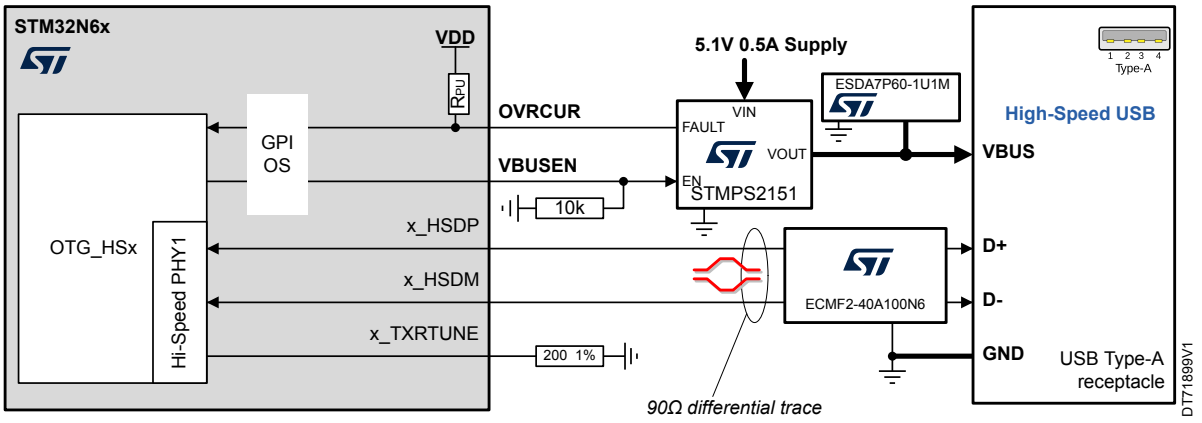
Recommendation	Min	Typ	Max	Unit
Differential impedance	76.5	90	103.5	Ω
Single-ended impedance	38.25	45	51.75	Ω
Length matching within a pair (including package)	-50	-	+50	mils
	-1.27	-	+1.27	mm
Max trace length (up to connector or first active component)	-	-	8	inches
	-	-	203	mm
Max number of vias (recommended value)	-	-	2	-
Distance between any differential trace and other signals	S-2S	S-3S or more		(1)
Do not route over a power plane split. No stubs (point to point only). No right angles				

1. *Definition can be found in the DDR memory routing guidelines.*

13.3.1 USB hi-speed host with Type-A connector (USBH)

A 200 Ω 1% resistor should be connected between USBH_HS_TXRTUNE and V_{SS}.

Figure 10. **USB hi-speed host example**



Note: VBUS 1A is also possible using STMPS2171 instead of STMPS2151.

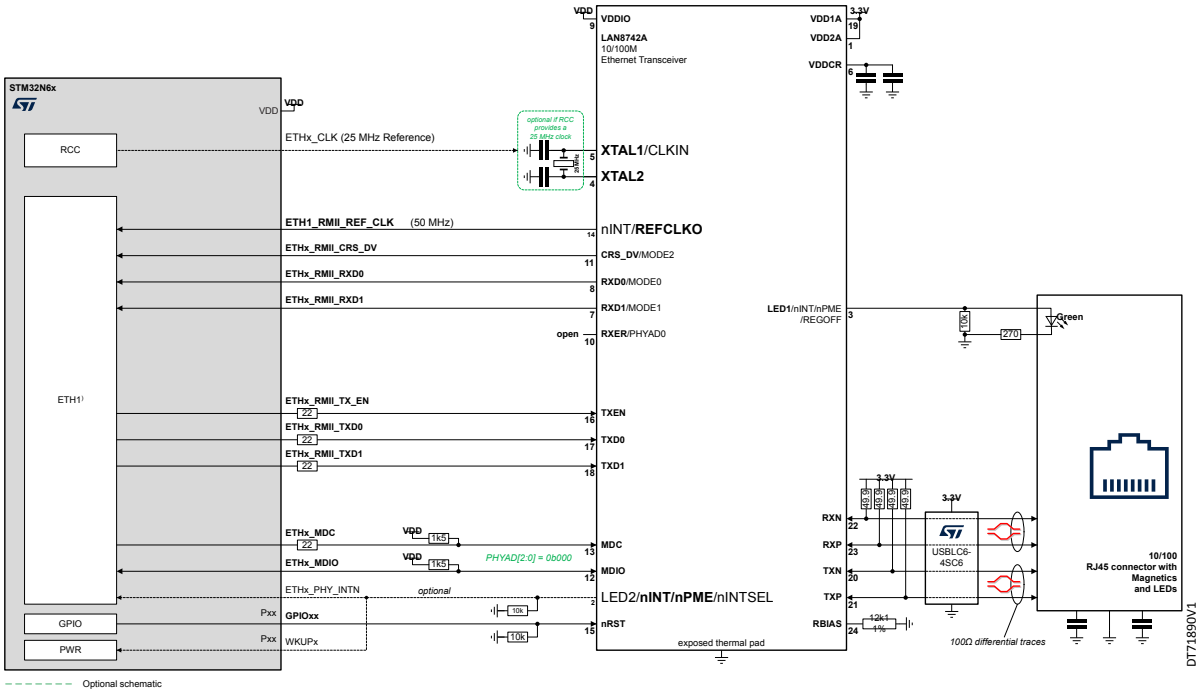
13.4 Ethernet

13.4.1 10/100M Ethernet

Note: Good signal integrity is dependent on the board, GPIO strength settings (GPIO_OSPEEDR registers), and V_{DD} voltage.

When using VDD = 1.8 V, setting VDDIOxVRSEL may be required to ensure the adequate speed on the pins used on the ETHx outputs. If needed, the impedance matching resistors must be placed as close as possible to the output driver pin. The values in the example below work in most cases, but can be tailored to the I/O drive strengths and PCB impedance of each side.

Figure 11. **10/100M Ethernet PHY connection example**



Note:

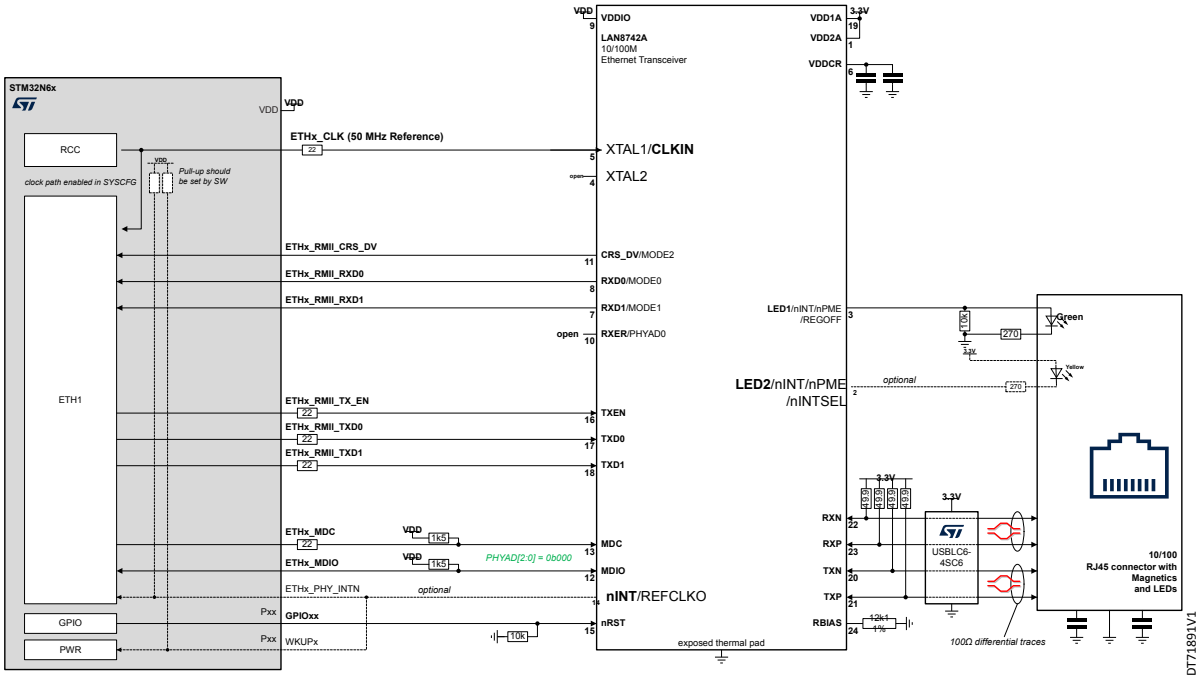
1. *ETH1 is either ETH1 direct or ETHSW port2 (ETHSW is not available on some part numbers).*
2. *ETH2 is not available on some part numbers.*
3. *ETH3 is ETHSW port1. ETHSW is not available on some part numbers.*
4. *Decoupling capacitors are not shown.*

As RCC cannot provide the 25 MHz reference clock to the PHY in low-power modes, the dedicated 25 MHz crystal is required on the PHY in case a "wake-up on LAN" (WOL) is needed for the platform.

Setting RCC PLLs to get 25 MHz output for PHY clocking can constrain other RCC frequencies. In this case, it is more flexible to put a dedicated 25 MHz crystal on the PHY.

Alternatively, if PHY allows it and if the RCC can provide a precise 50 MHz clock (to be checked with respect to HSE quartz frequency and RCC, other peripheral, or core clock frequency settings), the STM32N6 devices can provide a 50 MHz ETH_CLK to the PHY, and REF_CLK is left unconnected on both sides. This saves BOM and area, as well as power on some PHYs.

Figure 12. 10/100M Ethernet PHY connection (with REFCLK from RCC)



Note:

1. *ETH1 is either ETH1 direct or ETHSW port2 (ETHSW is not available on some part numbers).*
2. *ETH2 is not available on some part numbers.*
3. *ETH3 is ETHSW port1. ETHSW is not available on some part numbers.*
4. *Decoupling capacitors are not shown.*

As the RCC cannot provide the 50 MHz reference clock to the PHY in low-power modes, this option is not possible in case a a "wake-up on LAN" (WOL) is needed for the platform.

Setting RCC PLLs to get 50 MHz output for PHY clocking can constrain other RCC frequencies. In that case, this option is not possible.

Table 11. ETH RMII pins

Pin name	Signal direction(1)	ETH1(2)	ETH2(3)	ETH3(3)(4)	Comments
ETHx_CLK	→	PF3, PF5, PF8	PF4, PG3	-(5)	Optional 25 MHz or 50 MHz reference(6)
ETHx_RMII_REF_CLK	←	PA14	PC0, PF6	PA5	Optional if 50 MHz provided by ETHx_CLK
ETHx_RMII_CRS_DV	←	PA11	PC3, PF8	PA2	-
ETHx_RMII_RXD0	←	PF1	PG0	PA9	-
ETHx_RMII_RXD1	←	PC2	PC12	PA10	-
ETHx_RMII_TX_EN	→	PA13	PC4	PA3	-
ETHx_RMII_TXD0	→	PA15	PC7	PA6	-
ETHx_RMII_TXD1	→	PC1	PC8	PA7	-
ETHx_MDC	→	PA9, PF0, PF4	PC6, PG4, PH10	-(7)	-
ETHx_MDIO	→ ←	PA10, PF2, PF5	PC5, PF9, PH11	-	-
ETHx_PHY_INTN	←	PA12, PC6, PF5	PF5, PG3	PA1	Optional

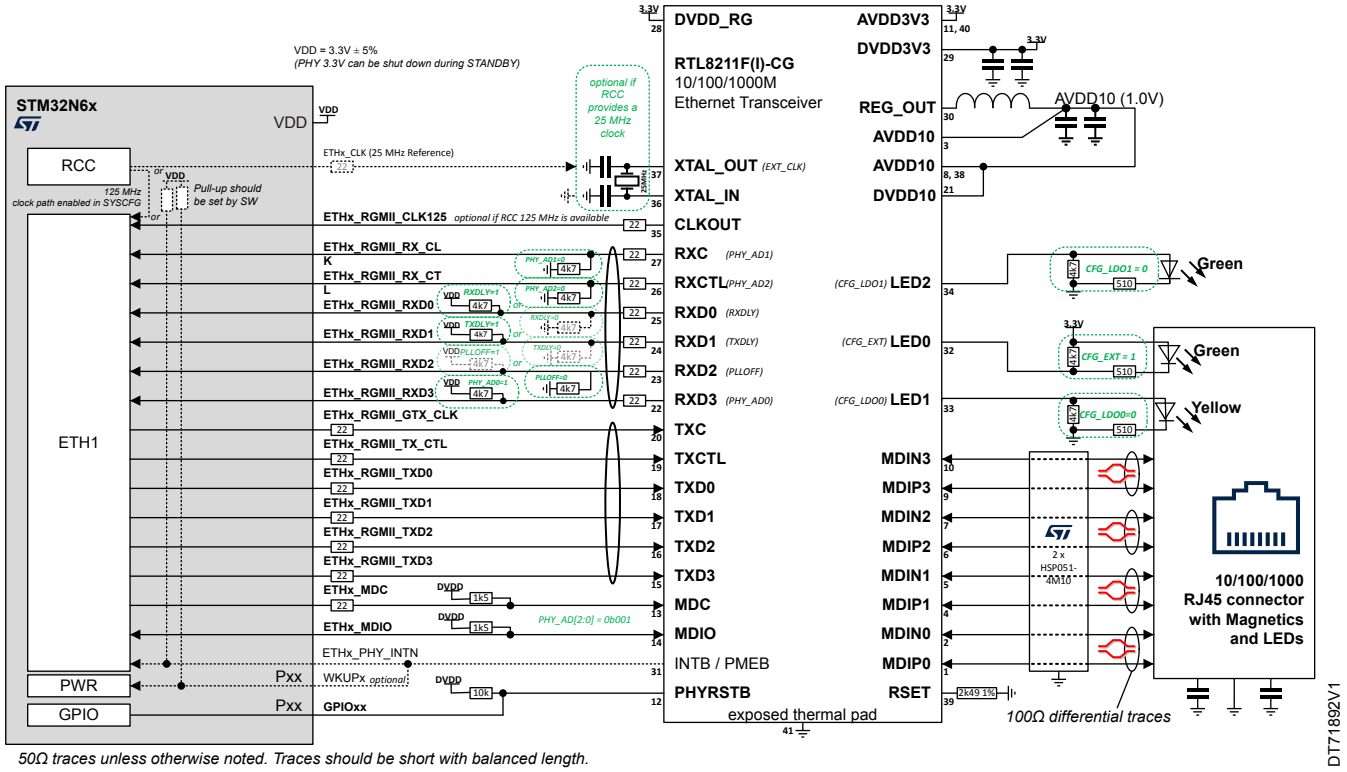
1. *→ MPU to PHY, ← PHY to MPU.*
2. *Can also be used as ETHSW port2. ETHSW is not available on some part numbers.*
3. *Not available on some part numbers.*
4. *Equivalent to ETHSW port1.*
5. *If needed, ETH1_CLK must be used.*
6. *As RCC cannot provide the reference clock to the PHY in low-power modes, a dedicated 25 MHz crystal is required on the PHY if "wake-up on LAN" (WOL) is needed for the platform.*
7. *ETH3 PHY share THE same MDC/MDIO pins as ETH1 PHY (need to use different address for the PHY).*

13.4.2 Gigabit Ethernet

Note: Good signal integrity is dependent on the board, GPIO strength settings (GPIO_OSPEEDR registers), and V_{DD} voltage.

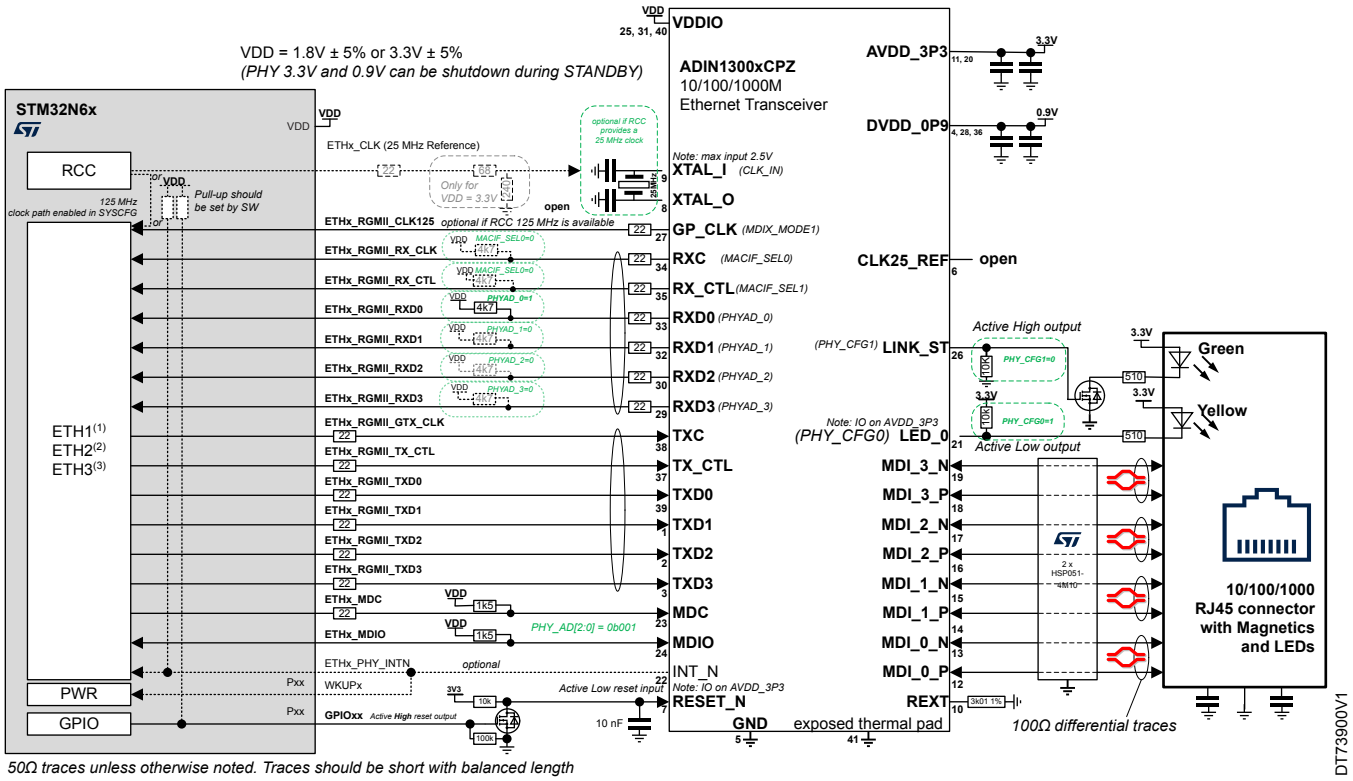
When using V_{DD} = 1.8 V, setting VDDIOxRSEL can be required to ensure the adequate speed on pins used on ETHx outputs. If needed, the impedance matching resistors must be placed as close as possible to the output driver pin. The values in the example below work in most cases, but can be tailored to the I/O drive strengths and PCB impedance of each side.

Figure 13. Gigabit Ethernet PHY connection with VDD = 3.3 V (RTL8211F)



50Ω traces unless otherwise noted. Traces should be short with balanced length.

Figure 14. Gigabit Ethernet PHY connection (ADIN1300xCPZ)



50Ω traces unless otherwise noted. Traces should be short with balanced length

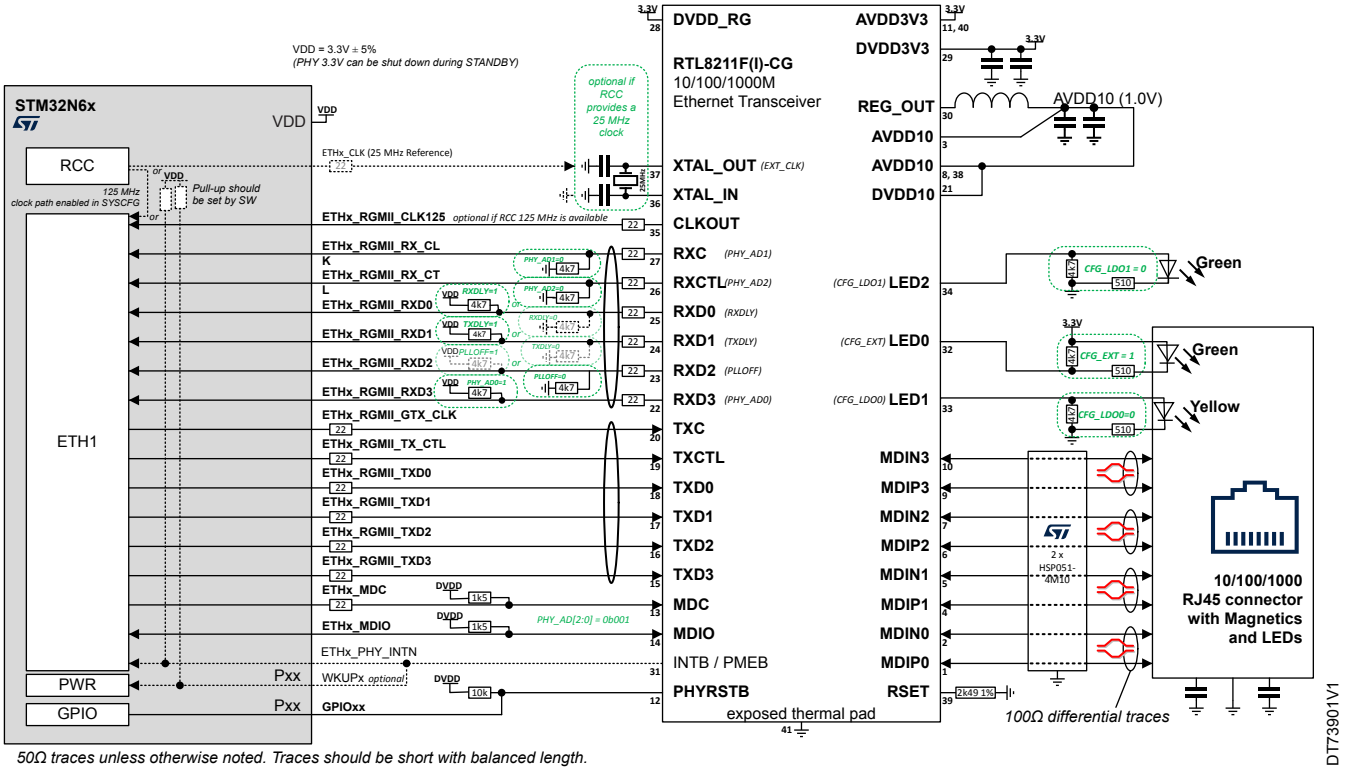
Note:

1. *ETH1 is either ETH1 direct or ETHSW port2 (ETHSW is not available on some part numbers).*
2. *ETH2 is not available on some part numbers.*
3. *ETH3 is ETHSW port1. ETHSW is not available on some part numbers.*
4. *Decoupling capacitors are not shown.*

As RCC cannot provide the 25 MHz reference clock to the PHY in low-power modes, the dedicated 25 MHz crystal is required on the PHY in case "wake-up on LAN" (WOL) is needed for the platform.

Setting RCC PLLs to get 25 MHz output for PHY can constrain other RCC frequencies. In that case, it is more flexible to put a dedicated 25 MHz crystal on the PHY.

Figure 15. Gigabit Ethernet PHY connection with V_{DD} = 1.8 V (RTL8211F)



Note:

1. *ETH1 is either ETH1 direct or ETHSW port2 (ETHSW is not available on some part numbers).*
2. *ETH2 is not available on some part numbers.*
3. *ETH3 is ETHSW port1. ETHSW is not available on some part numbers.*
4. *Decoupling capacitors are not shown.*

As RCC cannot provide the 25MHz reference clock to the PHY in low-power modes, the dedicated 25 MHz crystal is required on the PHY in case "wake-up on LAN" (WOL) is needed for the platform.

Setting RCC PLLs to get 25 MHz output for PHY can constrain other RCC frequencies. In that case, it is more flexible to put a dedicated 25 MHz crystal on the PHY.

Table 12. ETH RGMII pins

Pin name	Signal direction(1)	ETH1 (2)	ETH2 (3)	ETH3 (3)(4)	comments
ETHx_CLK	→	PF3, PF5, PF8	PF4, PG3	-(5)	Optional 25 MHz reference (6)
ETHx_RGMII_CLK125	←	PC4, PH9	PF8, PG2	-(7)	Optional if 125 MHz is fed internally from RCC to ETH IP
ETHx_RGMII_RX_CLK	←	PA14	PC0, PF6	PA5	-
ETHx_RGMII_RX_CTL	←	PA11	PC3, PF8	PA2	-
ETHx_RGMII_RXD0	←	PF1	PG0	PA9	-
ETHx_RGMII_RXD1	←	PC2	PC12	PA10	-
ETHx_RGMII_RXD2	←	PG0, PH12	PA0, PF9	PH7	-
ETHx_RGMII_RXD3	←	PC12, PH13	PC11, PG1	PH8	-
ETHx_RGMII_GTX_CLK	→	PC0	PF7	PH2	-
ETHx_RGMII_TX_CTL	→	PA13	PC4	PA3	-
ETHx_RGMII_TXD0	→	PA15	PC7	PA6	-
ETHx_RGMII_TXD1	→	PC1	PC8	PA7	-
ETHx_RGMII_TXD2	→	PC7, PH10	PC9, PF10	PH6	-
ETHx_RGMII_TXD3	→	PC8, PH11	PC10, PF11	PH3	-
ETHx_MDC	→	PA9, PF0, PF4	PC6, PG4, PH10	-(8)	-
ETHx_MDIO	→ ←	PA10, PF2, PF5	PC5, PF9, PH11	-(8)	-
ETHx_PHY_INTN	←	PA12, PC6, PF5	PF5, PG3	PA1	Optional

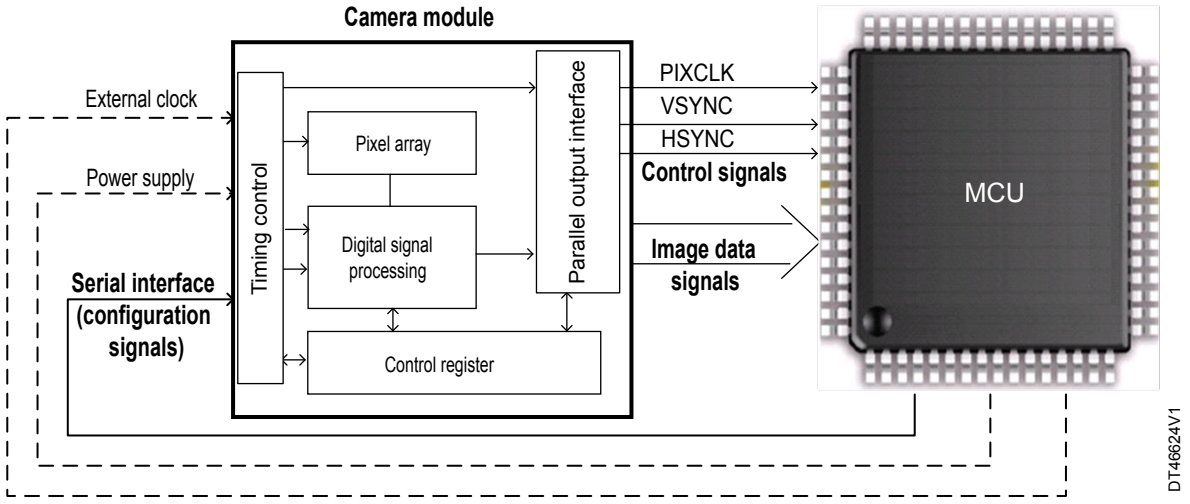
1. *→ MPU to PHY, ← PHY to MPU.*
2. *Can also be used as ETHSW port2. ETHSW is not available on some part numbers.*
3. *Not available on some part numbers.*
4. *Equivalent to ETHSW port1.*
5. *If needed, ETH1_CLK must be used.*
6. *As RCC cannot provide the reference clock to the PHY in low-power modes, a dedicated 25 MHz crystal is required on the PHY if "wake-up on LAN" (WOL) is needed for the platform.*
7. *If needed, ETH1_RGMII_CLK125 must be used.*
8. *ETH3 PHY share the same MDC/MDIO pins than ETH1 PHY (need to use a different address for the PHY).*

13.5 Camera serial interface

As pixel data received by the camera serial interface (CSI) are processed by DCMIPP, the parallel high-resolution sensor interface is not available when using CSI. In that case, a second parallel low-performance sensor is still possible using DCMI. Refer to the reference manual for details.

A 200 Ω 1% resistor must connect CSI_REXT and V_{SS}.

Figure 16. CSI example



Note: *1. Supplies and decoupling capacitors are not shown.*
2. Image sensor controls are not shown (I2C for control, autofocus, and so on).

Table 13. CSI PCB routing recommendations

Recommendation	Min	Typ	Max	Unit
Differential impedance	90	100	110	Ω
Single-ended impedance	45	50	55	Ω
Length matching within a pair (including package	-5	-	+5	mils
	-0.127	-	+0.127	mm
Length matching between clock and data pairs	-100	-	+100	mils
	-2.54	-	+2.54	mm
Max link length (including camera module cables)	-	-	8	inches
	-	-	203	mm
Max number of vias (recommended value)	-	-	2	-
Distance between any differential trace and other signals	S-2S	S-3S or more		-
Do no route over a power plane split. No stubs (point to point only). No right angles				

14 Recommended PCB routing guidelines for STM32N6x5 and STM32N6x7

14.1 PCB stack-up

To reduce the reflections on high-speed signals, the impedance between the source, sink, and transmission lines have to be matched. The impedance of a signal trace depends on its geometry and its position with respect to any reference plane.

The trace width and spacing between differential pairs for a specific impedance requirement is dependent on the chosen PCB stack-up. As there are limitations in the minimum trace width and spacing, which depend on the type of the PCB technology and cost requirements, a PCB stack-up needs to be chosen which addresses all the impedance requirements.

The minimum configuration that can be used is four or six layers stack-up. An eight-layer board may be required for very dense PCBs that have multiple SDRAM/SRAM/NOR/LCD components. The following stack-ups (See the two figures below) are intended as examples, which can be used as guide lines for a stack-up evaluation and selection.

These stack-up configurations place the GND plane next to the power plane to increase the capacitance and reduce the physical gap between GND and the power plane. So, high-speed signals on the top layer have a solid GND reference plane, which helps reduce the EMC emissions. Therefore, moving up in the layers and having a GND reference for each PCB signal layer improves the radiated EMC performance.

Figure 17. Layer PCB stack-up

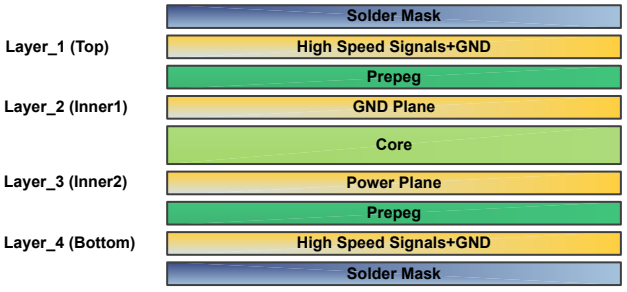
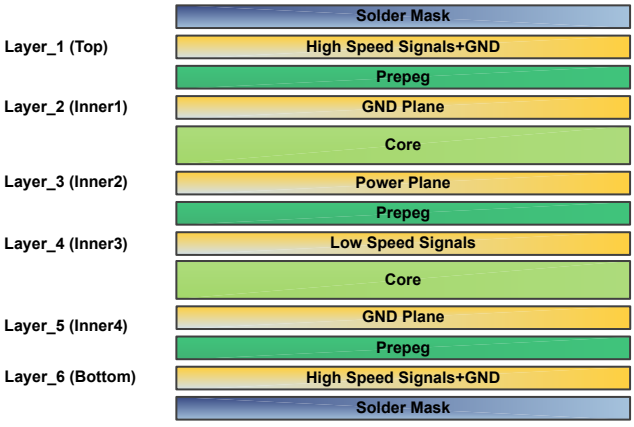


Figure 18. Six layer PCB stack-up example



14.2 Crystal oscillator

For further guidance on how to layout and route crystal oscillator circuits, refer to the application note AN2867.

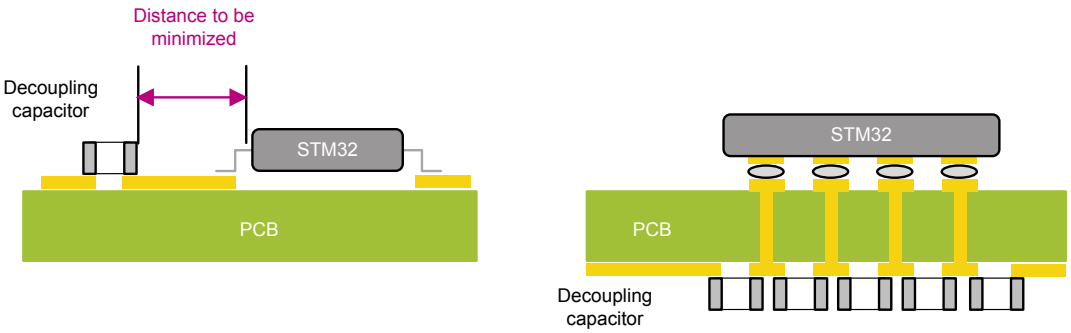
14.3 Power supply decoupling

An adequate power decoupling for STM32N6 MCUs is necessary to prevent excessive power and ground bounce noise. Refer to Table 4. Power supply pins.

The following recommendations must be followed:

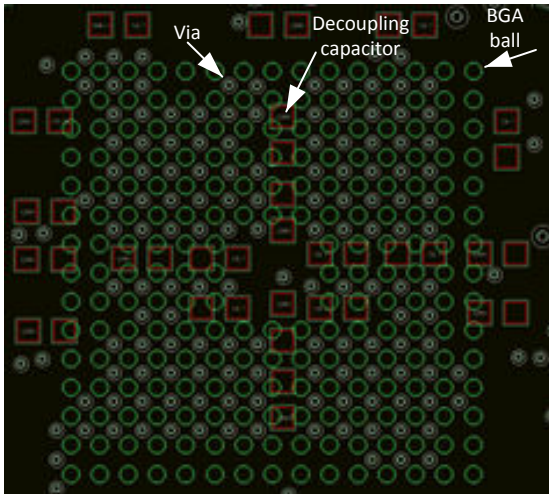
- Place the decoupling capacitors as close as possible to the power and ground pins of the MCU. For BGA packages, it is recommended to place the decoupling capacitors on the opposing side of the PCB (see Figure 19. Decoupling capacitor placement depending on package type. Decoupling capacitor placement depending on package type).
- Add the recommended decoupling capacitors to as many V_{DD}/V_{SS} pairs as possible.
- Connect the decoupling capacitor pad to the power and ground plane with a wide and short trace/via. This reduces the series inductance, maximizes the current flow, and minimizes the transient voltage drops from the power plane and in turn reduces the ground bounce occurrence.

Figure 19. Decoupling capacitor placement depending on package type



The figure below shows an example of decoupling capacitor placement underneath the STM32N6 MCU, closer to the pins and with fewer vias.

Figure 20. Example of decoupling capacitor placed underneath



14.4 High-speed signal layout

14.4.1 SDMMC bus interface

Interface connectivity

The SD/SDIO MMC card host interface (SDMMC) provides an interface between the AHB peripheral bus and multimedia cards (MMCs), SD memory cards, and SDIO cards.

The SDMMC interface is a serial data bus interface that consists of a clock (CK), command signal (CMD), and eight data lines (D[0:7]).

Interface signal layout guidelines

- Reference the plane using GND or PWR (if PWR, add a 10 nf switching cap between PWR and GND).
- Trace impedance: 50 Ω ± 10%.
- All clock and data lines must have equal lengths to minimize any skew.
- The maximum skew between data and clock must be less than 250 ps @ 10 mm.
- The maximum trace length must be less than 120 mm. If the signal trace exceeds this trace-length/speed criteria, then a termination must be used.
- The trace capacitance must not exceed 20 pF at 3.3 V and 15 pF at 1.8 V.
- The maximum signal trace inductance must be less than 16 nH.
- Use the recommended pull-up resistance for CMD and data signals to prevent the bus from floating.
- The mismatch within data bus, data, and CK or CK and CMD must be below 10 mm.
- All data signals must have the same number of vias.

*Note: The total capacitance of the SD memory card bus is the sum of the bus controller capacitance CHOST, the bus capacitance CBUS itself and the capacitance CCARD of each card connected to this line. The total bus capacitance is CL= CHost + CBus + N*CCard where the host is an STM32N6, the bus is all the signals, and the Card is an SD card.*

The figures below show different typical use cases.

Figure 21. microSD™ card interconnection example

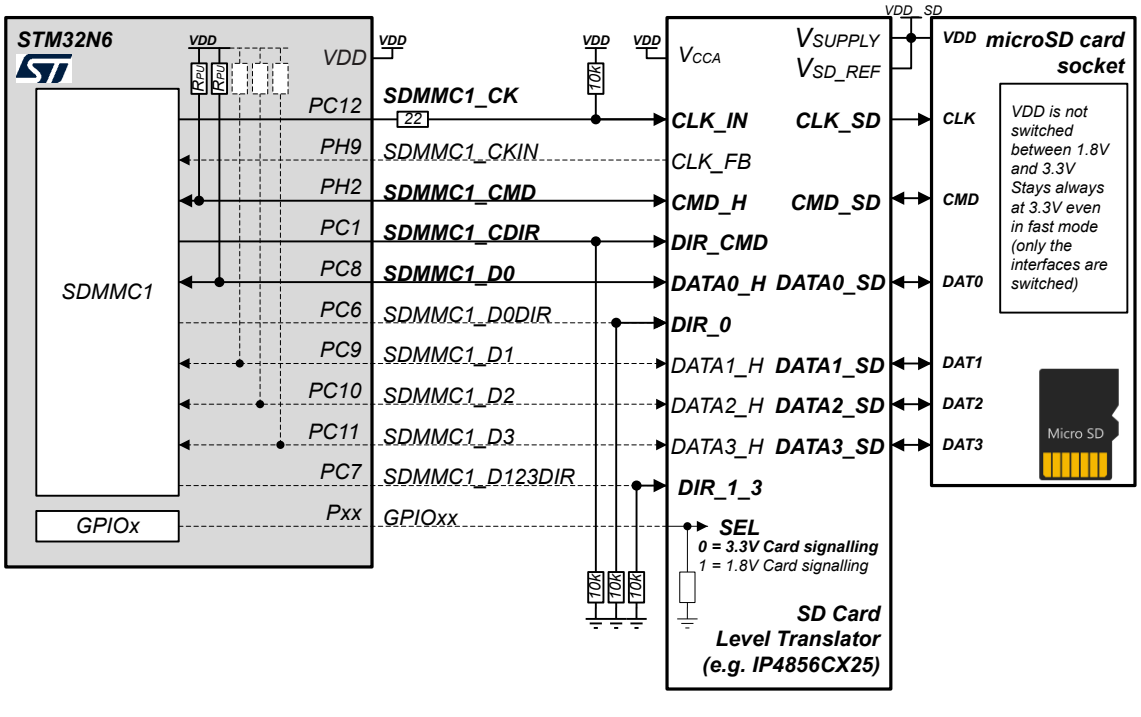
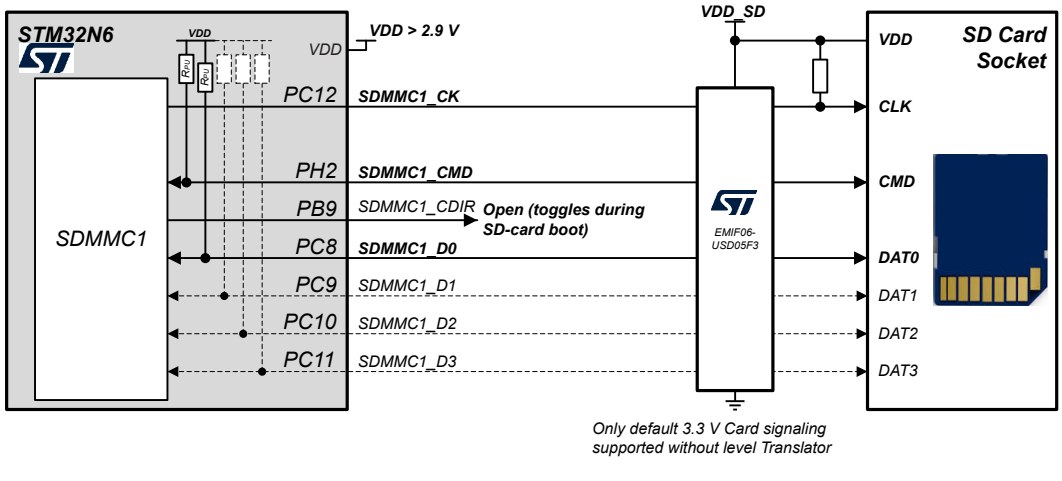


Figure 22. SD card interconnection example



14.4.2 Flexible memory controller (FMC) interface

Interface connectivity

The flexible memory controller (FMC) includes three memory controllers:

- The NOR/PSRAM memory controller
- The NAND memory controller
- The synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) controller

The main purposes of the FMC are:

- To translate AXI transactions into the appropriate external device protocol
- To meet the access time requirements of the external memory devices

All external memories share the addresses, data, and control signals with the controller. Each external device is accessed by means of a unique chip select. The FMC performs only one access at a time to an external device. The main features of the FMC are the following:

- Interface with static-memory mapped devices including:
  - Static random-access memory (SRAM)
  - NOR flash memory/OneNAND flash memory
  - PSRAM (four memory banks)
  - NAND flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-,16-,32-bit data bus width
- Independent chip select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is the FMC kernel clock divided by two.

Interface signal layout guidelines

- For reference the plane using GND or PWR (if PWR), add 10 nf stitching cap between PWR and GND.
- Trace impedance: 50 Ω ± 10%.
- The maximum trace length must not exceed 120 mm. If the signal trace exceeds this trace-length / speed criteria, then a termination must be used.
- To reduce the crosstalk, it is strongly recommended to place data tracks on the different layers to the address and control lanes. However, when the data and address / control tracks coexist on the same layer they must be separated from each other by at least 5 mm.
- Match the trace lengths for the data group within ± 10 mm of each other to reduce any excessive skew.
- Serpentine traces (this is an “S” pattern to increase trace length) can be used to match the lengths.
- Placing the clock (SDCLK) signal on an internal layer, minimizes the noise (EMI). Route the clock signal at least three times the width of the trace away from other signals. To avoid unnecessary impedance changes and reflection, avoid the use of vias as much as possible. Serpentine routing is to be avoided also.
- Match the clock traces to the data/address group traces length to within ±10 mm.
- Match the clock trace length to each signal trace in the address and command groups to within ±10 mm (with maximum of ≤ 20 mm).
- Trace capacitances:
  - At 3.3 V, keep the trace capacitance within 20 pF with overall capacitive loading (including data address, SDCLK, and control) to no more than 30 pF.
  - At 1.8 V, keep the trace capacitance within 15 pF with overall capacitive loading (including data, address, SDCLK, and control) to no more than 20 pF.

14.4.3 Extended-SPI interface (XSPI)

The XSPI interface provides communication with external high-speed volatile and nonvolatile memories. Thanks to its flexibility, it supports single-SPI, dual-SPI, quad-SPI, octo-SPI, and 16-bit protocol memories providing high performance, low pin count, and PCB design cost.

A dedicated external power supply for octo-SPI and hexa-SPI interfaces is available.

XSPI I/O manager (XSPIM)

The user can set a fully programmable premapping of the XSPI1 and XSPI2 ports signals with the XSPI I/O manager (XSPIM). It connects up to 16-bit external memory on the port 1, and up to 8-bit external memory on the port 2.

In direct mode, each XSPI directly drive the corresponding port (XSPI1 mapped to port 1, XSPI2 mapped to port 2). In Figure 23. XSPI direct mode example, a 16-bit SPI memory is connected to port 1 while an octo-SPI memory is connected to port2.

In swapped mode, the XSPI2 can be configured in 16-bit mode, and the XSPI1 can be configured in octal mode, to connect an external 16-bit memory on port 1, and to connect in a concurrent way an octal external memory connected to port 2 of the I/O manager.

In multiplexed mode, only one output port is used to access two memories. Each memory requests a dedicated chip select. The arbiter in the IO manager manages the access of XSPI1 and XSPI2 to the targeted memory. The external memories can be two separate chips or embedded in a single multichip package.

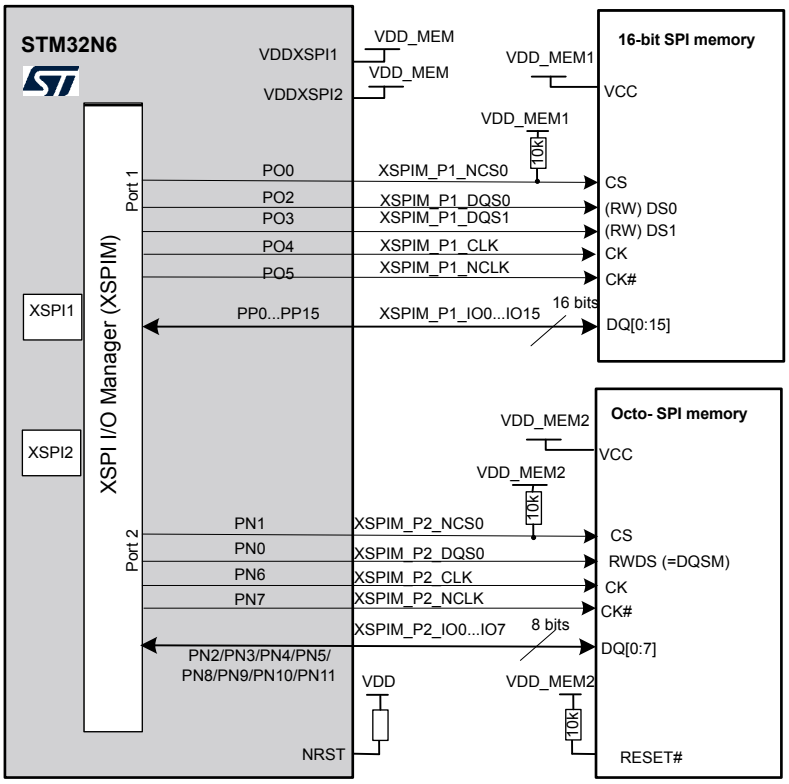
The multiplexed mode can be very useful for some packages where the port2 (or port1) is not mapped. In Figure 24. XSPI multiplexed interconnection example , the same bus of port 1 is shared between two external 16-bit SPI memories.

For additional descriptions of use cases, refer to the XSPI I/O manager (XSPIM) section in the document .

Interface signal layout guidelines

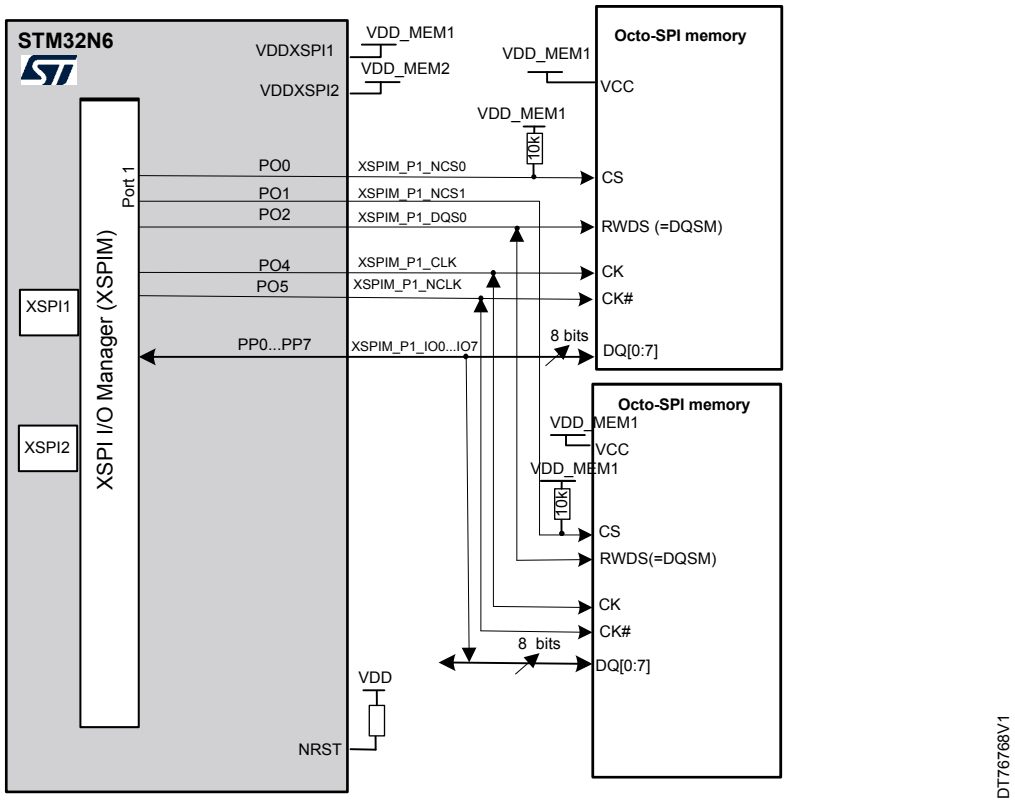
- Reference the plane using GND or PWR (if PWR, add 10 F stitching capacitor between PWR and GND).
- Trace impedance: 50 Ω for single-ended and 100 Ω for differential pairs (CLK/NCLK).
- The maximum trace length must be less than120 mm. If the signal trace exceeds this trace-length/speed criterion, then a termination must be used.
- Avoid using multiple signal layers for the data signal routing.
- Route the clock signal at least three times the width of the trace away from other signals. To avoid unnecessary impedance changes and reflection, avoid the use of vias as much as possible. Serpentine routing is to be avoided also.
- Match the trace lengths for the data group within ± 10 mm of each other to reduce any excessive skew.
- Serpentine traces (this is an “S” shape pattern to increase trace length) can be used to match the lengths.
- Avoid using a serpentine routing for the clock signal and use via(s) as little as possible for the whole path. A via alters the impedance and adds a reflection to the signal.
- Avoid discontinuities on high speed traces. Such as vias and SMD components. If SMD components are needed, place these components symmetrically to ensure good signal quality

Figure 23. XSPI direct mode example



Note: Two octo-SPI memories accessed in XSPI dual octal mode can replace the 16-bit SPI memory.

Figure 24. **XSPI multiplexed interconnection example**



Note: V_{DD}, V_{DD_MEM1}, V_{DD_MEM2} supply voltage names are completely independent.

14.4.4 ADF interface

The audio digital filter (ADF) is a high-performance module dedicated to the connection of external sigma-delta (ΣΔ) modulators, and specially the digital microphones. It is mainly targeted for the following applications: audio capture signals, metering. The ADF features one digital serial interface (SITF0) and one digital filter (DFLT0) with flexible digital processing options in order to offer up to 24-bit final resolution.

The ADF serial interface supports several standards allowing the connection of various ΣΔ modulator sensors: SPI interface, Manchester coded 1-wire interface, PDM interface. For further information, refer to the reference manual RM0486.

14.4.5 Embedded trace macrocell (ETM)

Interface connectivity

The ETM enables the reconstruction of the program execution. The data is traced using the data watchpoint and trace (DWT) component or the instruction trace macrocell (ITM) whereas instructions are traced using the embedded trace macrocell (ETM). The ETM interface is synchronous with the four data bus lines D[0:3] and the clock signal CLK.

Interface signals layout guidelines:

- Reference the plane using GND or PWR (if PWR, add 10 F stitching capacitor between PWR and GNDTrace impedance: 50 Ω ± 10%.
- All the data traces must be as short as possible (≤25 mm).
- Trace the lines, which must run on the same layer with a solid ground plane underneath it without vias.
- Trace the clock, which must have only a point-to-point connection. Any stubs must be avoided.

It is strongly recommended also for other (data) lines to be point-to-point only. If any stubs are needed, they must be as short as possible. If long stubs are required, there must be a possibility to optionally disconnect them (for example, by jumpers).

Revision history

Table 14. Document revision history

Date	Version	Changes
28-Nov-2024	1	Initial release
12-May-2025	2	Updated document title. Changed all V_{CORE} occurrences into V_{DDCORE}. Moved the note concerning ground pins and section *Decoupling power figures* to Section 3.2: Secondary power supplies. Updated list of external devices and Table 4. Power supply pins in Decoupling power figures. Added Section 3.4: System pins. Added STM32N6 power-up sequence and STM32N6 power-down sequence in Section 3.7: System startup. Added Table 7. Package thermal characteristics. Updated Figure 5. STM32CubeMX example screenshot. Replaced VDDIO1 by VDDIO5 in Section 12.4: I/O speed settings and by VDDIO4 in Section 13.2: SD card. Updated list of USB options in Section 13.3: USB. Removed note 1 from Table 13. CSI PCB routing recommendations. Added Section 14: Recommended PCB routing guidelines for STM32N6x5 and STM32N6x7.
28-Aug-2025	3	Updated Section 12.4: I/O speed settings and note in Section 13.3: USB.

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