13. 3:8译码器

LIBRARY IEEE;

USE IEEE.std\_logic\_1164.ALL;

ENTITY decoder\_74LS138 IS

PORT (g1,g2a,g2b,a,b,c : IN std\_logic;

y: OUT std\_logic\_vector(7 DOWNTO 0));

END decoder\_74LS138;

ARCHITECTURE rtl\_arc OF decoder\_74LS138 IS

SIGNAL comb : std\_logic\_vector(2 DOWNTO 0);

BEGIN

comb <= c & b & a;

PROCESS (g1,g2a,g2b,comb)

BEGIN

IF (g1 = '1' AND g2a = '0' AND g2b = '0') THEN

CASE comb IS

WHEN "000" => y <= "11111110";

WHEN "001" => y <= "11111101";

WHEN "010" => y <= "11111011";

WHEN "011" => y <= "11110111";

WHEN "100" => y <= "11101111";

WHEN "101" => y <= "11011111";

WHEN "110" => y <= "10111111";

WHEN "111" => y <= "01111111";

WHEN OTHERS => y <= "XXXXXXXX";

END CASE;

ELSE

y <= "11111111";

END IF;

END PROCESS;

END rtl\_arc;