14． 七段译码器

LIBRARY IEEE;

USE IEEE.STD\_ LOGIC\_ 1164. ALL;

USE IEEE.STD\_ LOGIC UNSIGNED.ALL;

ENTITY DECODER IS

PORT(INP:IN STD\_ LOGIC VECTOR(3 DOWNTO 0);

OUTP:OUT BIT\_ VECTOR (6 DOWNTO 0);

SELIN:IN BIT\_ VECTOR(2 DOWNTO 0);

SELOUT:OUT BIT\_ \_VECTOR(2 DOWNTO 0));

END DECODER; .

ARCHITECTURE ART4 OF DECODER IS

BEGIN

process(inp)

begin

CASE NP IS

WHEN "0000"=>OUTP<= "0111111";

WHEN "0001"=>OUTP<= "0000110";

WHEN "0010"=>OUTP<= "1011011";

WHEN "0011"=>OUTP<= "1001111";

WHEN "0100"=>OUTP<= "1100110";

WHEN "0101"=>OUTP<= "1101101";

WHEN "0110"=>OUTP<= "1111101";

WHEN "0111"=>OUTP<= "0000111";

WHEN "1000"=>OUTP<= "1111111";

WHEN "1001"=>OUTP<= "1101111";

WHEN "1010"=>OUTP<= "1110111";

WHEN "1011"=>OUTP<= "1111100";

WHEN "1100"=>OUTP<= "0111001";

WHEN "1101"=>OUTP<= "1011110";

WHEN "1110"=>OUTP<= "1111001";

WHEN "1111"=>OUTP<= "1110001";

WHEN OTHERS=>NULL;

END CASE;

END PROCESS;

SELOUT<=SELIN;

END ART4;