15. 8/3优先编码器

LIBRARY IEEE;

USE IEEE.STD LOGIC 1164.ALL;

USE IEEE.STD\_ LOGIC\_ UNSIGNED.ALL;

ENTITY ENCODER IS

PORT(

A:IN STD\_ LOGIC\_ VECTOR(0 TO 7);

B:OUT STD\_ LOGIC\_ VECTOR(0 TO 2)

);

END

ARCHITECTURE encoder\_arc OF ENCODER IS

BEGIN

PROCESS(A)

BEGIN

IF

(A(7)='0')THEN B<="1l1";

ELSIF (A(6)='0')THEN B<="110";

ELSIF (A(5)='0')THEN B<="101";

ELSIF (A(4)='0')THEN B<="100";

ELSIF (A(3)='0')THEN B<="011";

ELSIF (A(2)='0')THEN B<="010";

ELSIF (A(1)='0')THEN B<="001";

ELSIF (A(0)='0’)THEN B<="000";

ELSE B<="ZZZ";

END IF;

END PROCESS;

END;