**21. 有限状态机**

**LIBRARY IEEE;**

**USE IEEE.std\_logic\_1164.ALL;**

**ENTITY FSM IS**

**PORT (clk k: IN std\_logic;**

**s0,s1,s2,s3 : OUT std\_logic);**

**END store\_controller;**

**ARCHITECTURE state\_machine OF FSM IS**

**TYPE state\_type IS (S0,S1,S2,S3);**

**SIGNAL state : state\_type;**

**BEGIN**

**one\_process:PROCESS (clk)**

**BEGIN**

**IF (clk'event AND clk =‘0') THEN**

**CASE state IS**

**WHEN S0 => IF (k ='1') THEN**

**state <= S0;**

**ELSE**

**state <= S1;**

**END IF;**

**WHEN S1 => IF (k='1') THEN**

**state <= S2;**

**ELSE**

**state <= S1;**

**END IF;**

**WHEN S2 => IF (k ='1') THEN**

**state <= S2;**

**ELSE**

**state <= S3;**

**END IF;**

**WHEN S3 => IF (k ='1') THEN**

**state <= S0;**

**ELSE**

**state <= S3;**

**END IF;**

**END CASE;**

**END IF;**

**END PROCESS;**

**s0 <= '1' WHEN state = S0 ELSE '0';**

**s1 <= '1' WHEN state = S1 ELSE '0';**

**s2 <= '1' WHEN state = S2 ELSE '0';**

**s3 <= '1' WHEN state = S3 ELSE '0';**

**END state\_machine;**