**本科试题（三）**

**一、选择题（每小题2分，共20分。）**

1．与最小项表达式F(A,B,C)=m0+m3+m4+m7相等的逻辑函数为（ ）。

A. ***F=B⊙C*** B.  C.  D.***F=∑(0,4)***

2．证明成立的最简单方法是依据以下哪种定律或规则？（ ）

A. 对偶规则 B. 分配律 C.反演规则 D.多余项定律

3．2421BCD码为（10111111）2421BCD，与其相等的十进制数是（ ）。

A.(277)10 B.(82)10 C. (59)10 D. (1115)10

4． 一个四输入端与非门，使其输出为0的输入变量取值组合有（ ）种。

A. 15 B. 8 C. 7 D. 1

5． （ ）电路在任何时刻只能有一个输入端有效。

A.普通二进制编码器 B.优先编码器 C.七段显示译码器 D. 二进制译码器

6．中规模集成计数器都具有规定的模值，但可以用（ ）来构成任意进制计数。

A.复0和复9 B.置数法和复位法 C.改变输入法 D. 控制CP脉冲

7．数字系统级的设计与逻辑部件级设计分别采用（ ）的设计方法。

A. 自上而下、自上而下 B. 自下而上、自下而上

C. 自上而下、自下而上 D. 自下而上、自上而下

8．使用ROM和PLA实现组合逻辑时，要将逻辑表达式分别写成（ ）。

A. 最小项之和、最小项之和 B. 最简与-或式、最简与-或式

C. 最简与-或式、最小项之和 D. 最小项之和、最简与-或式

9. 下列时序电路状态转移表中，具有自启动功能的是（ ）。

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| |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | PS | | | NS | | | | Q3 | Q2 | Q1 | Q3 | Q2 | Q1 | | 0 | 1 | 0 | 0 | 0 | 1 | | 0 | 0 | 1 | 0 | 1 | 1 | | 0 | 1 | 1 | 1 | 1 | 1 | | 1 | 1 | 1 | 1 | 0 | 0 | | 1 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 1 | 0 | | 1 | 1 | 0 | 1 | 0 | 1 | | 1 | 0 | 1 | 1 | 1 | 0 | |

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| |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | PS | | | NS | | | | Q3 | Q2 | Q1 | Q3 | Q2 | Q1 | | 0 | 1 | 0 | 0 | 0 | 1 | | 0 | 0 | 1 | 0 | 1 | 1 | | 0 | 1 | 1 | 1 | 1 | 1 | | 1 | 1 | 1 | 1 | 0 | 0 | | 1 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 1 | 0 | | 1 | 1 | 0 | 1 | 0 | 1 | | 1 | 0 | 1 | 1 | 0 | 0 | |

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| |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | PS | | | NS | | | | Q3 | Q2 | Q1 | Q3 | Q2 | Q1 | | 0 | 1 | 0 | 0 | 0 | 1 | | 0 | 0 | 1 | 0 | 1 | 1 | | 0 | 1 | 1 | 1 | 1 | 1 | | 1 | 1 | 1 | 1 | 0 | 0 | | 1 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 1 | 0 | | 1 | 1 | 0 | 1 | 1 | 0 | | 1 | 0 | 1 | 1 | 0 | 1 | |

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| A. 表1 |

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| B. 表2 |

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| --- |
| C. 表3 |

10. 寻址容量为16K×8的RAM需要 根地址线。( )

A.14 B.16 C.18 D.20

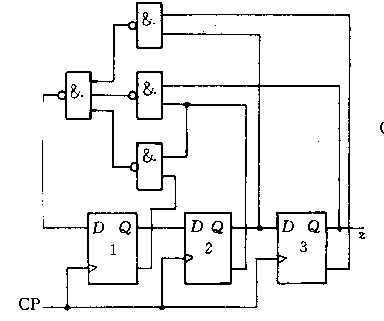
**二、简答题（各5分，共10分）**

1、简单描述VHDL语言程序基本结构所包含的五个部分。（5分）

1. 简单描述SRAM和DRAM存储元的存储机理。（5分）

**三、时序电路分析题（10分）**

试分析如图所示电路的功能  
（1）写出电路的输出函数、激励函数、状态方程。  
（2）写出状态表、画出状态图。  
（3）写出电路的功能。



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| Z |

**四、组合电路设计（10分）**

设计一个如图7所示六段显示的驱动译码器。它是为了显示图7所示的六个符号中的一个，实线表示亮，虚线表示不亮（图中e是垂直线，f是水平线）。设计的器件有三个输入A、B、C及六个输出a、b、c、d、e、f。图中表示的三位数是输入码，即译码器接收三位码，使适当的段亮。每一段的驱动电位是高电平。没有给出的码作为无关项。

1、列真值表。

2、求最简逻辑表达式。（卡诺图）

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| a |

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| b |

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| c |

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| --- |
| d |

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| --- |
| f |

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| --- |
| e |

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| --- |
| 东000 |

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| --- |
| 南001 |

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| --- |
| 西010 |

|  |
| --- |
| 北011 |

|  |
| --- |
| +: 100 |

|  |
| --- |
| －: 101 |

|  |
| --- |
| 图7 |

3、画出实现的驱动d段和f段的电路图。可以用与非门和异或门。

**五、时序电路设计（12分）**

用D触发器设计同步五进制计数器。已知状态转换过程的编码是110→011→100→001→101→110。

1、列出状态转移表。

2、写出状态方程。

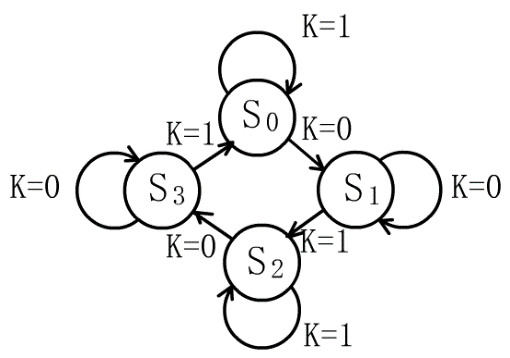
3、写出激励方程。

4、画出逻辑电路图。

5、画出允许自启动的状态转移图。

**六、硬件描述语言设计（14分）**

采用VHDL语言设计一个时序状态机如图所示。



**七、小型控制器设计（14分）**

图9所示为数字累加系统的数据通路图，设计**定序型**控制器。寄存器A从数据总线上接收一系列输入数据，寄存器B保存它们的累加结果，加法器完成求和运算，控制器指挥执行部件自动完成上述运算。其中LDA,LDB为打入寄存器的控制信号，ADD为三态门使能信号。假设累加系统启动之前寄存器A、B已清零。控制器的状态变化发生在T1节拍脉冲时间，打入寄存器操作发生在T2节拍脉冲时间，控制器状态周期为T=T1+T2。

|  |
| --- |
| 控 制 器 |

|  |
| --- |
| LDB |

|  |
| --- |
| 寄存器A |

|  |
| --- |
| 加法器 |

|  |
| --- |
| 寄存器B |

|  |
| --- |
| LDA |

|  |
| --- |
| ADD |

|  |
| --- |
| 数据输入 |

|  |
| --- |
| 图9 |

1、画出控制器的ASM图。

2、列出状态转移真值表。

3、写出激励方程和控制信号表达式。

4、画出定序型控制器电路图。