1. (20pts) Suppose there is a 5-stage pipeline has the following delays for each stage

IF	ID	EX	MEM	WB
250ps	350ps	150ps	300ps	200ps

What is the clock cycle time in a pipelined and non-pipelined processor? Further assuming there are no stalls, what is the speedup achieved by pipelining a single-cycle datapath?

2. (40pts)

Suppose in the basic 5-stage pipeline with the sequence of instructions:

or r1,r2,r3

or r2,r1,r4

or r1,r1,r2

Also, assume the following cycle times for each of the options related to forwarding

Without Forwarding	With Full Forwarding
250ps	300ps

What is the total execution time of this instruction sequence without forwarding and with full forwarding?

What is the speedup achieved by adding full forwarding to a pipeline that had no forwarding?

3. (40 pts)

For the following instruction sequence:

add $3, $1, $2

lw $4,-100($3)

sw $4, 8($3)

a) Assuming there is no forwarding hardware support, find the data hazards and insert nop instructions to eliminate the data hazards.

b) Assuming there is full forwarding hardware support, find the data hazards (if any) and

insert nop instructions to eliminate the data hazards.