1. (a) since the cache has a total of 16 blocks and the addresses are word addresses, the last 4 bits of the address are used for the index.

1	20	2	3	4	18	5	19	33	34	1	4
00001	10100	00010	00011	00100	10010	00101	10011	100001	100010	00001	00100
h	m	h	h	m	m	h	m	m	m	m	h

Hit rate: 5/12

index	
0000	Mem(0)
0001	Mem(1)
0010	Mem(34)
0011	Mem(19)
0100	Mem(4)
0101	Mem(5)
0110	Mem(6)
0111	Mem(7)
1000	Mem(8)
1001	Mem(9)
1010	Mem(10)
1011	Mem(11)
1100	Mem(12)
1101	Mem(13)
1110	Mem(14)
1011	Mem(15)

b. In this case, the lowest 1 bit should be used as word offset and the next lower 3 bits for index since there are 8 sets.

1	20	2	3	4	18	5	19	33	34	1	4
00001	10100	00010	00011	00100	10010	00101	10011	100001	100010	00001	00100
h	m	h	h	m	m	h	h	m	m	m	h

Hit rate: 6/12

index	
000	Mem(1)Mem(0)
001	Mem(35)Mem(34)
010	Mem(5)Mem(4)
011	Mem(7)Mem(6)
100	Mem(9)Mem(8)
101	Mem(11)Mem(10)
110	Mem(13)Mem(12)
111	Mem(15)Mem(14)

c. In this case, the lowest bit is for word offset and the next 2 bits are for index

1	20	2	3	4	18	5	19	33	34	1	4
00001	10100	00010	00011	00100	10010	00101	10011	100001	100010	00001	00100
h	m	h	h	m	m	h	h	m	m	h	h

Hit rate: 7/12

index		
00	Mem(1)Mem(0)	Mem(33)Mem(32)
01	Mem(35)Mem(34)	Mem(19)Mem(18)
10	Mem(21)Mem(20)	Mem(5)Mem(4)
11	Mem(7)Mem(6)	Mem(15)Mem(14)

2. a. AMAT = 2 + (1 – 85%) * 120 = 20 cycles

b. CPIstall= CPIidea + Memory stall cycles

= 1 + (1 - 90%) * 100 + 30% * (1 – 85%) * 120 = 16.4

c. AMAT = 2 + (1 – 85%) * 10 + (1 – 85%) * 95% * 120 = 20.6 cycles

3.

Cycle	IQ	LSQ	ROB
0			
1	lw		
2	add	lw	lw
3	add, sub1	lw	lw, add, sub1
4	add, sub2	lw	lw, add, sub1, sub2
5	add	lw	lw, add, sub1, sub2
6	sub		add, sub1, sub2
7			add, sub1, sub2
8			sub1, sub2
9			sub2
10			