1.

The virtual memory uses a page table to track the mapping of virtual addresses to physical addresses. This question shows how this table must be updated as addresses are accessed. The following data constitutes a stream of virtual addresses as seen on a system. Assume 4 KB pages, a 4-entry fully-associative TLB, and true LRU replacement. If pages must be brought in from disk, increment the next largest page number.

4669, 2227, 13916, 34587, 48870, 12608, 49225

TLB

Valid	Tag	Physical Page Number
1	11	12
1	7	4
1	3	6
0	4	9

Page table

Valid	Physical Page or in Disk
1	5
0	Disk
0	Disk
1	6
1	9
1	11
0	Disk
1	4
0	Disk
0	Disk
1	3
1	12

Given the address stream shown, and the initial TLB and page table states provided above, show the final state of the system. Also list for each reference if it is a hit in the TLB, a hit in the page table, or a page fault.

2.

Repeat question 1, but this time use 16 KB pages instead of 4 KB pages. What would be some of the advantages of having a larger page size? What are some of the disadvantages?

3.

There are several parameters that impact the overall size of the page table. Listed below are key page table parameters.

Virtual Address Size	Page Size	Page Table Entry Size
32bits	8KB	4bytes

Given the parameters shown above, calculate the total page table size for a system as question 1, running 5 applications that utilize half of the memory available.

4.

In this exercise, we will examine space/time optimizations for page tables. T e following list provides parameters of a virtual memory system.

Virtual Address (bits)	Physical DRAM Installed	Page Size	PTE Size (byte)
43	16GB	4KB	4

The following table shows the contents of a 4-entry TLB:

Entry-ID	Valid	VA Page	Modified	Protection	PA Page
1	1	140	1	RW	30
2	0	40	0	RX	34
3	1	200	1	RO	32
4	1	280	0	RW	31

Under what scenarios would entry 2's valid bit be set to zero?

5.

In this exercise, we will examine how replacement policies impact miss rate. Assume a 2-way set associative cache with 4 blocks. To solve the problems in this exercise, you may find it helpful to draw a table like the one below, as demonstrated for the address sequence "0, 1, 2, 3, 4."

Address of Memory Block Accessed	Hit or Miss	Evicted Block	Contents of Cache Blocks After Reference			
			Set0	Set1	Set2	Set3
0	Miss		Mem[0]			
1	Miss		Mem[0]		Mem[1]	
2	Miss		Mem[0]	Mem[2]	Mem[1]	
3	Miss		Mem[0]	Mem[2]	Mem[1]	Mem[3]
4	Miss	0	Mem[4]	Mem[2]	Mem[1]	Mem[3]
…						

Consider the following address sequence: 0, 2, 4, 8, 10, 12, 14, 16, 0

Assuming an LRU replacement policy, how many hits does this address sequence exhibit?

6.

Repeat question 5, assuming an MRU (most recently used) replacement policy, how many hits does this address sequence exhibit?

7.

Cache coherence concerns the views of multiple processors on a given cache block. T e following data shows two processors and their read/write operations on two different words of a cache block X (initially X[0] = X[1] = 0). Assume the size of integers is 32 bits.

P1	P2
X[0] ++; X[1] = 3;	X[0] = 5; X[1] +=2;

List the possible values of the given cache block for a correct cache coherence protocol implementation. List at least one more possible value of the block if the protocol doesn't ensure cache coherency.

8.

Memory consistency concerns the views of multiple data items. T e following data shows two processors and their read/write operations on different cache blocks (A and B initially 0).

P1	P2
A = 1; B = 2; A+=2; B++;	C = B; D = A;

List the possible values of C and D for an implementation that ensures both consistency assumptions on page 470 of the textbook.

9.

Chip multiprocessors (CMPs) have multiple cores and their caches on a single chip. CMP on-chip L2 cache design has interesting trade-of s. T e following table shows the miss rates and hit latencies for two benchmarks with private vs. shared L2 cache designs. Assume L1 cache misses once every 32 instructions.

	Private	Shared
Benchmark A misses-per-instruction	0.30%	0.12%
Benchmark B misses-per-instruction	0.06%	0.03%

Assume the following hit latencies:

Private Cache	Shared Cache	Memory
5	20	180

Which cache design is better for each of these benchmarks? Use data to support your conclusion.

10.

A computer has a 16KB write-back, write-allocate cache and 1MB physical memory. Each cache block is 64B, the cache is 4-way set associative and uses the true LRU replacement policy. Assume a 24-bit virtual address space and byte-addressable memory. The page size is 16KB. The cache uses a virtual tag and physical index. How big (in bits) is the tag store? The cache uses MSI protocol and assume that we need 2 bits to indicate cache coherence states.