计算机科学基础 C

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两种代码

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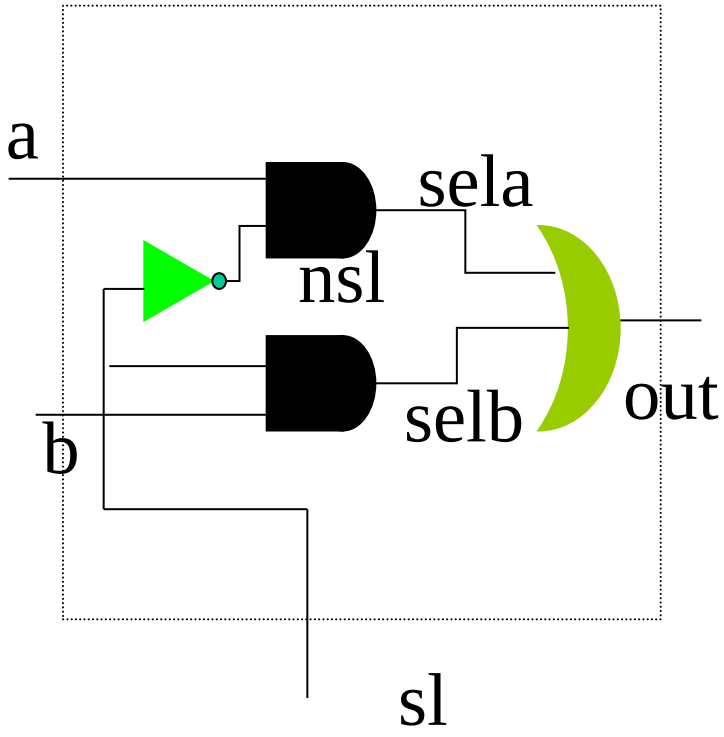
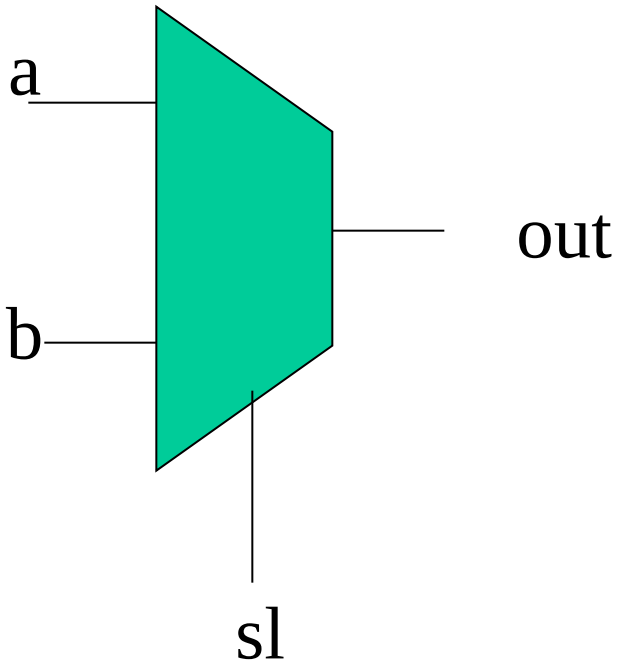
- ✱结构描述
- ✱行为级RTL描述

结构描述




```
module muxtwo (out, a, b, sl);
input a,b,sl;
output out;
not  u1（ns1，sl）；
and  u2（sela，a，nsl）；
and  u3（selb，b，sl）；
or   u4（out，sela，selb）；
endmodule
```

行为描述




```
module muxtwo (out, a, b, sl);
input a,b,sl;
output out;
Reg out;
always @(sl or a or b)
    if (!sl)  out = a;
        else out = b;
endmodule
```

Verilog小、股文

两种代码

❋Module八股

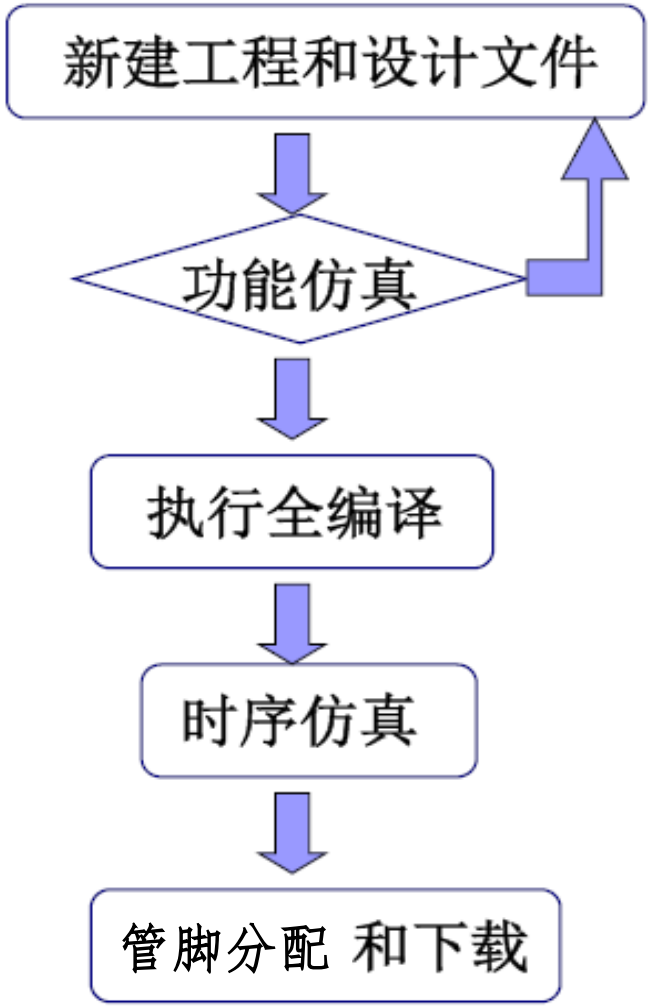
❋Testbench八股

Module八股

1. module 名字 (出入口声明);
2. 出入口方向位宽声明；　　//用于指定input/output
3. reg/wire;　　//always中被赋值的为reg，连线用wire；
4. always块列写时序或组合电路块;
5. assign列写连线或组合电路块
6. endmodule

QuartusII 设计流程

QuartusII 设计流程



硬件描述语言、原理图

建立波形文件
检查逻辑功能是否正确

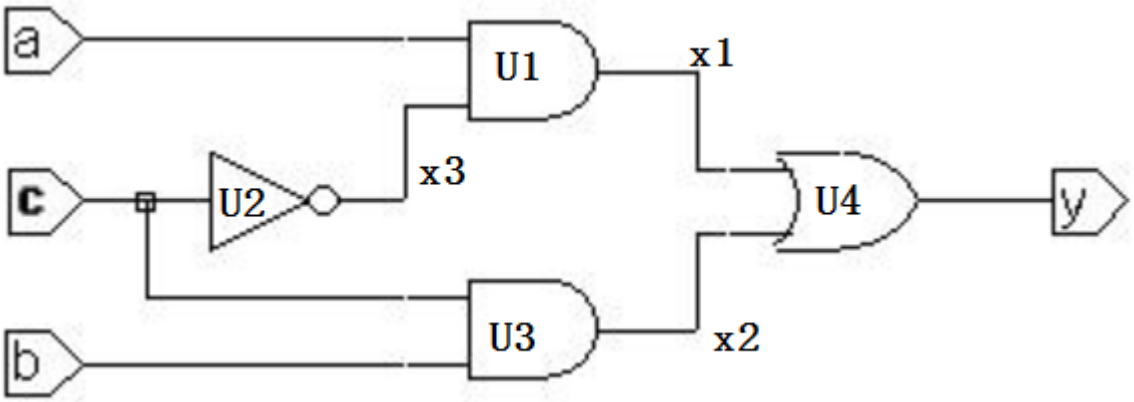
综合、布局布线

验证电路的时序

下载验证

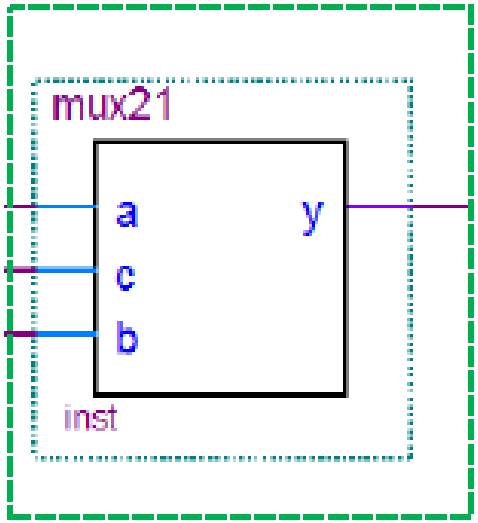
设计一个二选一电路

c为0输出a，c为1输出b



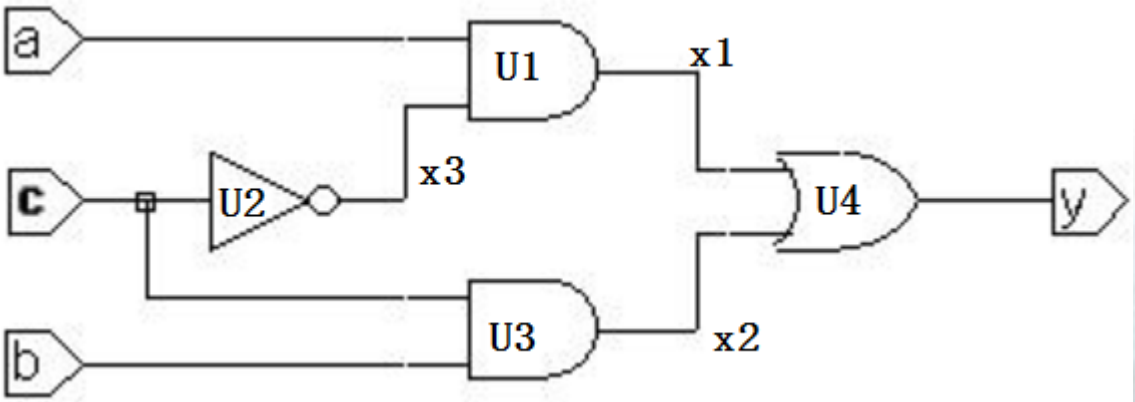
设计一个二选一电路

c为0输出a，c为1输出b




```
module mux21 (a,b,c,y);
  input a,b,c;
  output y;

  assign y=(a&~c)|(b&c);

  endmodule
```

```
module mux21 (a,b,c,y);
  input a,b,c;
  output y;

  wire x1,x2,x3;

  and U1 (x1,a,x3);
  not U2 (x3,c);
  and U3 (x2,c,b);
  or  U4 (y,x1,x2);

endmodule
```



新建工程和设计文件

- 建立工作文件夹和设计工程的文件夹。
- 新建工程向导。
- 新建原理图文件。

  1.添加元件、输入输出引脚

  2.连线

功能仿真

对设计文件进行逻辑功能的测试。
通过观察输入输出波形的关系来检查是否满足设计要求。

- 对设计文件执行分析与综合 
  Processing →Start →Start Analysis and Sythesis

- 建立波形文件，添加待观测信号节点
- 输入激励信号

- 在Simulator Tool中指定功能仿真模式
  Generate Functional Simulation Netlist
- 执行仿真、观察仿真结果

全编译

Processing →Start Compilation 

- 将设计项目适配到指定的目标器件中。
- 产生多种用途的输出文件。如功能和时序信息文件、器件编程的目标文件等。
- 编译成功后，可以读取硬件耗用统计报告、布局布线报告及时序特性报告等信息 。

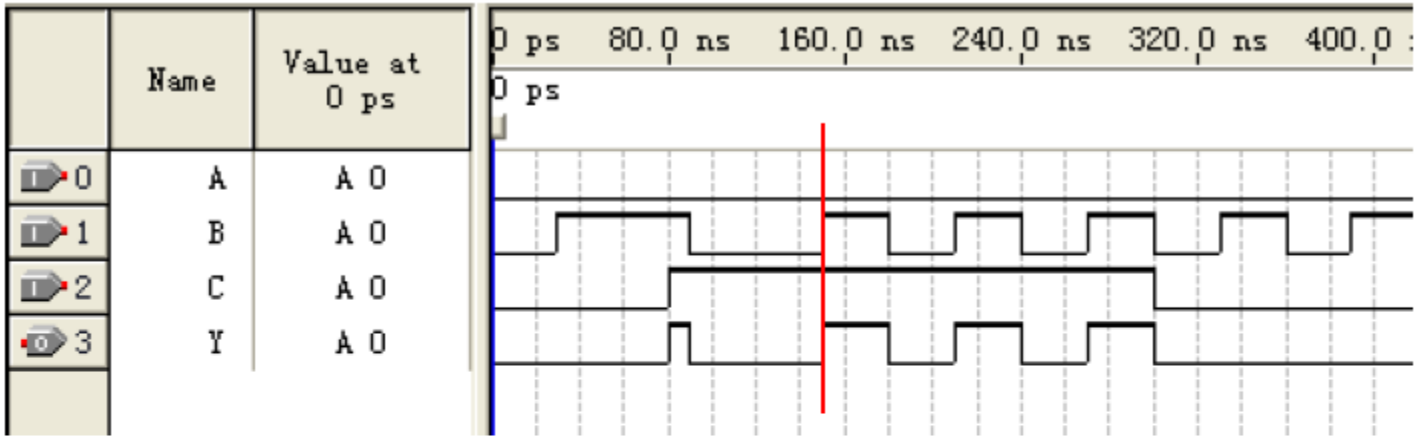
时序仿真

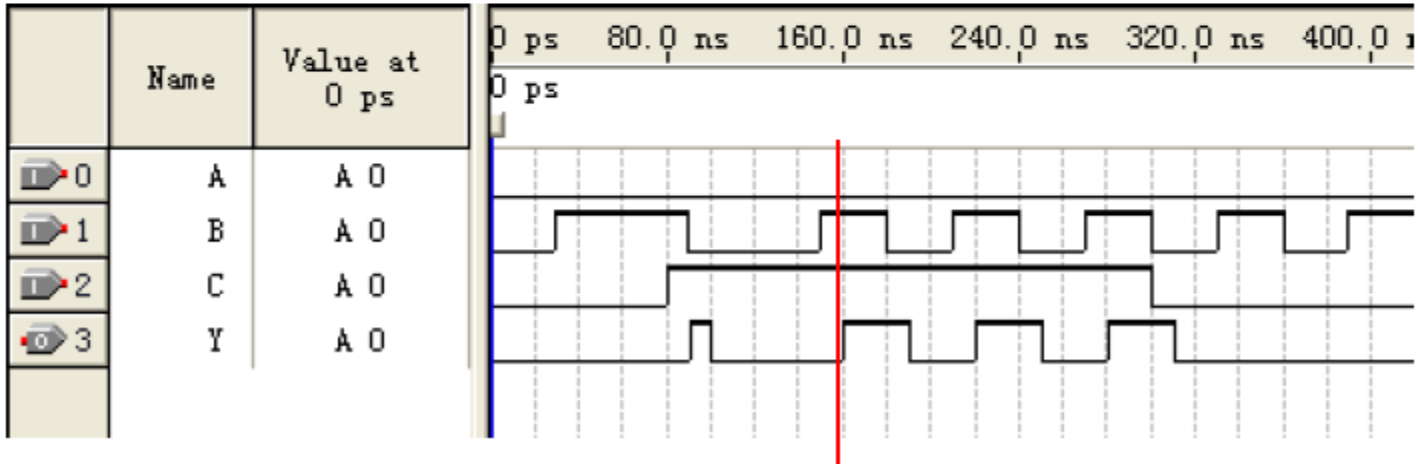
在全编译之后验证设计的时序性能。

- 建立波形文件，添加待观测信号节点
- 输入激励信号

- 在Simulator Tool中指定时序仿真模式。

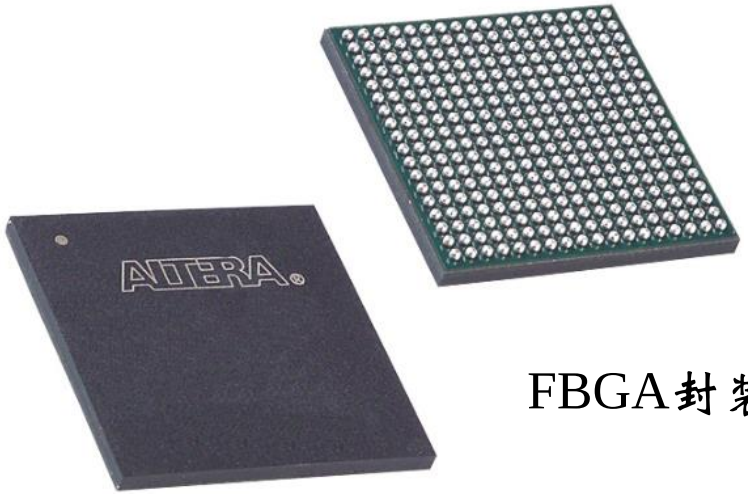
- 执行仿真、观察仿真结果


Name
Value at 0 ps
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0
0 ps
0 A A 0
1 B A 0
2 C A 0
3 Y A 0

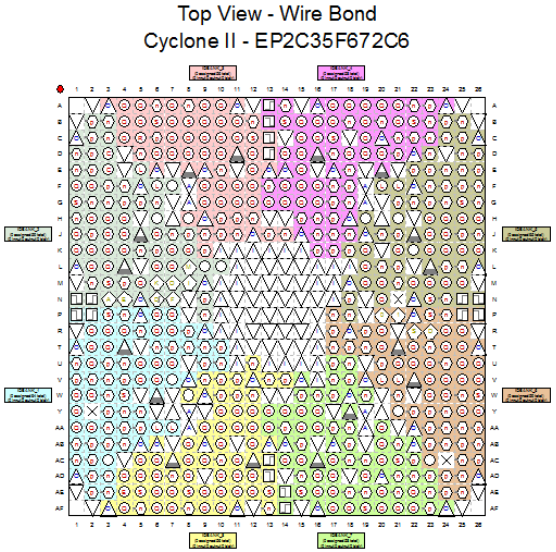

Name
Value at 0 ps
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0
0 ps
0 A A 0
1 B A 0
2 C A 0
3 Y A 0

管脚分配

将设计文件中的输入输出引脚与FPGA芯片的实际引脚相对应起来。



FBGA封装



DE2EP2C35672有475个可用引脚

分配后，再进行一次全编译，管脚信息写入位流文件

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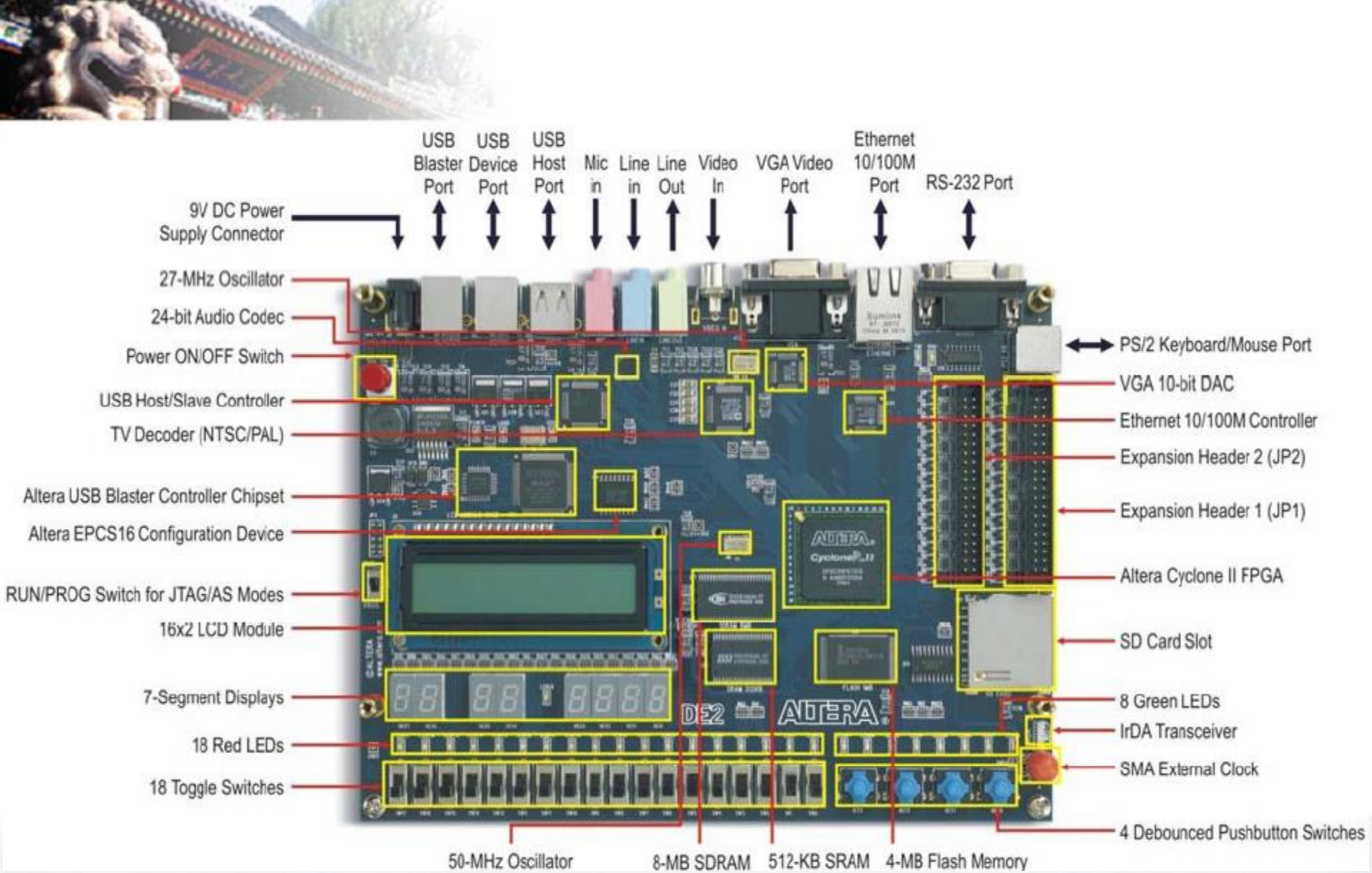
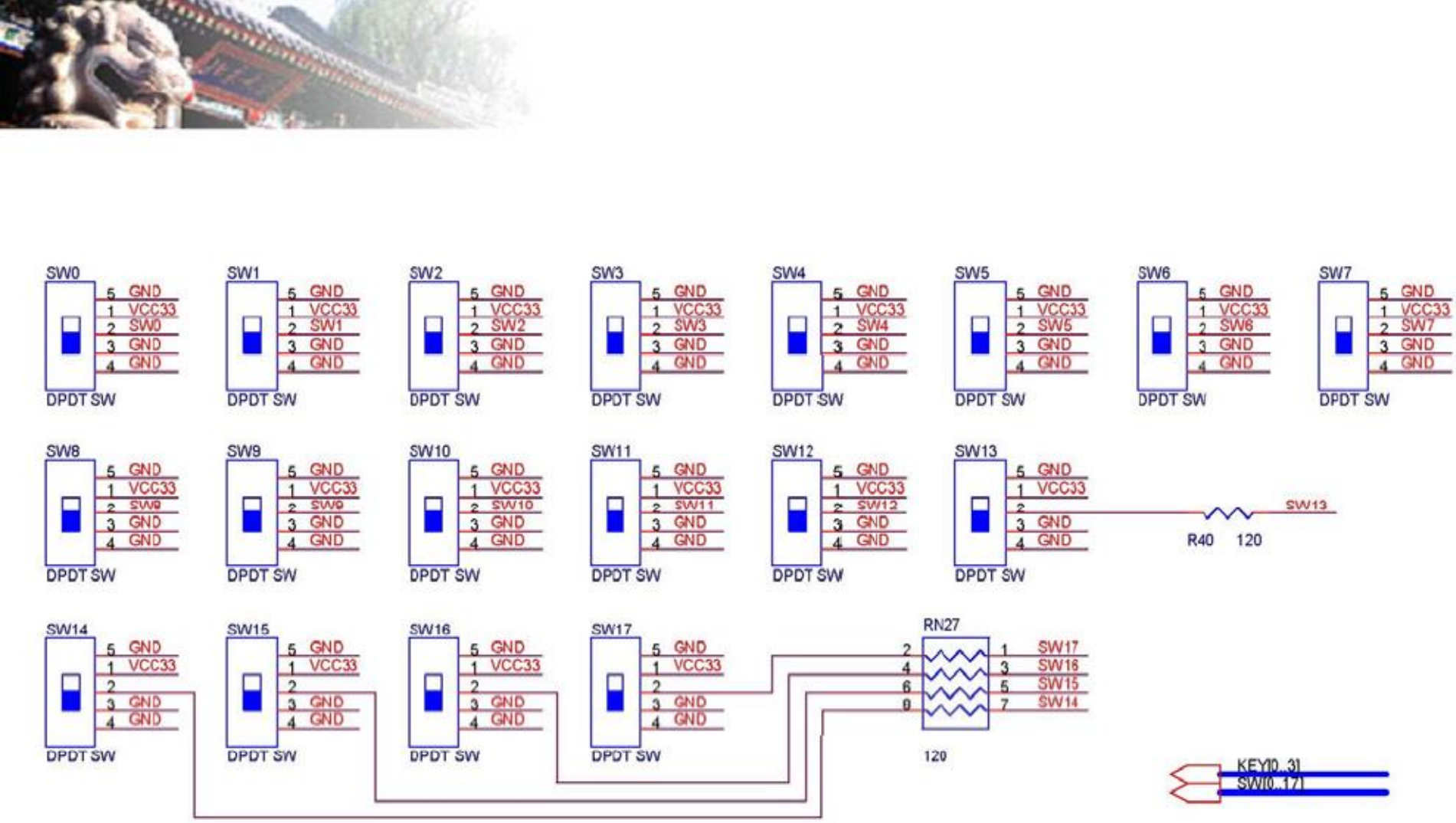
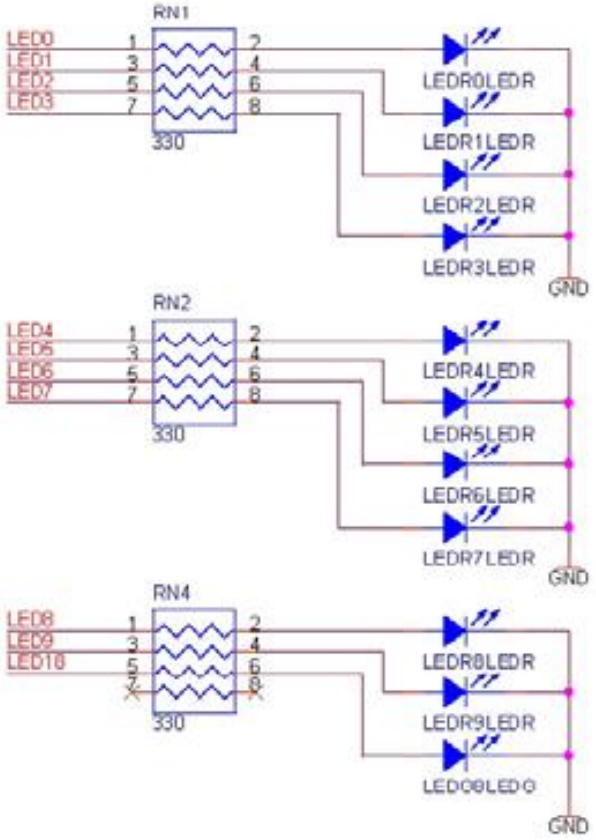
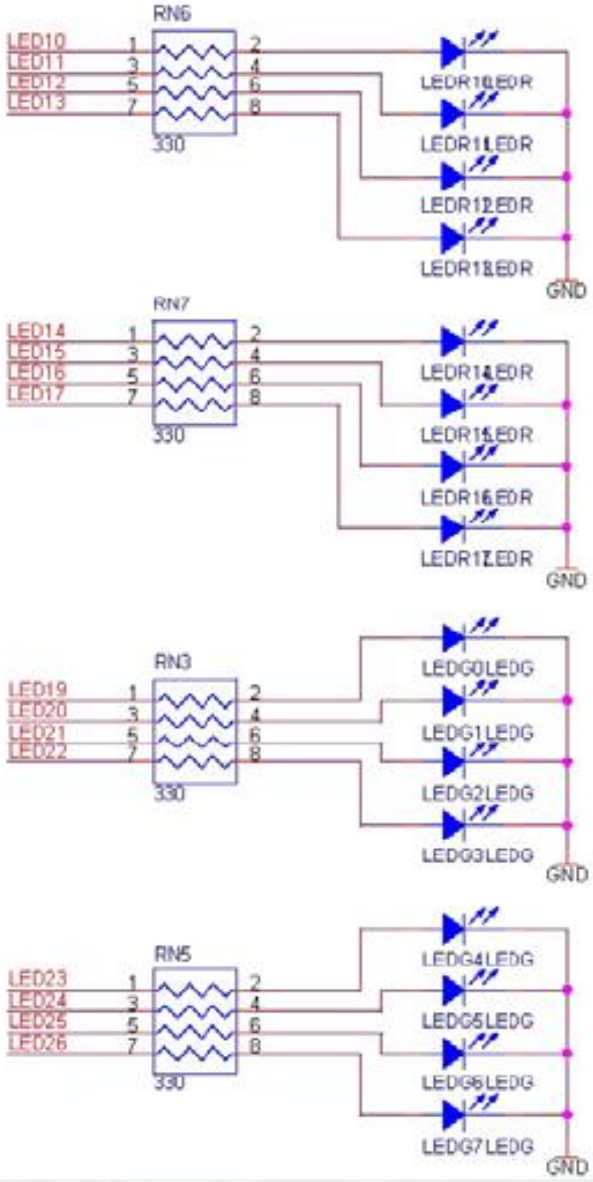

USB Blaster Port
USB Device Port
USB Host Port
Mic in
Line in
Line Out
Video In
VGA Video Port
Ethernet 10/100M Port
RS-232 Port
9V DC Power Supply Connector
27-MHz Oscillator
24-bit Audio Codec
Power ON/OFF Switch
USB Host/Slave Controller
TV Decoder (NTSC/PAL)
Altera USB Blaster Controller Chipset
Altera EPCS16 Configuration Device
RUN/PROG Switch for JTAG/AS Modes
16x2 LCD Module
7-Segment Displays
18 Red LEDs
18 Toggle Switches
PS/2 Keyboard/Mouse Port
VGA 10-bit DAC
Ethernet 10/100M Controller
Expansion Header 2 (JP2)
Expansion Header 1 (JP1)
Altera Cyclone II FPGA
SD Card Slot
8 Green LEDs
IrDA Transceiver
SMA External Clock
4 Debounced Pushbutton Switches
50-MHz Oscillator
8-MB SDRAM
512-KB SRAM
4-MB Flash Memory
DE2
ALTERA


SW0
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
SW10
SW11
SW12
SW13
SW14
SW15
SW16
SW17
5 GND
1 VCC33
2 SW0
2 SW1
2 SW2
2 SW3
2 SW4
2 SW5
2 SW6
2 SW7
2 SW8
2 SW9
2 SW10
2 SW11
2 SW12
2
3 GND
4 GND
DPDT SW
R40 120
RN27
120
KEY[0..3]
SW[0..17]


RN1
LED0
LED1
LED2
LED3
330
LEDR0LEDR
LEDR1LEDR
LEDR2LEDR
LEDR3LEDR
GND
RN2
LED4
LED5
LED6
LED7
330
LEDR4LEDR
LEDR5LEDR
LEDR6LEDR
LEDR7LEDR
GND
RN4
LED8
LED9
LED10
330
LEDR8LEDR
LEDR9LEDR
LED09LED9
GND


RN6
LED10
LED11
LED12
LED13
330
GND
RN7
LED14
LED15
LED16
LED17
330
GND
RN3
LED19
LED20
LED21
LED22
330
LEDG0LEDG
LEDG1LEDG
LEDG2LEDG
LEDG3LEDG
GND
RN5
LED23
LED24
LED25
LED26
330
LEDG4LEDG
LEDG5LEDG
LEDG6LEDG
LEDG7LEDG
GND

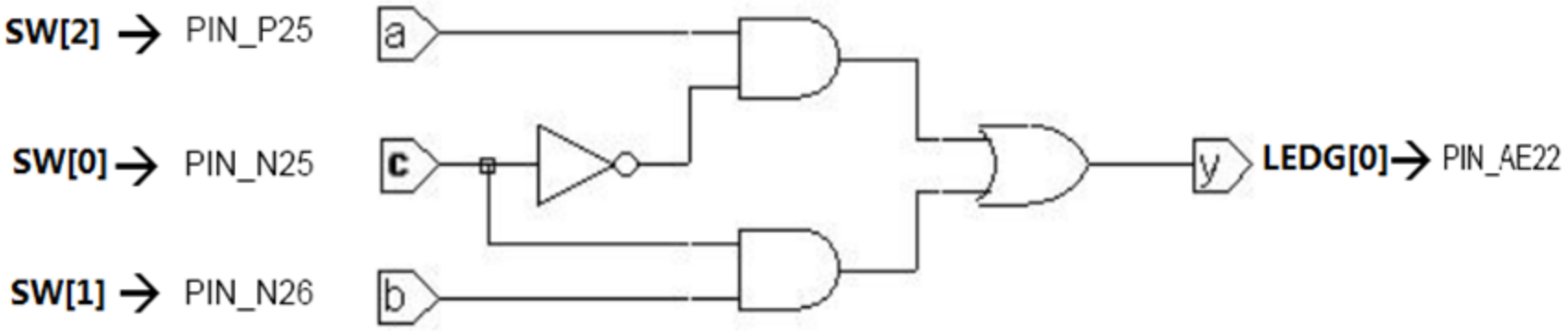
Signal Name	FPGA Pin No.	Description
SW[0]	PIN_N25	Toggle Switch[0]
SW[1]	PIN_N26	Toggle Switch[1]
SW[2]	PIN_P25	Toggle Switch[2]
SW[3]	PIN_AE14	Toggle Switch[3]
SW[4]	PIN_AF14	Toggle Switch[4]
SW[5]	PIN_AD13	Toggle Switch[5]
SW[6]	PIN_AC13	Toggle Switch[6]
SW[7]	PIN_C13	Toggle Switch[7]
SW[8]	PIN_B13	Toggle Switch[8]
SW[9]	PIN_A13	Toggle Switch[9]
SW[10]	PIN_N1	Toggle Switch[10]
SW[11]	PIN_P1	Toggle Switch[11]
SW[12]	PIN_P2	Toggle Switch[12]
SW[13]	PIN_T7	Toggle Switch[13]
SW[14]	PIN_U3	Toggle Switch[14]
SW[15]	PIN_U4	Toggle Switch[15]
SW[16]	PIN_V1	Toggle Switch[16]
SW[17]	PIN_V2	Toggle Switch[17]

Signal Name	FPGA Pin No.	Description
LEDR[0]	PIN_AE23	LED Red[0]
LEDR[1]	PIN_AF23	LED Red[1]
LEDR[2]	PIN_AB21	LED Red[2]
LEDR[3]	PIN_AC22	LED Red[3]
LEDR[4]	PIN_AD22	LED Red[4]
LEDR[5]	PIN_AD23	LED Red[5]
LEDR[6]	PIN_AD21	LED Red[6]
LEDR[7]	PIN_AC21	LED Red[7]
LEDR[8]	PIN_AA14	LED Red[8]
LEDR[9]	PIN_Y13	LED Red[9]
LEDR[10]	PIN_AA13	LED Red[10]
LEDR[15]	PIN_AE13	LED Red[15]
LEDR[16]	PIN_AE12	LED Red[16]
LEDR[17]	PIN_AD12	LED Red[17]
LEDG[0]	PIN_AE22	LED Green[0]
LEDG[1]	PIN_AF22	LED Green[1]
LEDG[2]	PIN_W19	LED Green[2]
LEDG[3]	PIN_V18	LED Green[3]
LEDG[4]	PIN_U18	LED Green[4]
LEDG[5]	PIN_U17	LED Green[5]
LEDG[6]	PIN_AA20	LED Green[6]
LEDG[7]	PIN_Y18	LED Green[7]
LEDG[8]	PIN_Y12	LED Green[8]

2选1数据选择器 管脚分配

Assignments→Assignment Editor 

Category : Pin



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下载

- 下载电缆一端连接PC机的并口，另一端连接实验板JTAG口 。
- 连接电源线，打开电源。
- Tools →Programmer  下载SOF文件。
- 验证设计。

知识点小结

- 要求掌握 QuartusII 设计流程
- 学会原理图输入
- 学会HDL输入
- 学会电路仿真，下载，原型测试