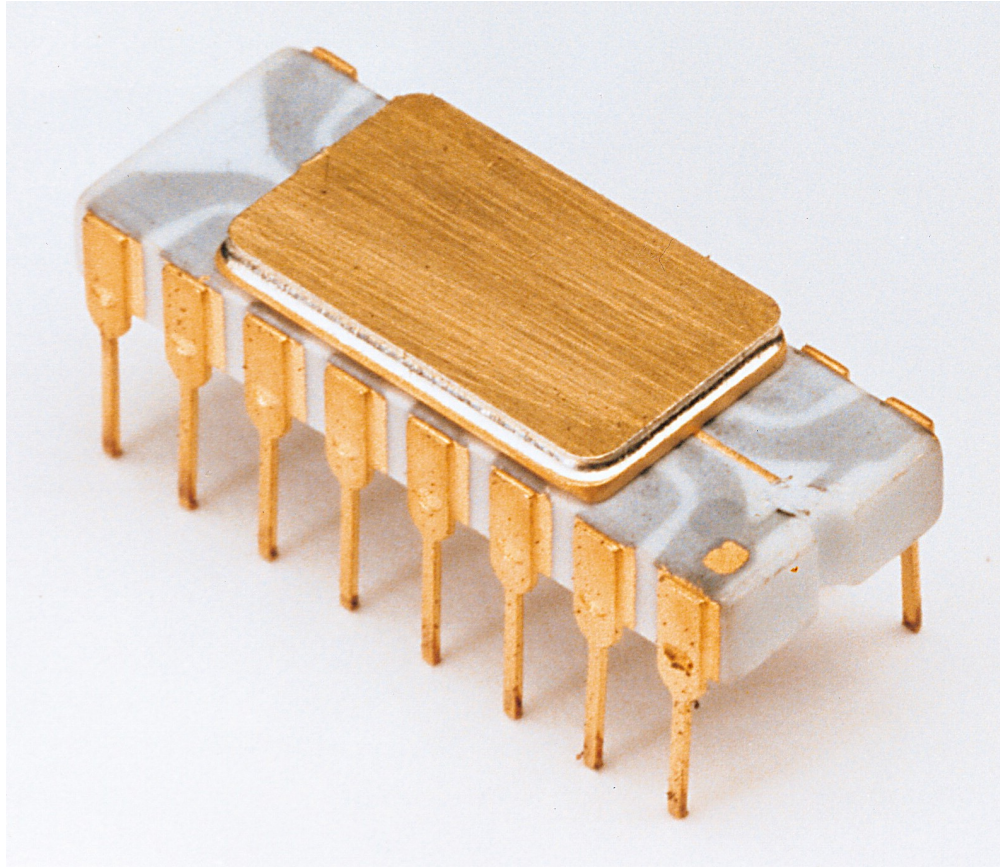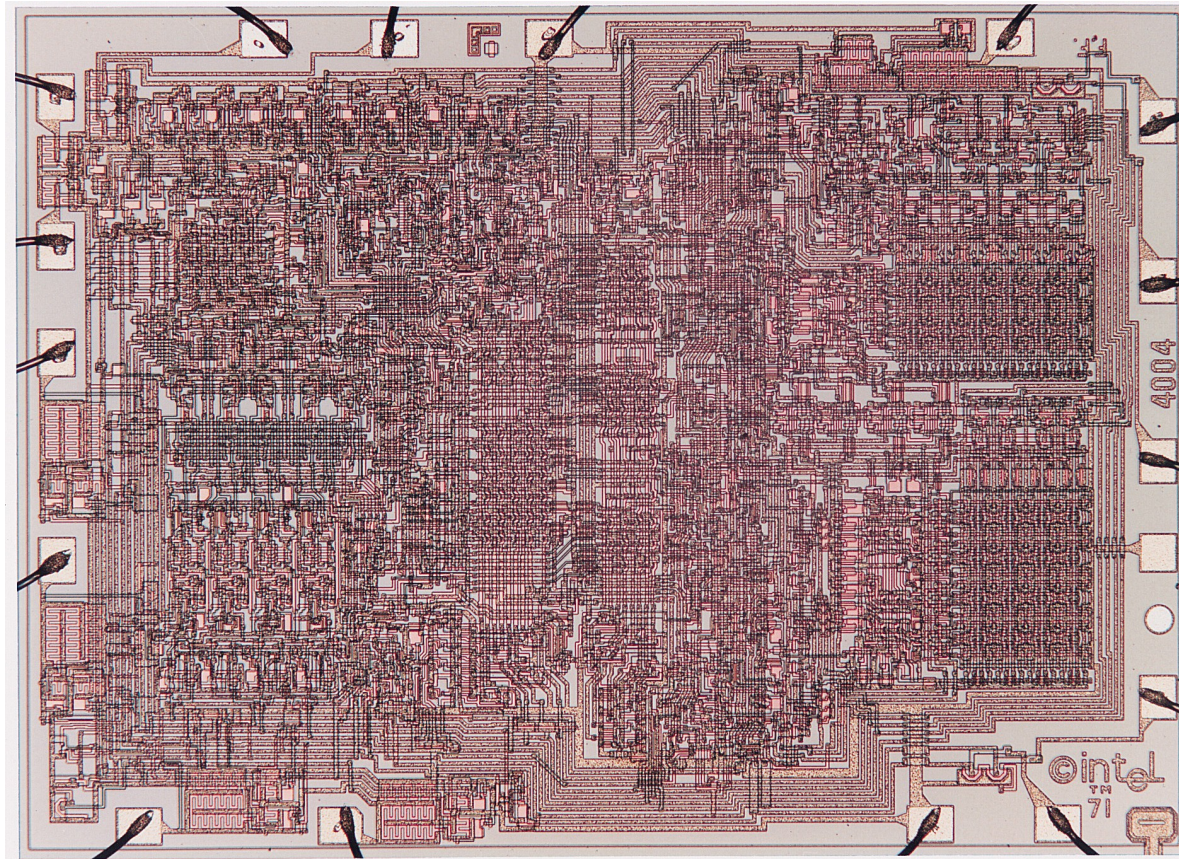# Microprocessors

Intel 4004 (1971)

Microprocessors
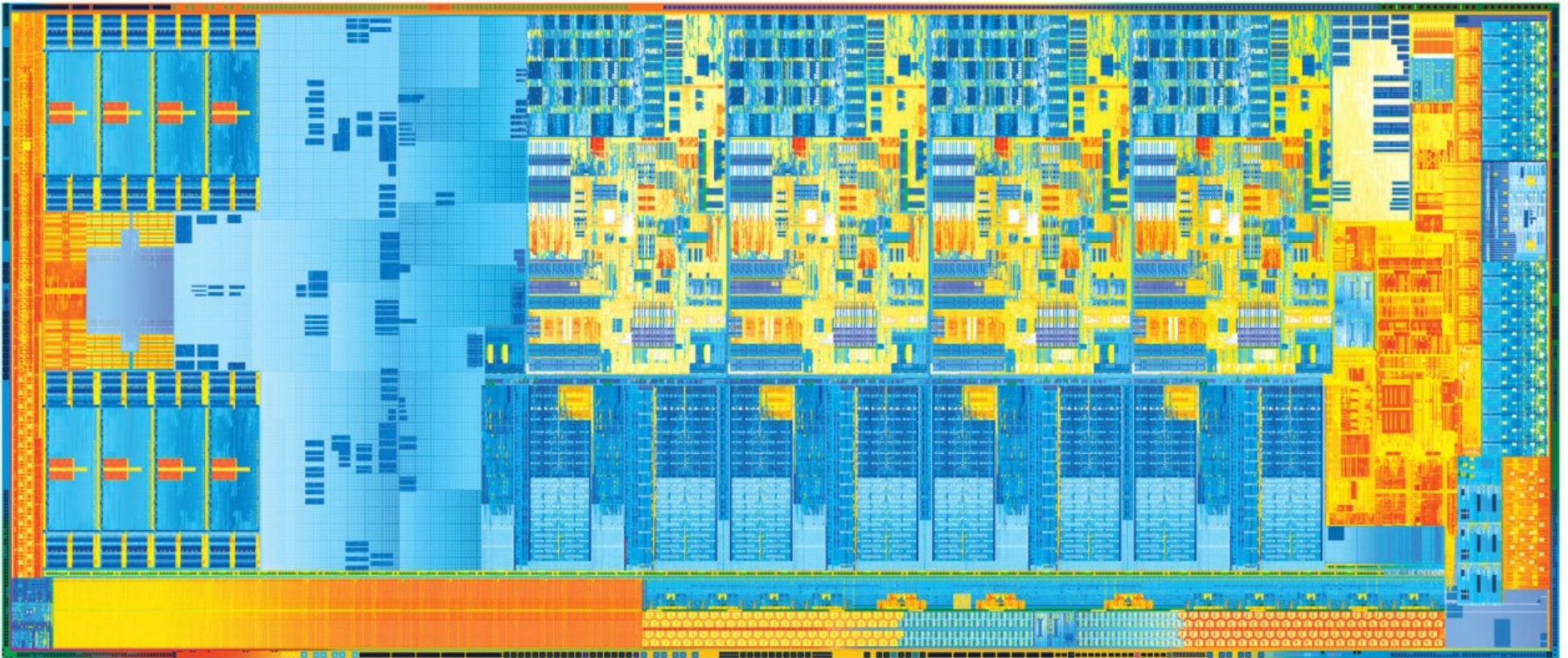

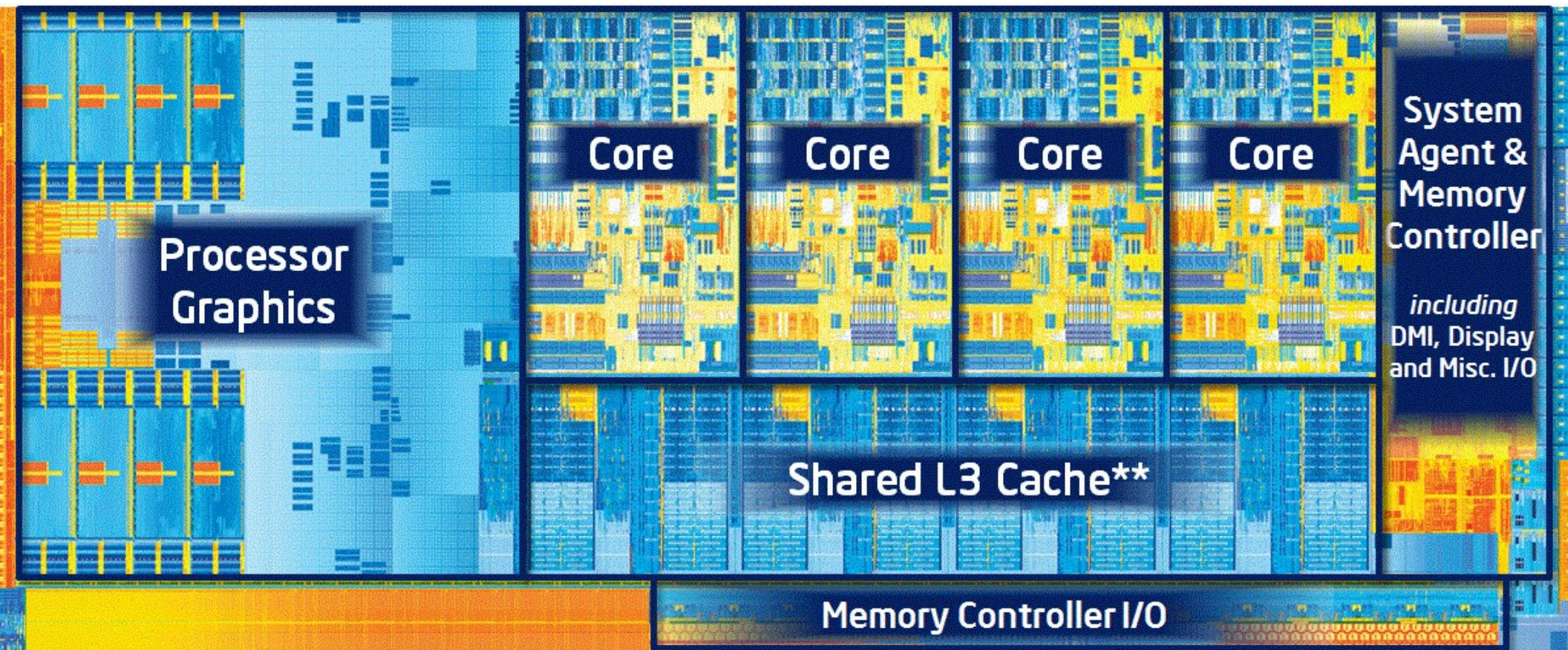2,300 Transitors @ 740kHz

Microprocessors

Intel i7 2012

Microprocessors

1.6 Billion Transistors @ 3.8GHz

Microprocessors

Microprocessors

- What's in the core?
  - Registers
    - Similar to memory, fast access
    - Can be used to hold values or manage processor execution
  - Each register = a collection of flip flops (1 bit store)
    - Usually in multiples of 8 e.g. 8/16/32/64 bit

Microprocessors
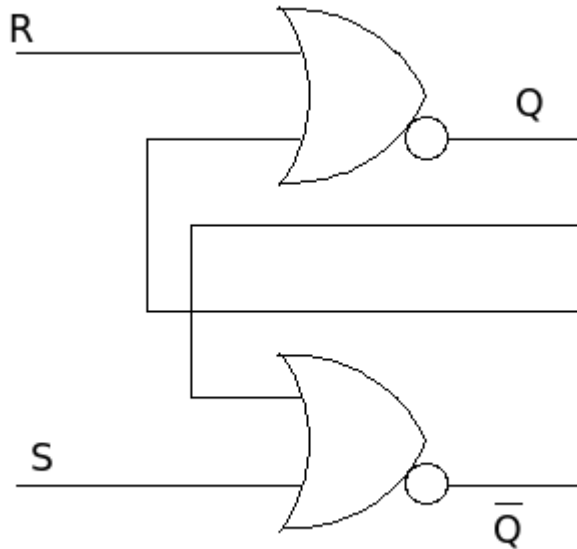
A flip-flop is a 1 bit latch (store)

Truth table

State	R	S	Q
1	0	1	1
2	0	0	1
3	1	0	0
4	0	0	0
5	1	1	?

Microprocessors

- ## What's in the core?
  - – Arithmetic Unit
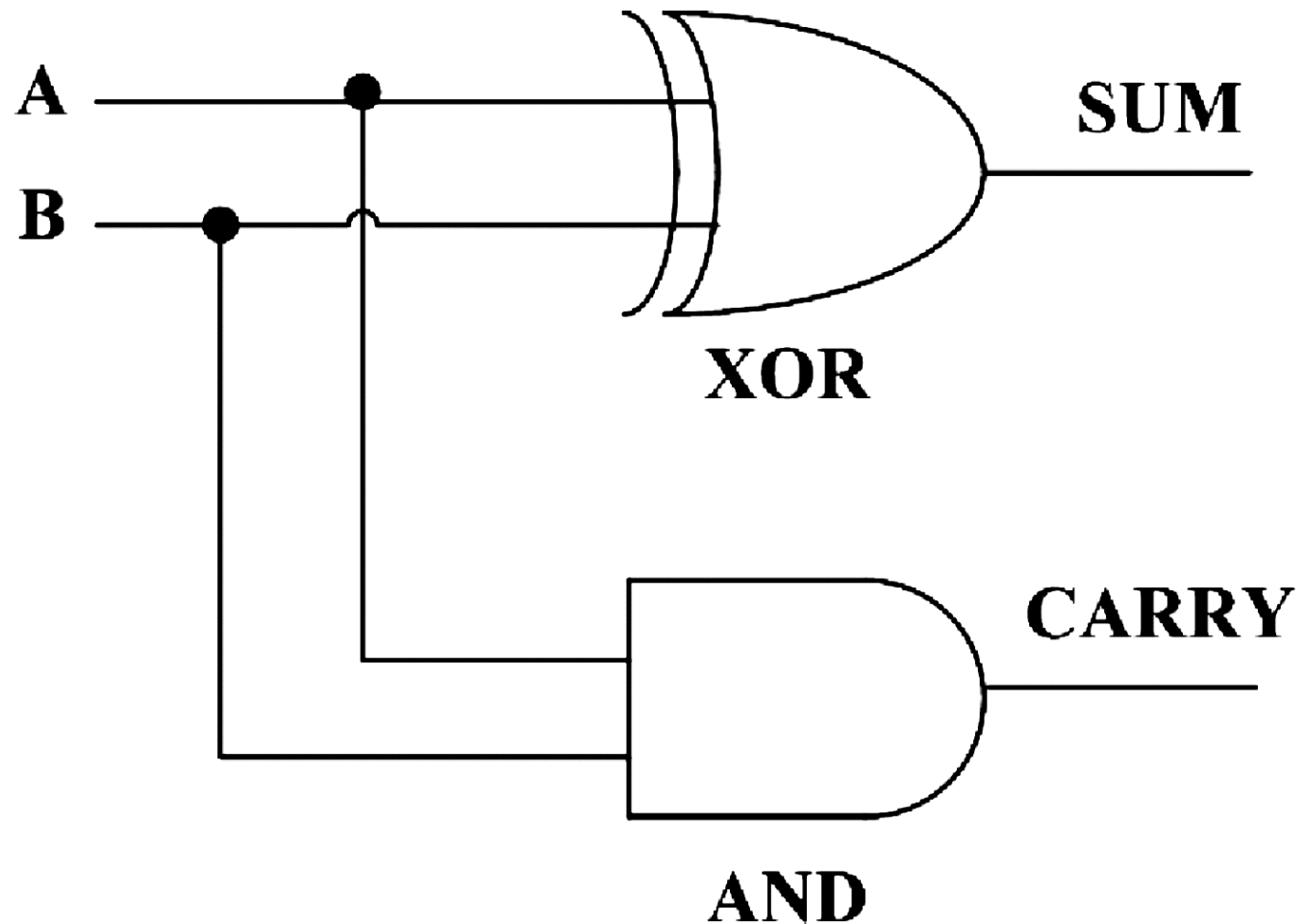
Microprocessors

- ## What's in the core?

  - Instruction decoder

Numeric instruction from memory (machine code) → Instruction Decoder → Process control and status signals
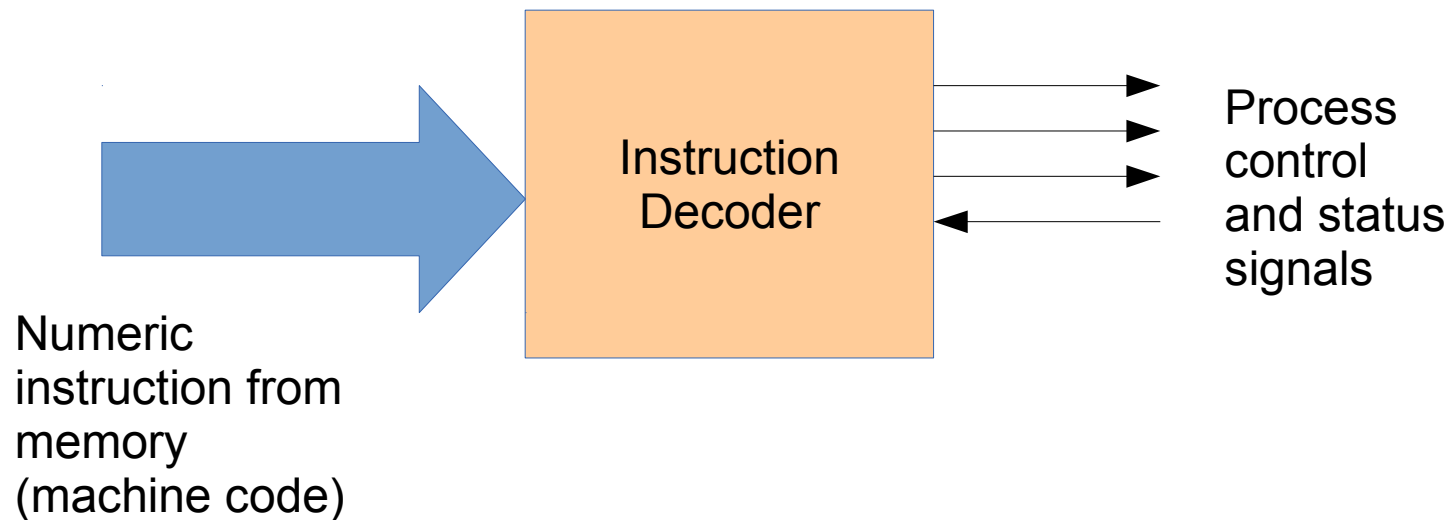
Microprocessors

- What processor will we be using?

  - NXP LPC1114
  - Contains a ARM Cortex M0 core

ARM Cortex microcontrollers

- The ARM family of microcontrollers

  - First ARM processor prototype 26 April 1985

  - Began manufacture (ARM2) in 1986

  - Contained 30,000 transistors (80286 had 134,000 transistors and was slower, consumed more power)

  - 1990 Arm holdings set up to license ARM cores to chip producers.

ARM Cortex microcontrollers

- The ARM family of microcontrollers
  - 2004 Cortex family of processors introduced
  - 2012 20 billion Arm cores shipped to date

ARM Cortex microcontrollers

- The ARM family of microcontrollers

  - 32 bit processor

  - Memory mapped I/O

  - RISC

  - Harvard Architecture

  - Instructions sets:

    - ARM

    - Thumb (Version 1 and 2)

    - Java byte code

ARM Cortex microcontrollers

- The ARM family of microcontrollers
  - Cortex M series
    - Targeted at microcontroller industry
    - Thumb instruction set only (V2)
  - Cortex A series
    - Application profile
    - Targeted at tablet, phone, general purpose computing
  - Cortex R series
    - Real-time profile
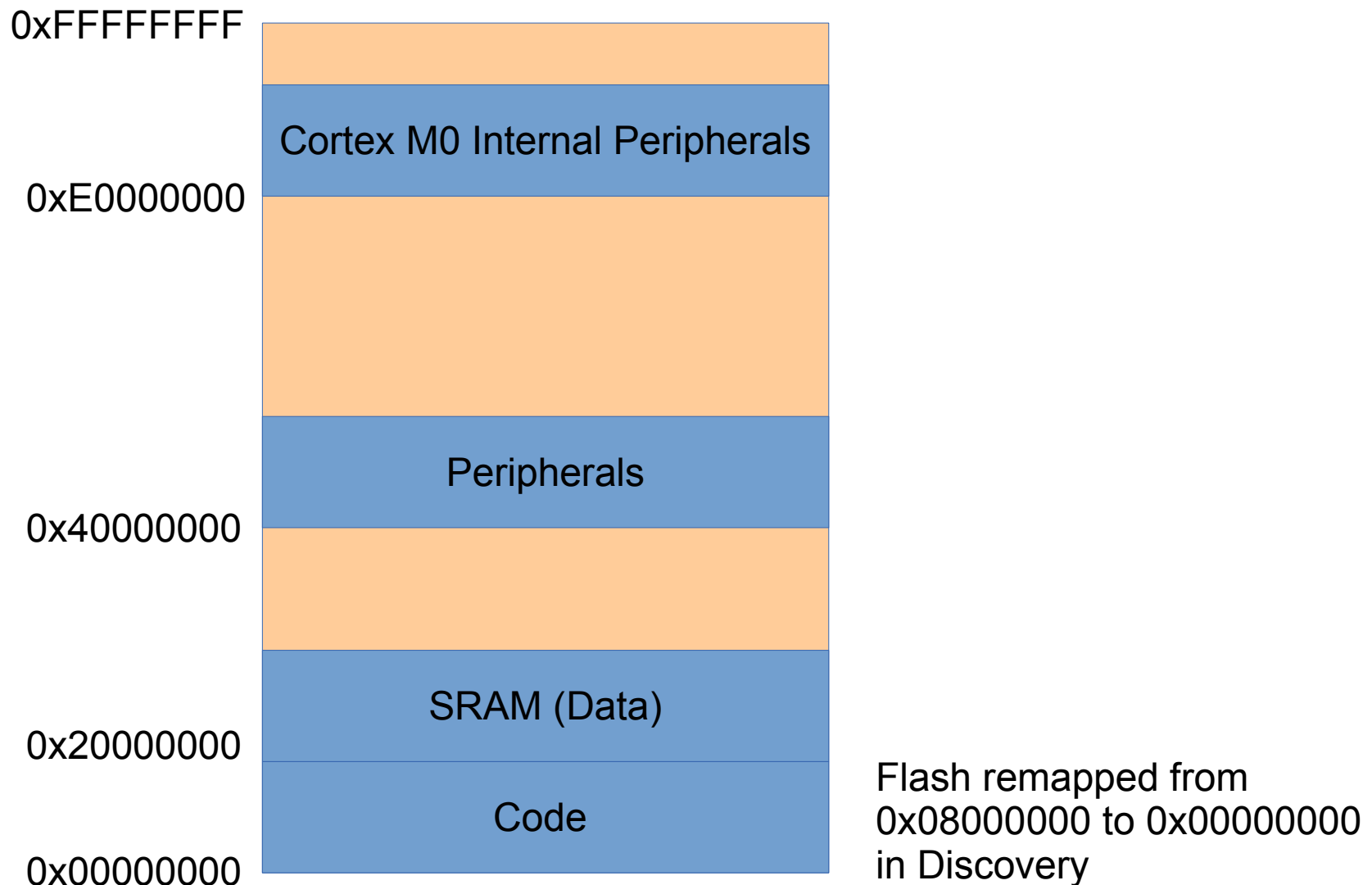
ARM Cortex microcontrollers

- The ARM family of microcontrollers

Cortex M family

- Executes Thumb2 instructions

- Mostly 16 bit for high code density

- Different operating modes

    - Normal/User/Thread (Thread Mode)

    - Interrupt Handler/OS (Handler Mode)

    - Certain registers can only be accessed in Handler Mode (memory protection of sorts)

ARM Cortex microcontrollers

- Memory map

0xFFFFFFFF

Cortex M0 Internal Peripherals

0xE0000000

Peripherals

0x40000000

SRAM (Data)

0x20000000

Code

0x00000000

Flash remapped from
0x08000000 to 0x00000000
in Discovery

ARM Cortex microcontrollers

- Internal peripheral buses
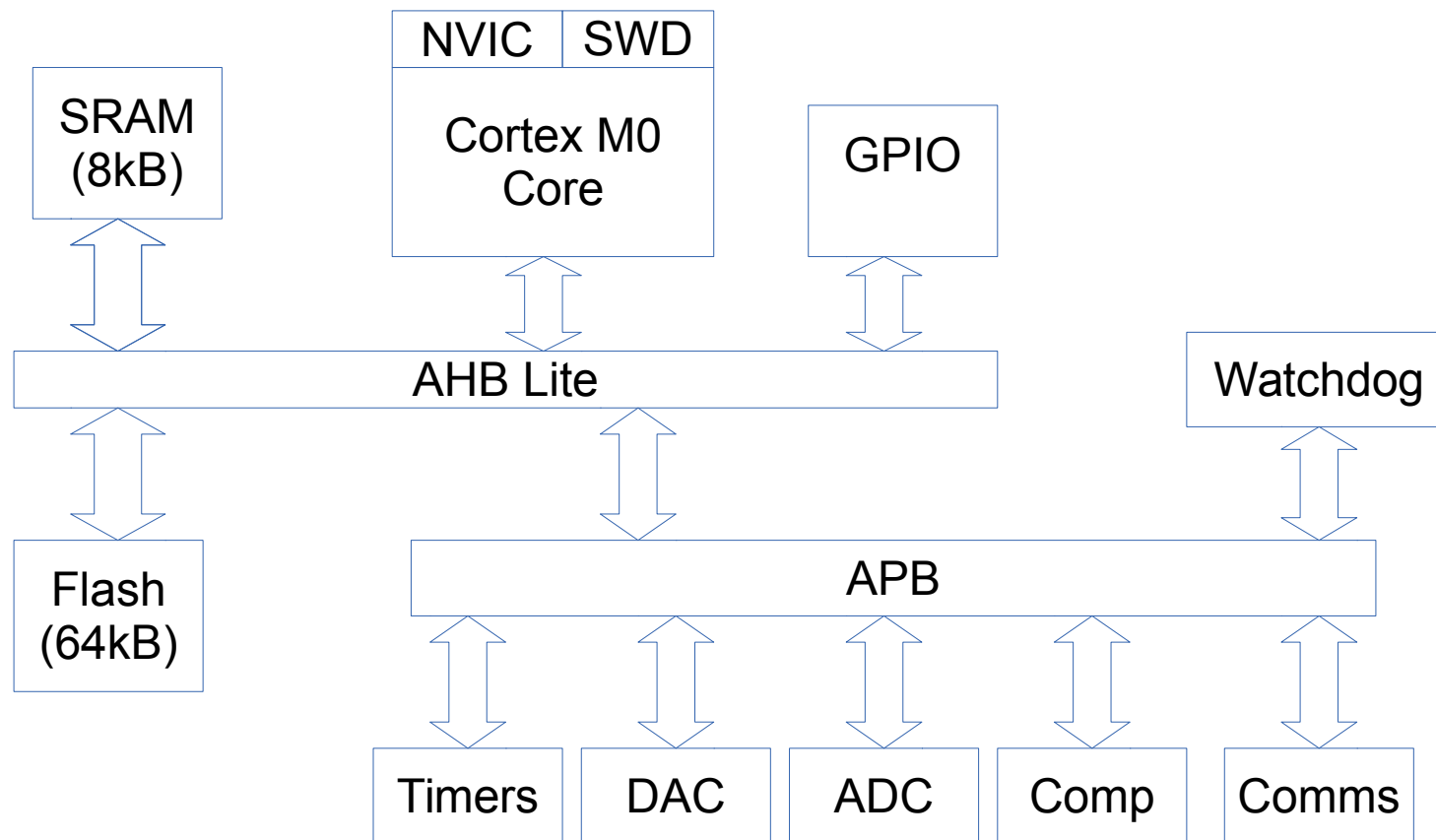
ARM Cortex microcontrollers

Cortex M0 Core
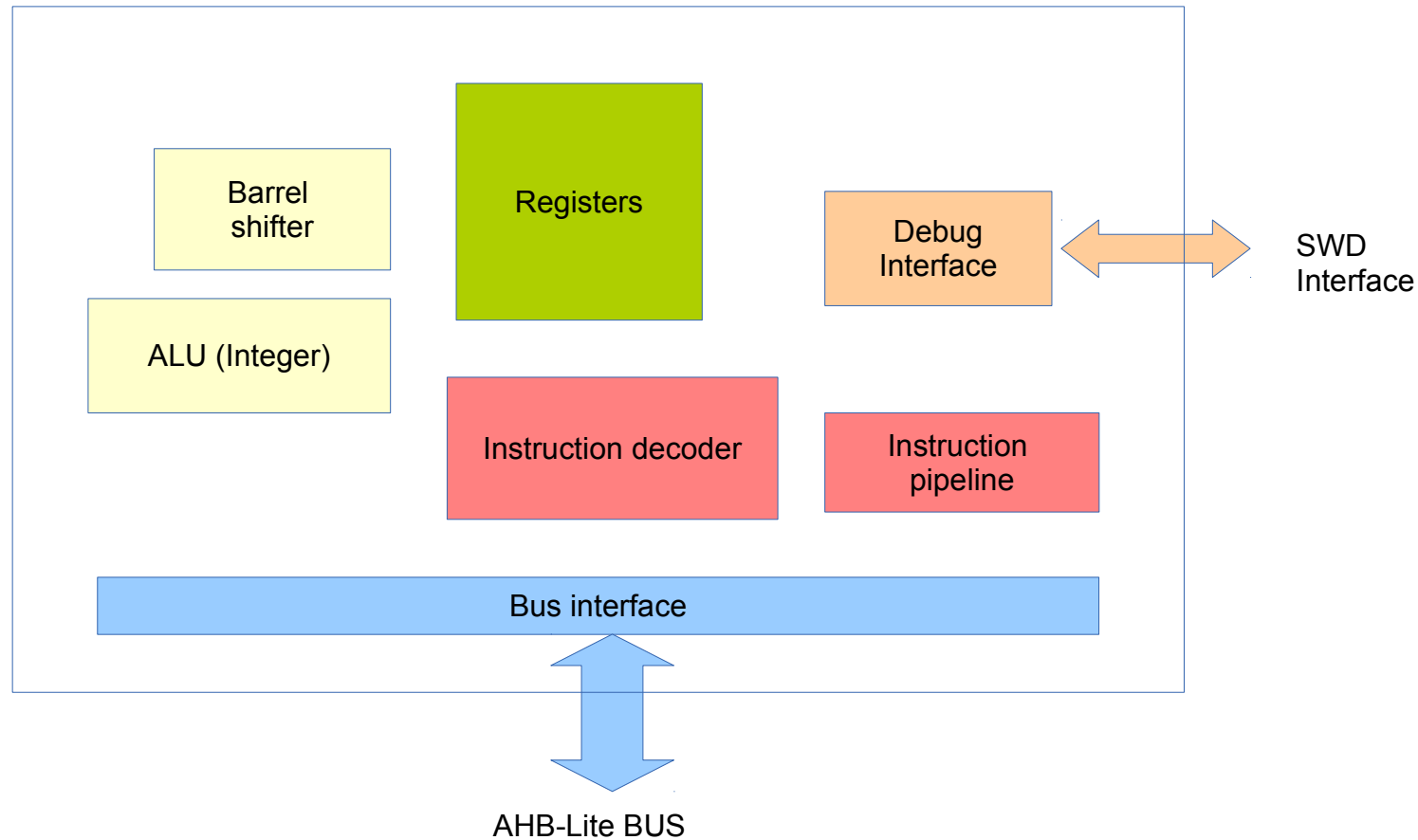
ARM Cortex microcontrollers

Cortex M0 Registers

R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
Stack Pointer (R13)
Link Register (R14)
Program Counter (R15)

Program Status Register (PSR)
Priority Mask Register (PRIMASK)
Control

Process Stack Pointer (PSP) or Main Stack Pointer (MSP)

LPC1110/11/12/13/14

SWD

XTALIN
XTALOUT[3]
RESET

CLOCK GENERATION, POWER CONTROL, SYSTEM FUNCTIONS

IRC

POR

CLKOUT

clocks and controls

TEST/DEBUG INTERFACE

ARM CORTEX-M0

system bus

FLASH 4/8/16/24/32 kB

SRAM 1/2/4/8 kB

ROM

slave   slave   slave

GPIO ports PIO0/1/2/3

HIGH-SPEED GPIO

slave

AHB-LITE BUS

slave

AHB TO APB BRIDGE

RXD
TXD
DTR, DSR, CTS[5], DCD, RI, RTS[5]

UART

10-bit ADC

AD[7:0][4]

SPI0

{ SCK0, SSEL0
MISO0, MOSI

CT32B0_MAT[3:0][3]
CT32B0_CAP0[3]

32-bit COUNTER/TIMER 0

SPI1[1]

{ SCK1, SSEL1
MISO1, MOSI

CT32B1_MAT[3:0][3]
CT32B1_CAP0[3]

32-bit COUNTER/TIMER 1

I²C-BUS[2]

SCL
SDA

CT16B0_MAT[2:0][3]
CT16B0_CAP0[3]

16-bit COUNTER/TIMER 0

CT16B1_MAT[1:0][3]
CT16B1_CAP0[3]

16-bit COUNTER/TIMER 1

WDT

IOCONFIG

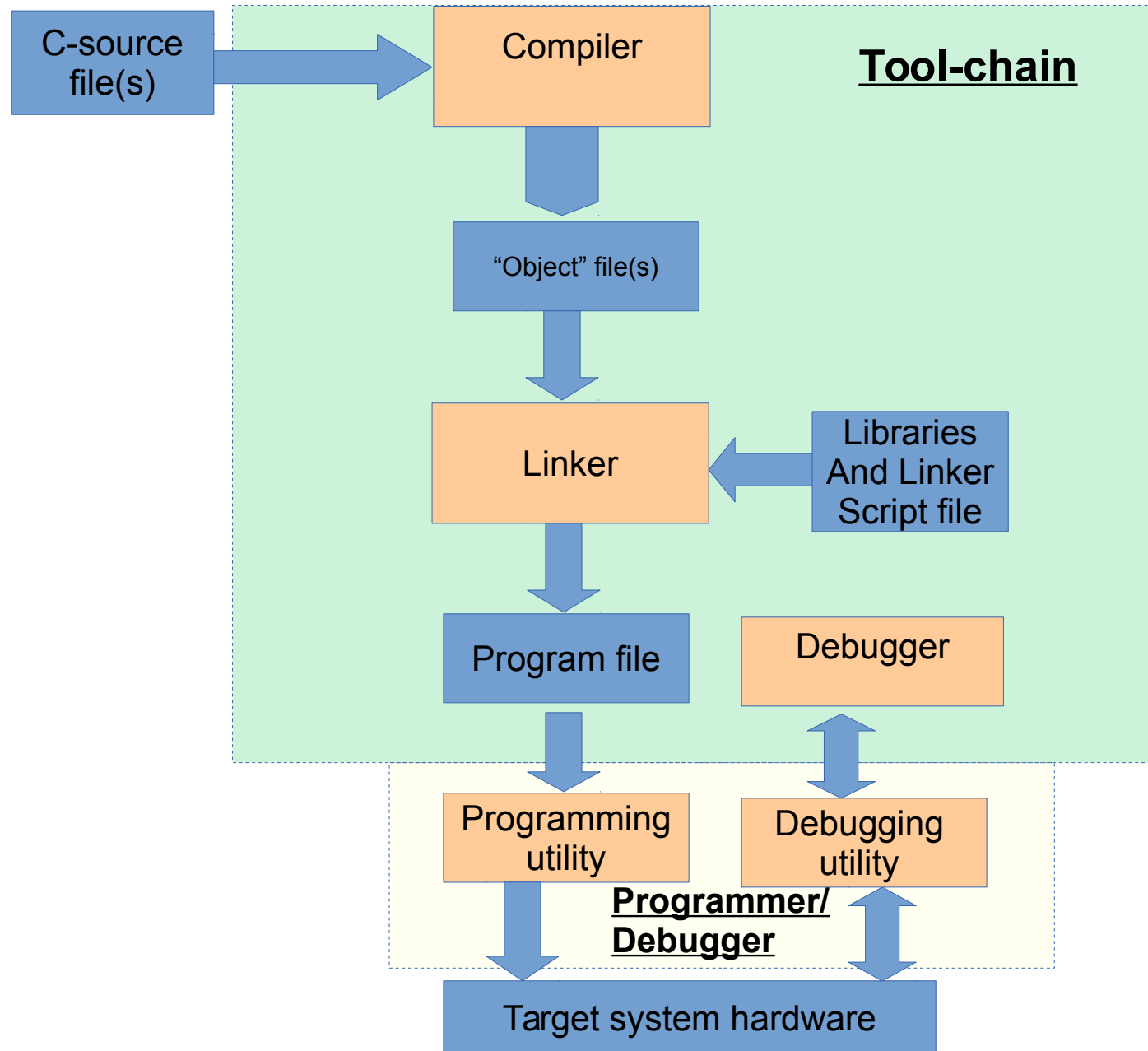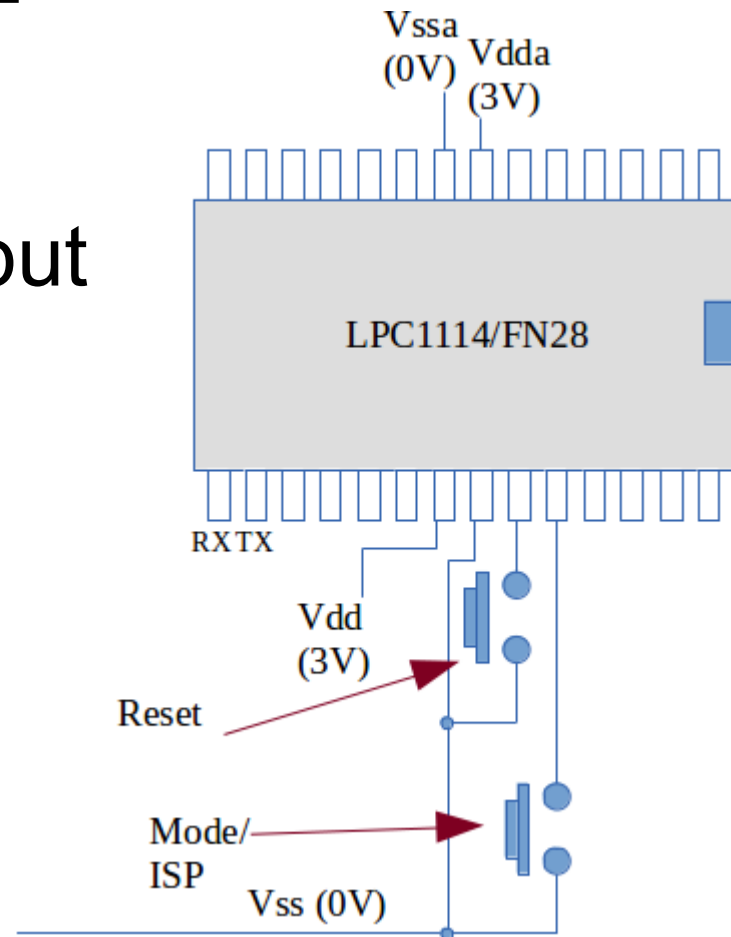SYSTEM CONTROL

PMU

Programming

ARM Cortex microcontrollers

- In System Programming (ISP)

- Requires only a UART (€6 approx)

- Allows programming but not debugging

Vssa (0V) Vdda (3V)

LPC1114/FN28

USB/Serial converter

3V
0V
RX
TX

RX TX

Vdd (3V)

Reset

Mode/ISP

Vss (0V)

How is this module graded?

- Lab quizzes (25%)

  – You are required to attend lab

- Two, open book, in-class tests (25%)

  – No repeat possible so don't miss

- Final exam (50%)

  – Exam includes topics covered in lab