Dongyang Wu

wudongya@usc.edu | www.linkedin.com/in/william-wu-dongyang/

EDUCATION

- **University of Southern California (USC)** Los Angeles, CA
  Master of Electrical Engineering; GPA: 4.0/4.0 08/2022-05/2024
    - C
    - o
    - u
    - r
    - s
    - e
    - :
    -
    - D
    - i
    - g
    - i
    - t
    - a
    - l
    -
    - S
    - y
    - s
    - t
    - e
    - m
    -
    - D
    - e
    - s
    - i
    - g
    - n
    -
    - (
    - E
    - E
    - 5
    - 6
    - 0
    -)
    - ,
    -
    - C
    - o

- m
- p
- u
- t
- e
- r
-
- S
- y
- s
- t
- e
- m
- s
-
- A
- r
- c
- h
- i
- t
- e
- c
- t
- u
- r
- e
-
- (
- E
- E
- 5
- 5
- 7
-)
- ,
-
- M
- O
- S
-
- V
- L
- S
- I
-

- C
- i
- r
- c
- u
- i
- t
-
- D
- e
- s
- i
- g
- n
-
- (
- E
- E
- 4
- 7
- 7
-)
- ,
-
- C
- o
- m
- p
- u
- t
- e
- r
-
- s
- y
- s
- t
- e
- m
- s
-
- O
- r
- g
- a
- n

- i
- z
- a
- t
- i
- o
- n
-
- (
- E
- E
- 4
- 5
- 7
-)
- ,
-
- I
- n
- t
- r
- o
- d
- u
- c
- t
- i
- o
- n
-
- t
- o
-
- C
- o
- m
- p
- u
- t
- e
- r
-
- N
- e
- t
- w

- o
- r
- k
- s
-
- (
- E
- E
- 4
- 5
- 0
-)

- **The Chinese University of Hong Kong, Shenzhen (CUHKSZ)** Shenzhen, China
  Bachelor of Computer Science and Engineering; GPA: 3.4/4.0 09/2018-06/2022

SKILLS

Programming Languages: Python, C/C++, Verilog, VHDL, SQL, MIPS
EDA Tools: Virtuoso, QuestaSim, Xilinx Vivado
Protocols: TCP/IP, USB, SPI, AXI, PCIe, MOESI
Tools: UNIX, Linux, Git, Makefile, CUDA

PROJECTS

- **Tomasulo Out-of-Order CPU** 06/2023-08/2023
  - Designed CPU with Out-of-Order Execution and In-order Commitment.
  - Implemented Branch Prediction Buffer(BPB) and Return Stack Address(RAS) for speculative execution beyond branches.
  - Implemented BRAM-based Copy Free Check-pointing(CFC) with RRAT for recovery from path misprediction.
  - Implemented Store Buffer(SB), Store Address Buffer(SAB), Reorder Buffer(ROB), 2-stage Dispatch Unit, Free Register List(FRL) and Issue Unit(IU).
- **PCIe Physical Layer Design** 06/2023-08/2023
  - Designed physical layer components for PCIe 2-lane system.
  - Implemented Elastic Buffer with Primed Method to achieve Clock Domain Crossing by adjusting Skip Ordered Set.
  - Implemented Deskew Buffer to eliminate skew between lanes.
- **VLSI CMOS Design** 01/2023-05/2023
  - Designed basic combinational and sequential circuits using Cadence Virtuoso.
  - Accounted for 20-bit mux unit, 20-bit Han-Carlson adder unit 20-bit register Schematic and Layout design work
  - Integrated components using wave pipeline with the area of 5.96 mm^2 in 2.0 Ghz (cycle time=0.5 ns).
  - Validated the correctness of all aforementioned components with vector file and cleared DRC and LVS errors.