Dongyang Wu

wudongya@usc.edu | www.linkedin.com/in/william-wu-dongyang/

EDUCATION

- **University of Southern California (USC)** Los Angeles, CA
  Master of Electrical Engineering; GPA: 4.0/4.0 08/2022-05/2024
  - Courses: Digital System Design (EE560), Computer Systems Architecture (EE557), MOS VLSI Circuit Design (EE477), Computer Systems Organization (EE457), Introduction to Computer Networks (EE450)
  - Added to the MS Honors Program
- **The Chinese University of Hong Kong, Shenzhen (CUHKSZ)** Shenzhen, China
  Bachelor of Computer Science and Engineering; GPA: 3.4/4.0 09/2018-06/2022
  - Courses: Computer Architecture, Parallel Computing, Operating Systems, Compiler Construction, Microprocessors and Computer Systems, Design and Analysis of Algorithms

SKILLS

Programming Languages: Python, C/C++, Verilog, VHDL, SQL, MIPS
EDA Tools: Virtuoso, QuestaSim, Xilinx Vivado
Protocols: TCP/IP, USB, SPI, AXI, PCIe, MOESI
Tools: UNIX, Linux, Git, Makefile, CUDA, MPI, pthreads

PROJECTS

- **Tomasulo Out-of-Order CPU** 06/2023-08/2023
  - Designed CPU with Out-of-Order Execution and In-order Commitment.
  - Implemented Branch Prediction Buffer(BPB) and Return Stack Address(RAS) for speculative execution beyond branches.
  - Implemented BRAM-based Copy Free Check-pointing(CFC) with RRAT for recovery from path misprediction.
  - Implemented Store Buffer(SB), Store Address Buffer(SAB), Reorder Buffer(ROB), 2-stage Dispatch Unit, Free Register List(FRL) and Issue Unit(IU).
- **PCIe Physical Layer Design** 06/2023-08/2023
  - Designed physical layer components for PCIe 2-lane system.
  - Implemented Elastic Buffer with Primed Method to achieve Clock Domain Crossing by adjusting Skip Ordered Set.
  - Implemented Deskew Buffer to eliminate skew between lanes.
- **VLSI CMOS Design** 01/2023-05/2023
  - Designed basic combinational and sequential circuits using Cadence Virtuoso.
  - Accounted for 20-bit mux unit, 20-bit Han-Carlson adder unit 20-bit register Schematic and Layout design work
  - Integrated components using wave pipeline with the area of 5.96 mm^2 in 2.0 GHz (cycle time=0.5 ns).
  - Validated the correctness of all aforementioned components with vector file and cleared DRC and LVS errors.
- **High-Level Simulation of Computer Architecture** 01/2023-05/2023
  - Designed different branch prediction algorithms and used Intel Pin for simulation and accuracy analysis.
  - Implemented gem5 for performance analysis for various benchmarks under different parameters.
- **Socket Project** 10/2023-12/2023
  - Designed TCP and UDP sockets by C for communication between different ports.
  - Used Makefile to compile all programs.