$\begin{array}{c} \textbf{Dongyang Wu} \\ \textbf{wudongya@usc.edu} \mid \textbf{www.linkedin.com/in/william-wu-dongyang/} \end{array}$

EDUCATION

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University of Southern California (USC) Master of Electrical Engineering; GPA: 4.0/4.0	Los Angeles, CA 08/2022-05/2024
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• The Chinese University of Hong Kong, Shenzhen (CUHKSZ) Bachelor of Computer Science and Engineering; GPA: 3.4/4.0

Shenzhen, China 09/2018-06/2022

SKILLS

Programming Languages: Python, C/C++, Verilog, VHDL, SQL, MIPS

EDA Tools: Virtuoso, QuestaSim, Xilinx Vivado **Protocols**: TCP/IP, USB, SPI, AXI, PCIe, MOESI

Tools: UNIX, Linux, Git, Makefile, CUDA

PROJECTS

• Tomasulo Out-of-Order CPU

06/2023-08/2023

- o Designed CPU with Out-of-Order Execution and In-order Commitment.
- $\circ\,$ Implemented Branch Prediction Buffer (BPB) and Return Stack Address (RAS) for speculative execution beyond branches.
- Implemented BRAM-based Copy Free Check-pointing (CFC) with RRAT for recovery from path misprediction.
- Implemented Store Buffer(SB), Store Address Buffer(SAB), Reorder Buffer(ROB), 2-stage Dispatch Unit, Free Register List(FRL) and Issue Unit(IU).

• PCIe Physical Layer Design

06/2023-08/2023

- Designed physical layer components for PCIe 2-lane system.
- Implemented Elastic Buffer with Primed Method to achieve Clock Domain Crossing by adjusting Skip Ordered Set.
- Implemented Deskew Buffer to eliminate skew between lanes.

• VLSI CMOS Design

01/2023-05/2023

- o Designed basic combinational and sequential circuits using Cadence Virtuoso.
- o Accounted for 20-bit mux unit, 20-bit Han-Carlson adder unit 20-bit register Schematic and Layout design work
- \circ Integrated components using wave pipeline with the area of 5.96 mm^2 in 2.0 Ghz (cycle time=0.5 ns).
- Validated the correctness of all aforementioned components with vector file and cleared DRC and LVS errors.