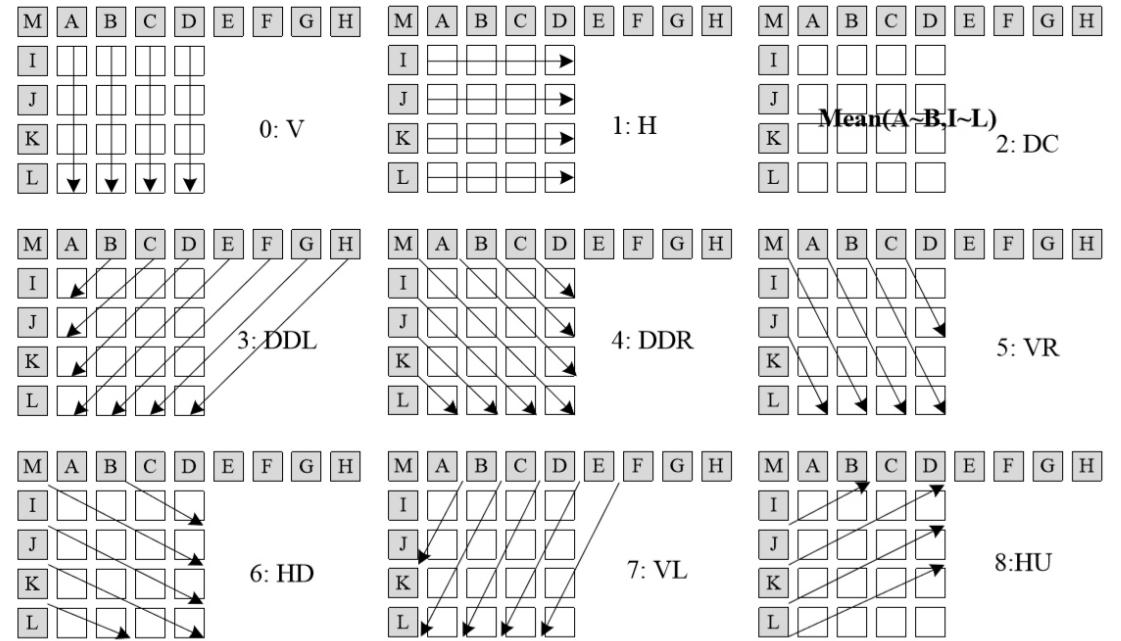


ABOUT THE PROJECT

Key words: H.264, video codec, intra prediction

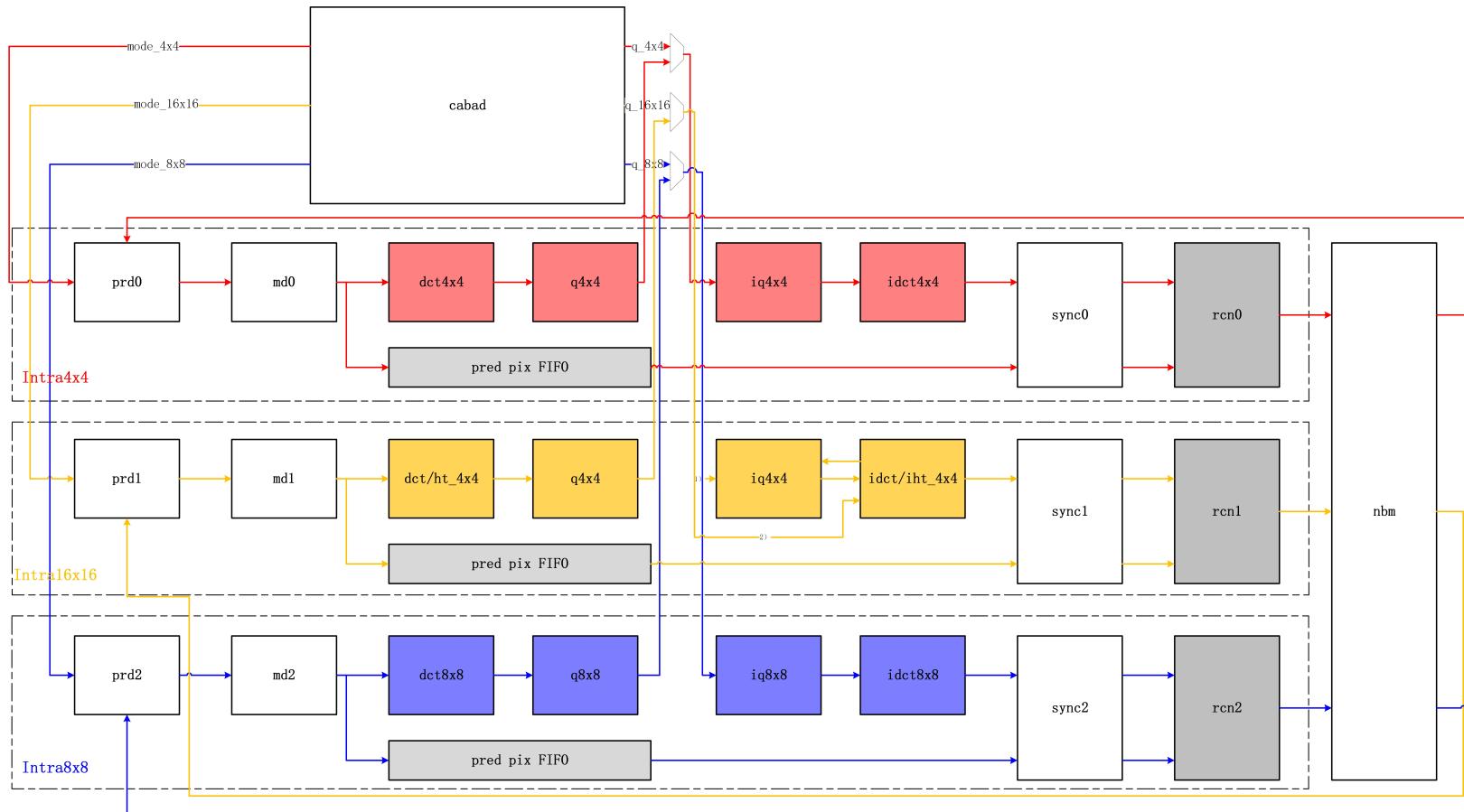
H.264 standard



- The project aims to design a commercial video codec chip. The chip is being taped out.

DETAILS-FRAMEWORK

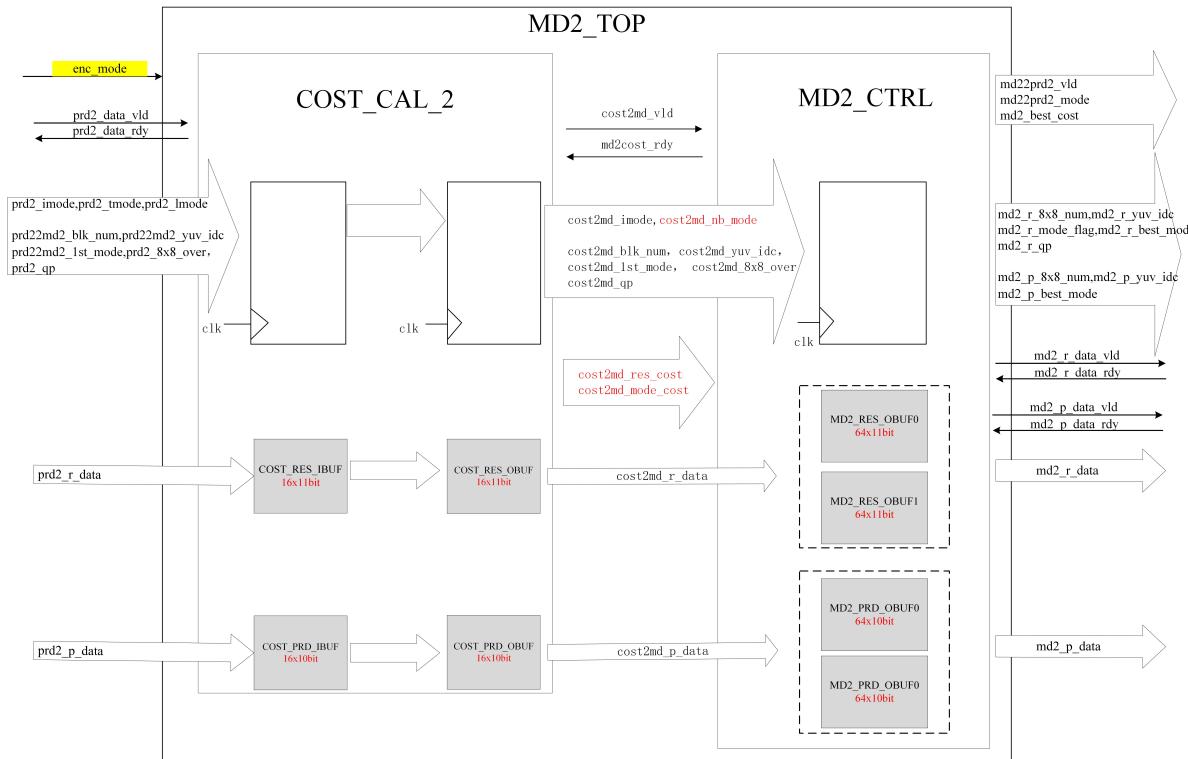
- A video codec chip that performs intra-frame prediction of the H.264 standard is designed. The chip is designed for a compression ratio of 30:1, and the maximum processing ability is 4K@60fps, YUV444, 10-bit color depth. The chip is designed to run at 400MHz, and has an area of 1672.94K gates(simulated by Design Compiler, TSMC 65nm, including on-chip memory).



Framework of the H.264 Decoder.

DETAILS-SUBMODULE

- Design core modules, including intra-frame prediction(PRD), mode decision(MD), and neighbour block maintenance(NBM).
- Design the hardware architecture with a predefined number of clock cycles and storege resources by using finite state machines, pipeline, Valid/Ready handshake mechanism, and ping-pong buffer, etc.
- The design is completed in Verilog HDL, and the functional verification is completed using NCVerilog based on the bus function model(BFM).



VLSI Architecture of Mode Decision(MD).

MD is used to choose the best prediction mode based on the distortion and rate.

DETAILS-BFM

- Build the BFM in SystemVerilog, providing a universal verification environment for the whole project. Complete the functional verification and DC synthesis of the whole design.
- The BFM has parameters that can be reconfigured randomly. It can also generate test vector and check DUT output automatically, providing simple and efficient functional verification.
- SystemVerilog-based software reference models for complex modules are implemented and integrated into the verification environment to perform hardware-software co-verification to improve the verification efficiency.

