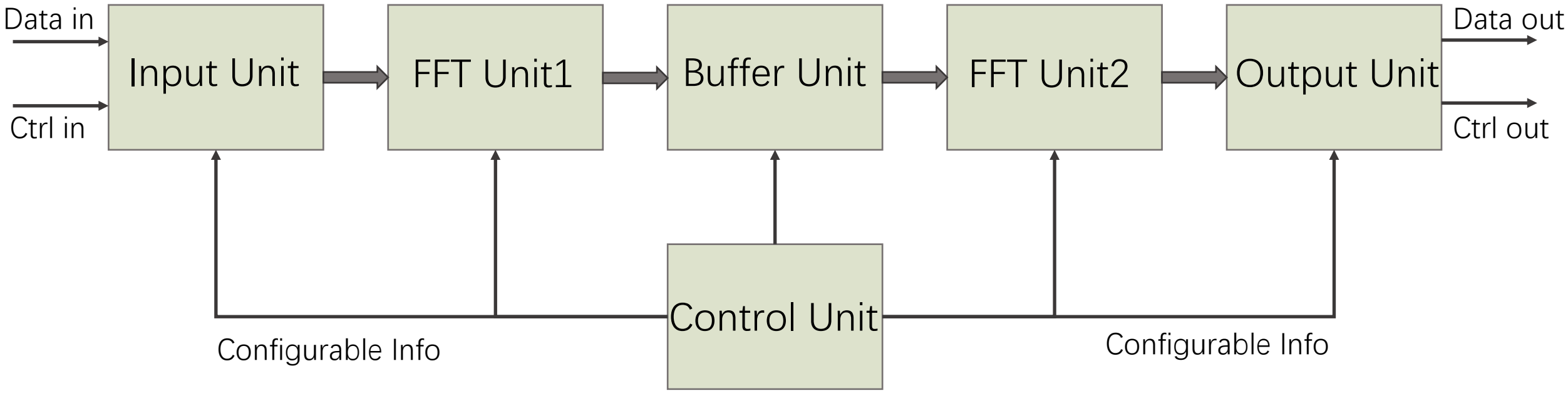
ABOUT THE PROJECT

Key words: FFT, Cooley-Turkey algorithm, *configurability*

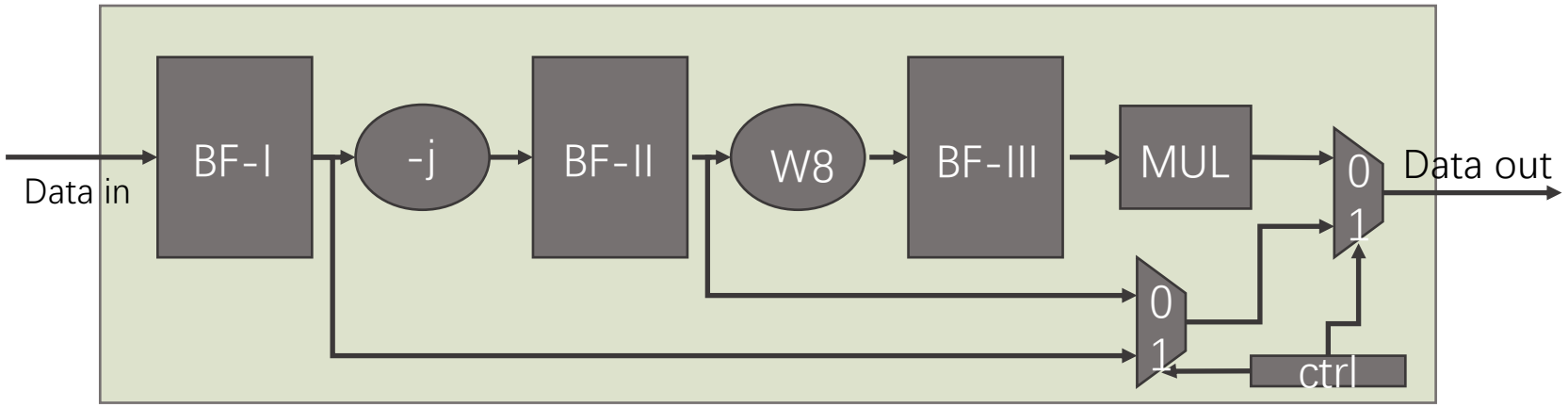


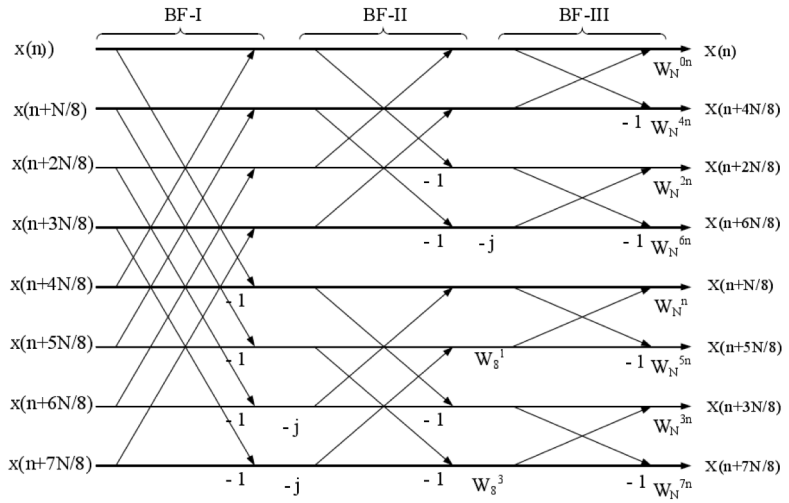
- The project is a cource project of "VLSI Design of Digital Signal Processing".

DETAILS

- A configurable FFT processor using the Cooley-Turkey algorithm for frequency-by-frequency extraction was implemented using VerilogHDL. The processor can handle Fast Fourier Transformation of arbitary 2^n points.

- The design was synthesized using the DC synthesis tool, and its performance metrics such as data throughput rate and integrated circuit area and power consumption were analyzed.



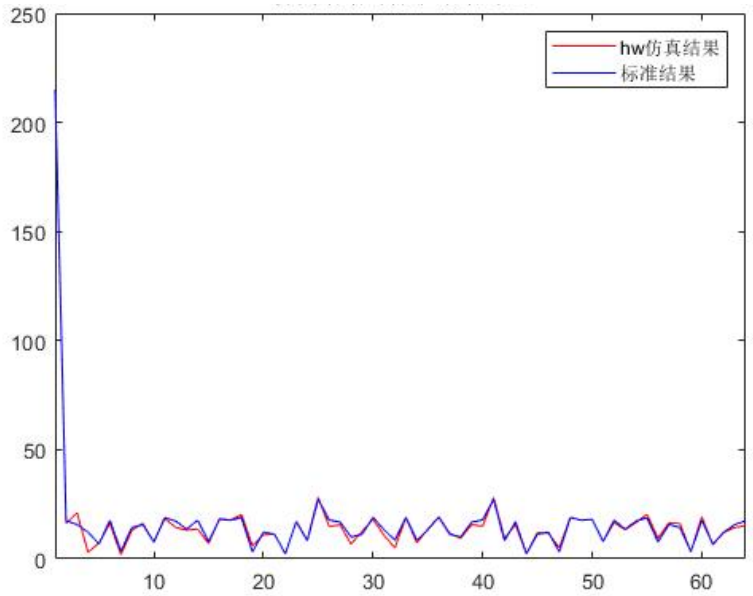


Detailed architecture of FFT unit. The architecture is determined according to radix 8 butterfly operation.

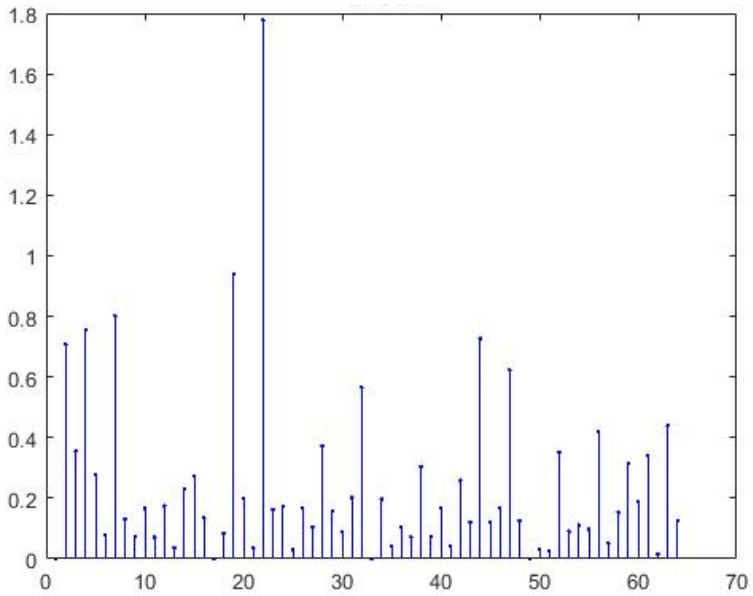
EXPLORATION

- Theoretical analysis and experiments are used to further consider the loss of precision and the output buffer backlog problem.

- Consider changing the pipeline structure to an iterative structure to increase the utilization efficiency and optimize the circuit area and power consumption.



Comparison of hw result(red line) and standard fft function result(blue line)



Relative error due to precision lost

- Python is used to do functional verification and analysis the relative error due to precision lost.