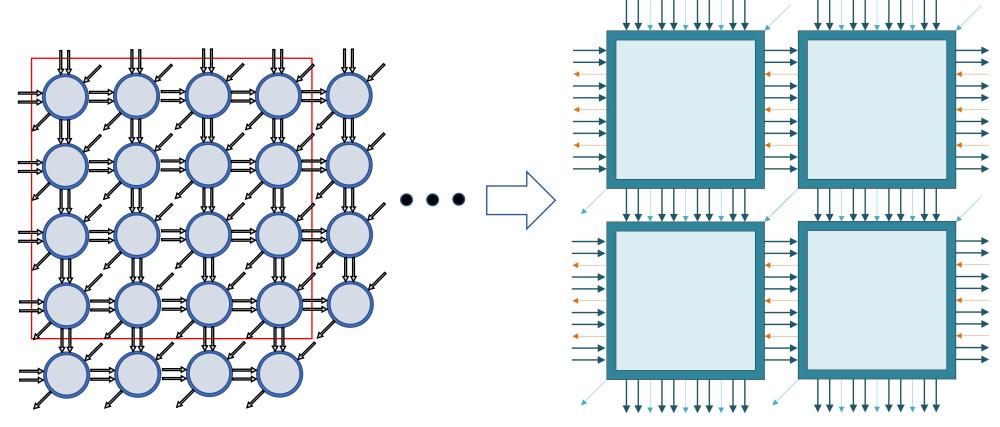
ABOUT THE PROJECT

Key words: GF(2m) field, multiplier, systolic array



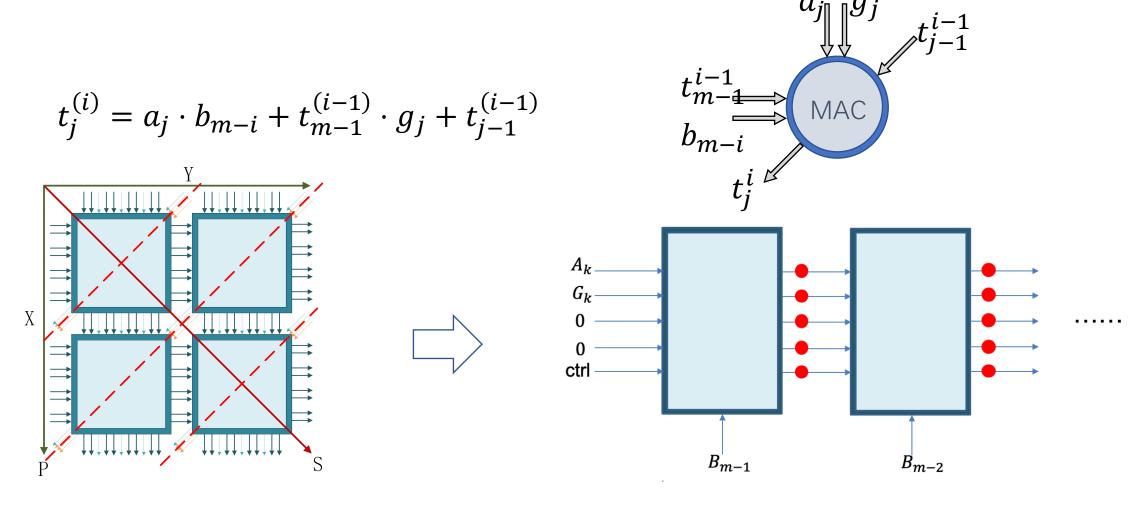
• The project is a cource project of "VLSI Design of Digital Signal Processing".

DETAILS

 Determine the basic unit architecture based on the knowledge of galois field and related high bits priority multiplication algorithm.

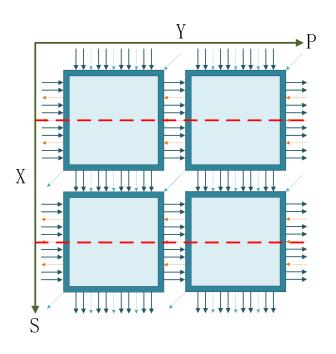
Design systolic array multiplier with parallel-bits input. Use systolic array projection to get pipline architecture in

order to improve area and energy consumption.



EXPLORATION

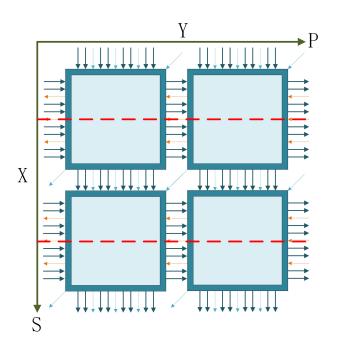
- Use DC compiler to do asic simulation and evaluate the performance of the design.
- Exploit the use of fine pipline and different projection vectors to further improve its performance.



e^T	$p^T e$	$s^T e$
$a_j, g_i, t_{j-1}^{(i-1)}(1, 0)$	0	1
$b_{m-i}, t_{m-1}^{(i-1)}(0,1)$	1	0
$t_{j}^{(i)}(1,-1)$	-1	1
$t_{j+1}^{(i+1)}$ (0,-1)	-1	0
HUE	1	

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Refreshed systolic array projection and the parameters