Bowen Huang

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Shanghai, China

PROFESSIONAL EXPERIENCE

Alibaba Group Jun 2021 - Present

Engineer, Alibaba Cloud-Server Development-Computing and Chip system Shanghai, China

- Responsible for accelerating video codec tasks on large-scale servers with FPGA based heterogeneous system

EDUCATION EXPERIENCE

Fudan University Sep 2019 - Jun 2021

Microelectronics, Master School of Microelectronics Shanghai, China

- Core GPA: 3.87 / 4.0 (Ranking 1/70)
- Supervisor: Prof. Yibo Fan

Nanjing University Sep 2015 - Jun 2019

Physics, Bachelor School of Physics Nanjing, China

- GPA: 3.73 / 4.00 (Ranking:30/159)

University of California, Berkeley Aug 2017 - Dec 2017

Physics, Exchange Term, School of Letters & Science Berkeley, USA

- GPA: 3.7 / 4.0

PUBLICATION

- **Bowen Huang**, Jinjia Zhou, Xiao Yan, Ming'e Jing, Rentao Wan and Yibo Fan. CS-MCNet: A Video Compressive Sensing Reconstruction Network with Interpretable Motion Compensation. Asian Conference on Computer Vision(ACCV), November 2020.
- **Bowen Huang**, Xiao Yan, Jinjia Zhou, and Yibo Fan.CSMCNet: Scalable Video Compressive Sensing Reconstruction with Interpretable Motion Estimation[J].arXiv preprint arxiv.2108.01522.
- Rentao Wan, Jinjia Zhou, **Bowen Huang**, Hui Zeng, Yibo Fan, Measurement Coding Framework with Adjacent Pixels based Measurement Matrix for Compressively Sensed Images, IEEE International Conference on Acoustics, Speach and Signal Processing(ICASSP), June 2021.
- Rentao Wan, Jinjia Zhou, **Bowen Huang**, Hui Zeng, Yibo Fan, "APMC: Adjacent Pixels based Measurement Coding System for Compressively Sensed Images", IEEE Transactions on Multimedia. (IF2020: 6.513) (accepted)

RESEARCH EXPERIENCE

Research on Compressive Sensing Based Video Codec Feb 2020 - Apr 2021

Fudan University/Osaka University, Advisor: AProf.Jinjia Zhou/Prof.Yibo Fan Shanghai, China

- Using neural network structures and video codec inter-frame prediction techniques to improve the speed and quality of video compressive sensing(CS) signal reconstruction.
  - Using Algorithm Unrolling to design a neural network structure with interpretable features. The reconstruction quality is enhanced by a multi-hypothesis motion compensation(MHMC) algorithm.
  - A test model CS-MCNet is built based on Pytorch, and the MHMC module is implemented through a fully connected layer. Compared with traditional methods, this method has 2-3 orders of magnitude improvement in reconstruction speed and 20% improvement in reconstruction quality(PSNR).
- A novel sampling and interpolation strategy is proposed to solve the task of multi-compression ratio CS.
  - The signal interception and interpolation strategies are designed so that the CS sampling and reconstruction of video signals under different compression ratios can be accomplished by one neural network with fixed structure parameters.
  - A test model CS-MCNet-ITP is build based on Pytorch, which is inherited from CS-MCNet. High quality signal interpolation is achieved by deconvolution. Experimentally, it is proved that the method can save 5 times the training and storage overhead with about 10% reconstruction quality loss.

- Based on the CS sampling rules, the sensing matrix and strategy are designed based on the similarity of adjacent pixels to improve the rate distortion optimization performance.

Design of High Performance, Low Cost H.264 Codec Chip Nov 2019 - Dec 2020

Fudan University, Advisor: Prof.Yibo Fan Shanghai, China

- A video codec chip that performs intra-frame prediction of the H.264 standard is designed. The chip is designed for a compression ratio of 30:1, and the maximum processing ability is 4K@60fps, YUV444, 10-bit color depth. The chip is designed to run at 400MHz, and has an area of 1672.94K gates(simulated by Design Compiler, TSMC 65nm, including on-chip memory). The chip is being taped out.
- Design core modules, including intra-frame prediction(PRD), mode decision(MD), and neighbour block maintenance(NBM).
  - Design the hardware architecture with a predefined number of clock cycles and storege resources by using finite state machines, pipeline, Valid/Ready handshake mechanism, and ping-pong buffer, etc.
  - The design is completed in Verilog HDL, and the functional verification is completed using NCVerilog based on the bus function model(BFM).
- Build the BFM in SystemVerilog, providing a universal verification environment for the whole project. Complete the functional verification and DC synthesization of the whole design.
  - The BFM has parameters that can be reconfigured randonly. It can also generate test vector and check DUT output automatically, providing simple and efficient functional verification.
  - SystemVerilog-based software reference models for complex modules are implemented and integrated into the verification environment to perform hardware-software co-verification to improve the verification efficiency.

Design of High Performance AV1 Codec Jan 2021 - Present

Fudan University, Alibaba Group, Advisor: Prof.Yibo Fan Shanghai, China

- Investigate the impact of screen content coding tool(SCC) based on the AV1 reference software AOM.
  - Test the impact of palette mode and intrabc mode on the coding performance of images in Taobao APP. Compare the results with HEVC to analyze the differences.
  - Test the effect of different combinations of parameters(SCC adaptive threshold, number of colors in the palette mode, etc.). Determine the optimal reference algorithm considering the limitation of hardware implementation on memory access and computational component utilization.
- Reduce the complexity of pattern selection in intra-frame prediction by employing pre-selection, early stop and other methods.
  - Quantify the neural network parameters in the mode selection with 16 bits, and change the anti-trigonometric function into interval determination, thus reducing the complexity of the hardware realization.
  - Change the percentage of individual components in the histogram into total number, and fix the number of excluded angular patterns to improve the hardware design friendliness.
- Participate in the hardware design of AV1 codec. The codec will be applied to heterogeneous computing system of large-scale servers, aiming to improve the display quality of images in APPs, and reduce the storage and bandwidth consumption of servers.

HONORS & AWARDS

Shanghai Outstanding Graduates(Top 1%)	Jun 2021
National Scholarship(Top 1%)	Oct.2020
Outstanding Students of Fudan University for the 2019-2020 academic year	May 2020
President of the Students Union of School of Physics, Nanjing University	Jun 2016 - Jun 2017

MISCELLANEOUS

- **Languages:** Chinese(native), English:TOEFL 109(R:30,L:30,S:24,W:25)/GRE 322+4
- **Program Languages:** Verilog, SystemVerilog, Python, C++, Matlab
- **Software:** Tools for FPGA design and ASIC design, such as Vivado, VCS, NCVerilog, etc.
- **Interests:** Badminton, Cycling, Electric Guitar, Drawing