Single-cycle MIPS Signal Naming

Signal Definition	Signal Domain	Previous Naming	New Naming
Data memory to RF steering (CU output)	control	MemtoReg	dm2reg
Destination register steering (CU output)	control	RegDst	reg_dst
ALU source steering (CU output)	control	ALUSrc	alu_src
Jump steering (CU output)	control	Jump	jump
Branch steering (CU output)	control	Branch	branch
ALU zero flog	status	Zero	alu_zero
PC source steering	control	PCSrc	pc_src
Data memory write enable (CU output)	control	MemWrite	we_dm
Register write enable (CU output)	control	RegWrite	we_reg
ALU control (CU output)	control	ALUControl	alu_ctrl
ALU input port A	datapath	SrcA	alu_pa
ALU input port B	datapath	SrcB	alu_pb
ALU output	datapath	ALUResult	alu_out
Instruction (IM output)	datapath	Instr	instr
Write address to RF	datapath	WriteReg	wa_rf
Write data to RF	datapath	Result	wd_rf
Write data to data memory	datapath	WriteData	wd_dm
Read data from data memory	datapath	ReadData	rd_dm
Signe extended immediate value	datapath	SignImm	sext_imm
PC current value	datapath	PC	pc_current
PC next value	datapath	PC’	pc_next
PC plus 4 value	datapath	PCPlus4	pc_plus4
Branch target address	datapath	PCBranch	bta
Jump target address	datapath	PCJump	jta