CDS1114

Introduction to Digital Systems

Latches & Flip-flops I

Lecture outcome

- By the end of today's lecture you should know
  - how basic gates combine to form latches
  - the operation of basic S-R, gated S-R and D latch
    - learn the difference between active HIGH and active LOW latches
    - identify the states of any latch and invalid con

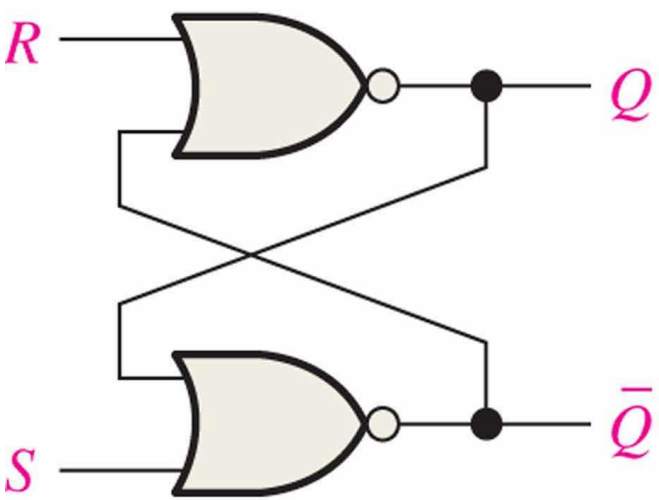
Latches

- A latch is a temporary storage device that has two stable states – SET and RESET
  - Sometimes called *bistable logic device* or *multivibrator*
- They retain their states indefinitely until certain conditions change them
- Similar to flip-flops (to be covered later), latches reside in either of two states using a feedback style arrangement in which outputs are fedback to opposite inputs

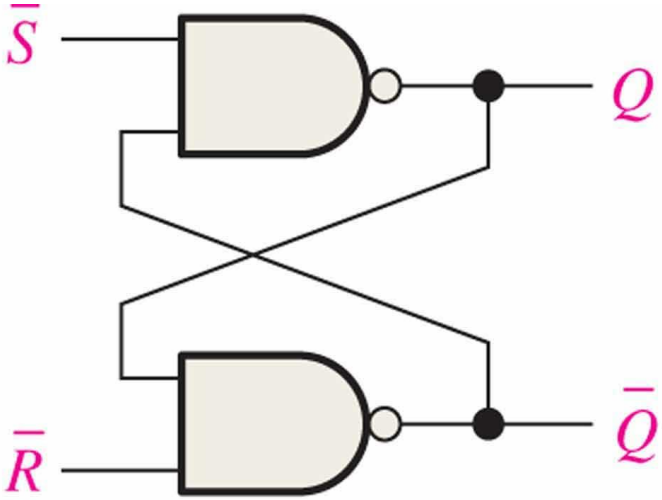
- Latches begin the study of sequential logic which will later cummulate with counters and shift registers

Set-Reset (S-R) Latch

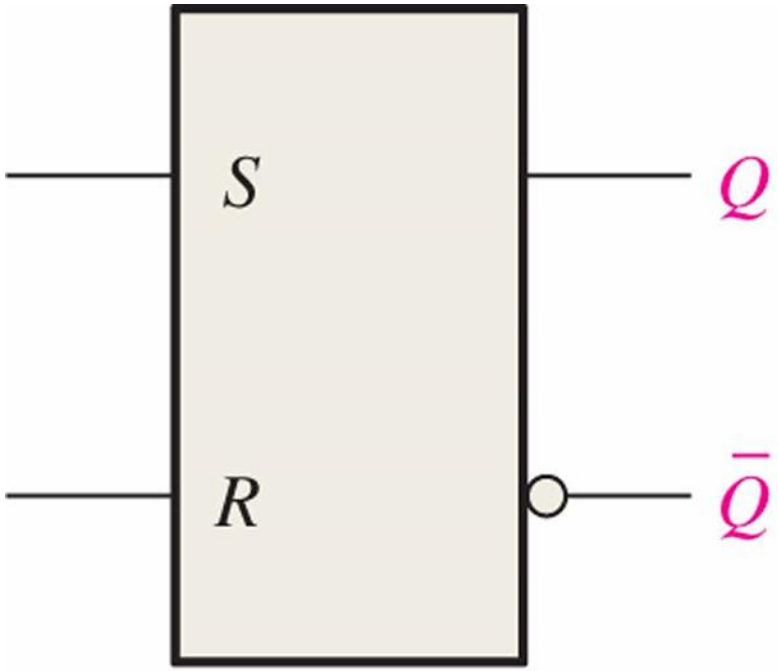
- Two types of S-R latch can be formed depending on the gates used
  - using two cross-coupled NOR gates - the latch responds to active-HIGH inputs
  - using two cross-coupled NAND gates - responds to active-LOW inputs



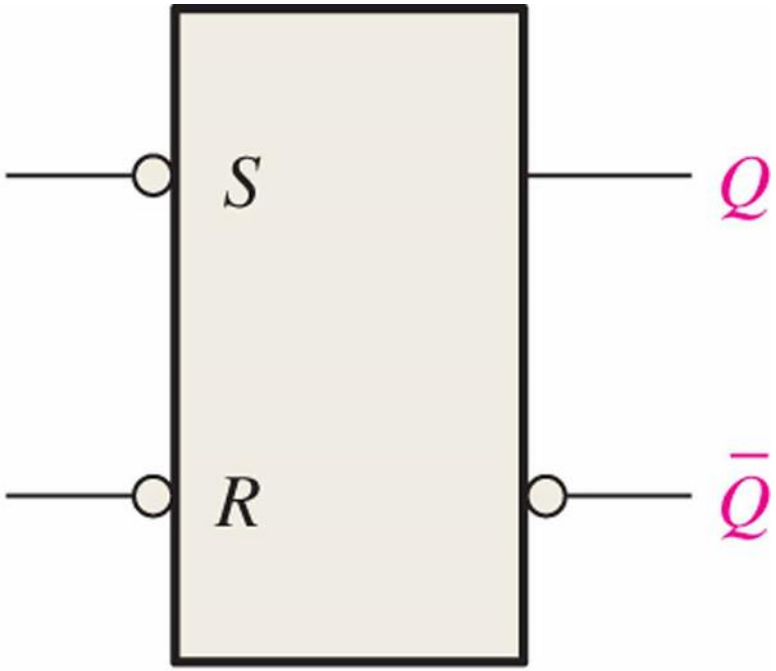
(a) Active-HIGH input S-R latch



(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch



(a) Active-HIGH input S-R latch

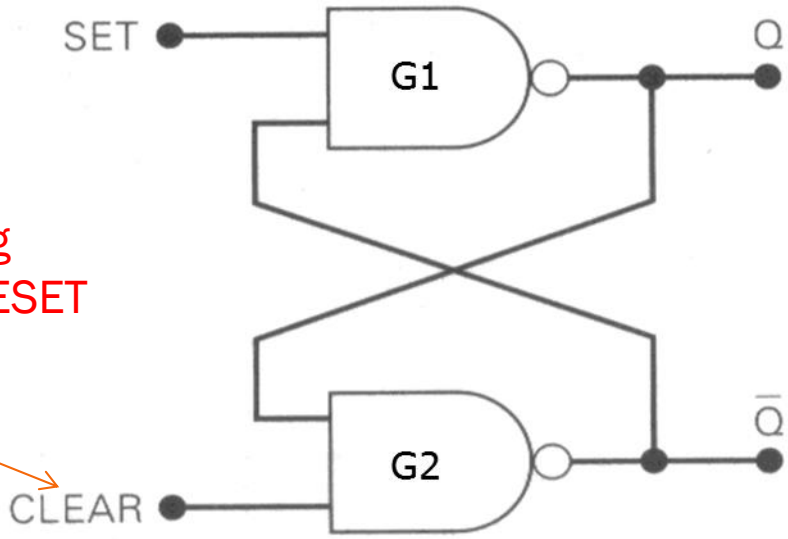


(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

Active-LOW S'-R' Latch

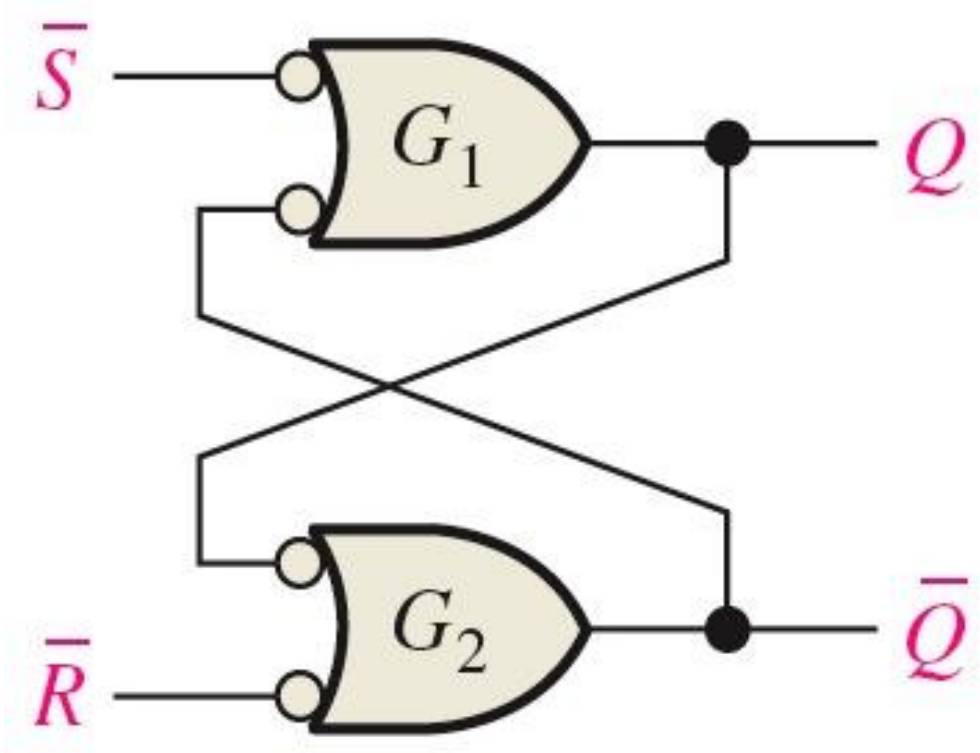
- Two NAND gates are cross-coupled so that the output of G1 is connected to one of the inputs of G2, and vice versa
- There are two latch inputs
  - the SET input is the input that sets Q to the 1 state.
  - The CLEAR input is the input that resets Q to the 0 state
- The gate outputs, labeled Q and Q', respectively, are latch outputs.
- Under normal conditions, the outputs will always be the inverse of each other

Note: the following diagrams show the RESET input as CLEAR



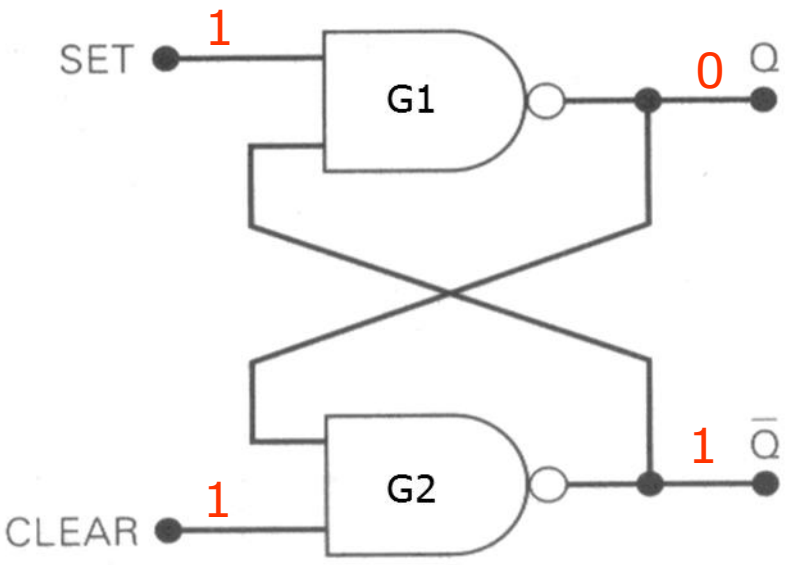
Active-LOW S'-R' Latch

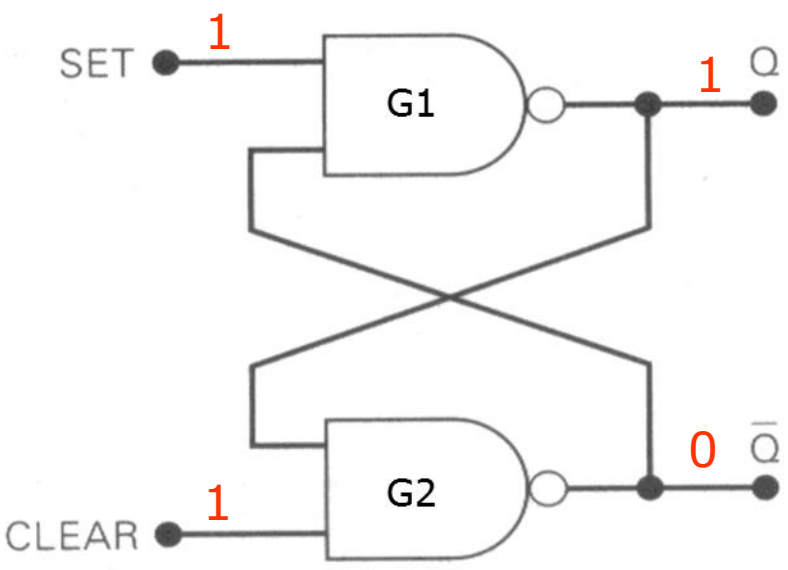
- An alternative to using two NAND gates is to use two negative-OR gates (this is the example shown in the textbook)



S'-R' latch – resting state

- In a resting/stable state, the inputs S' and R' are normally in HIGH state





- Assuming that Q=0 (and thus Q'=1), inputs to G2 are 0 and 1 which produce Q'=1 (because NAND) so Q' remains high
- With Q'=1, both inputs to G1 are high and produce Q=0
- Conversely, if Q=1 and Q'=0, the output would be similar but inversed with Q maintaining a high output and Q' a low
  - In effect, with both inputs S and R at high, the outputs remain unchanged from the state they are currently in

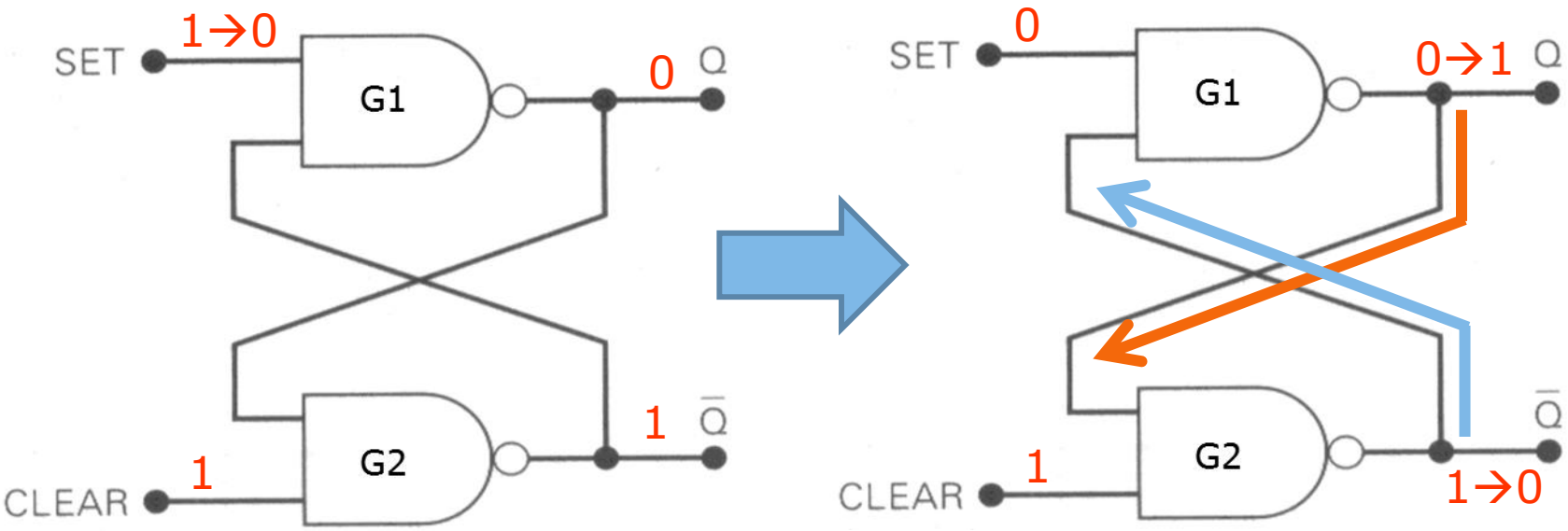
S'-R' latch – resting state

- Summary of condition SET = 1 and CLEAR =1.
  - There are two possible output states when SET and RESET = 1, which are either Q =0 and Q' = 1 or Q =1 and Q' = 0.
  - The outputs are remain unchanged comparing with previous state even there is new clock pulse or new input S =1 and R =1

- To change the state of the S'-R' latch, one of the inputs will be pulsed LOW whenever we want to change the latch outputs

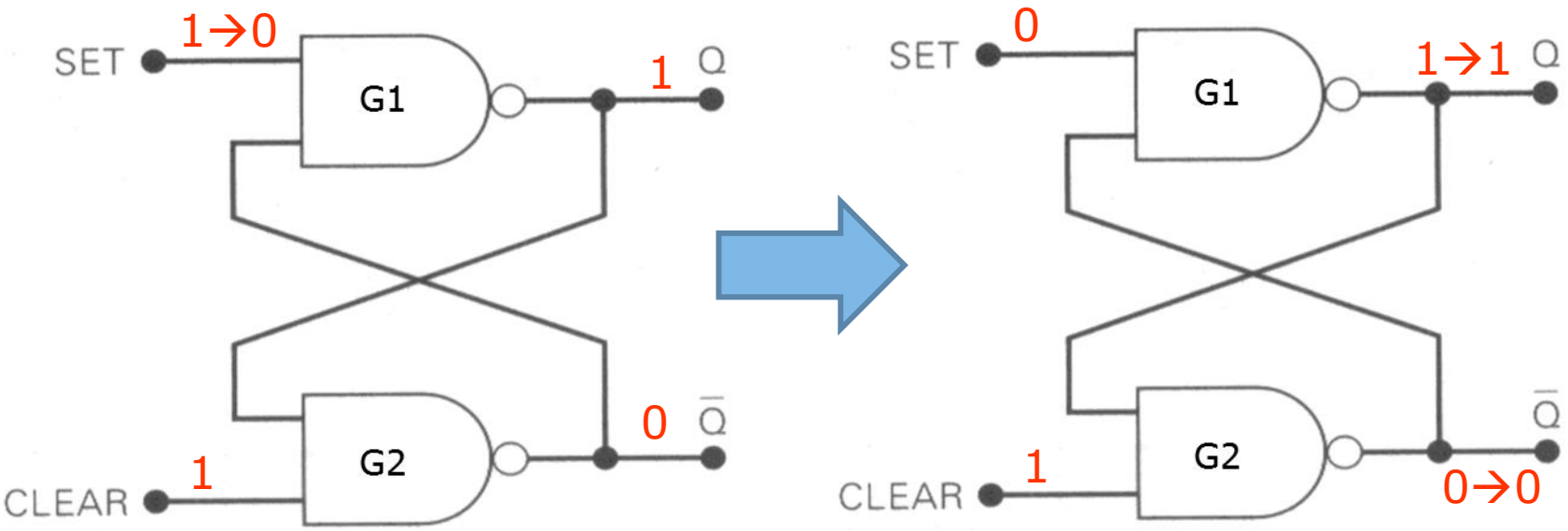
S'-R' latch – SET state

- In the SET state, the S input is made low (because active-LOW)
- Assuming that the current state of the latch was from resting, the following occurs



- As S is pulsed to LOW, Q will go HIGH (Q=1) and this causes both inputs to G2 to become HIGH and causes Q' to go LOW
- Thus the latch ends up with Q=1 and Q'=0

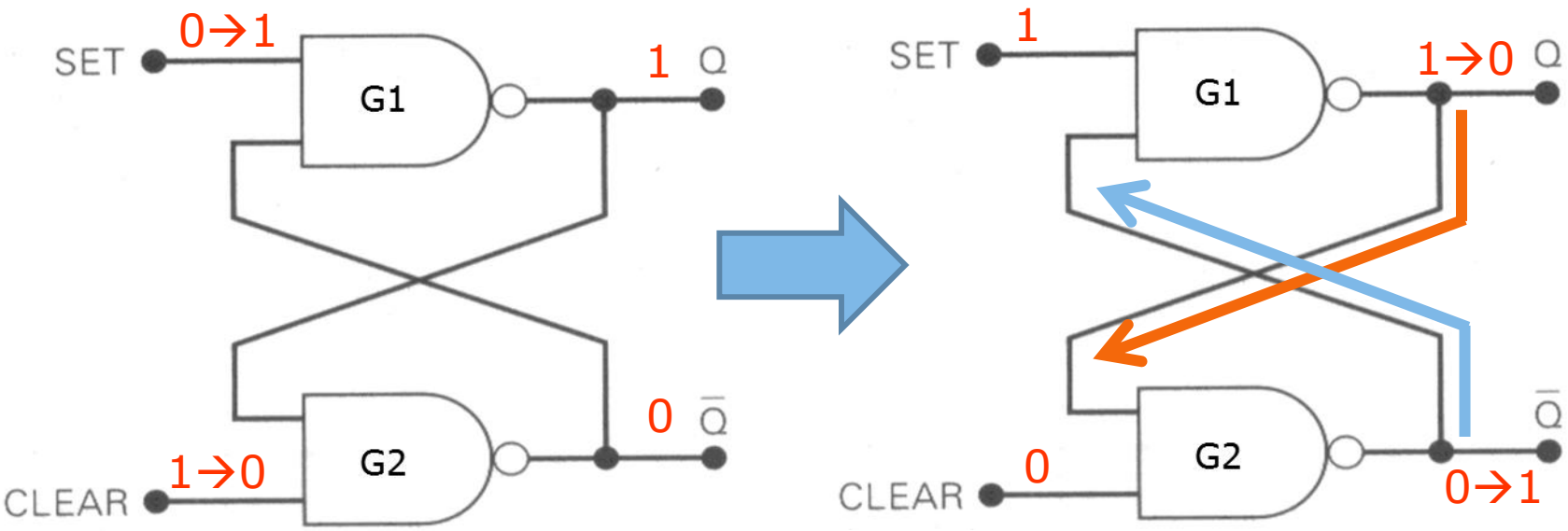
- If prior to input S being made LOW the outputs were Q=1 and Q'=0 (i.e. the latch is already in SET state), the following occurs:



- You can see that the LOW input to G1 does not affect the output of the latch and it remains SET
- Summary of condition SET = 0 and RESET =1.
  - A LOW input on SET will always cause the latch to end up in the Q = 1 state and Q' =0.
  - This operation is called *setting the latch*

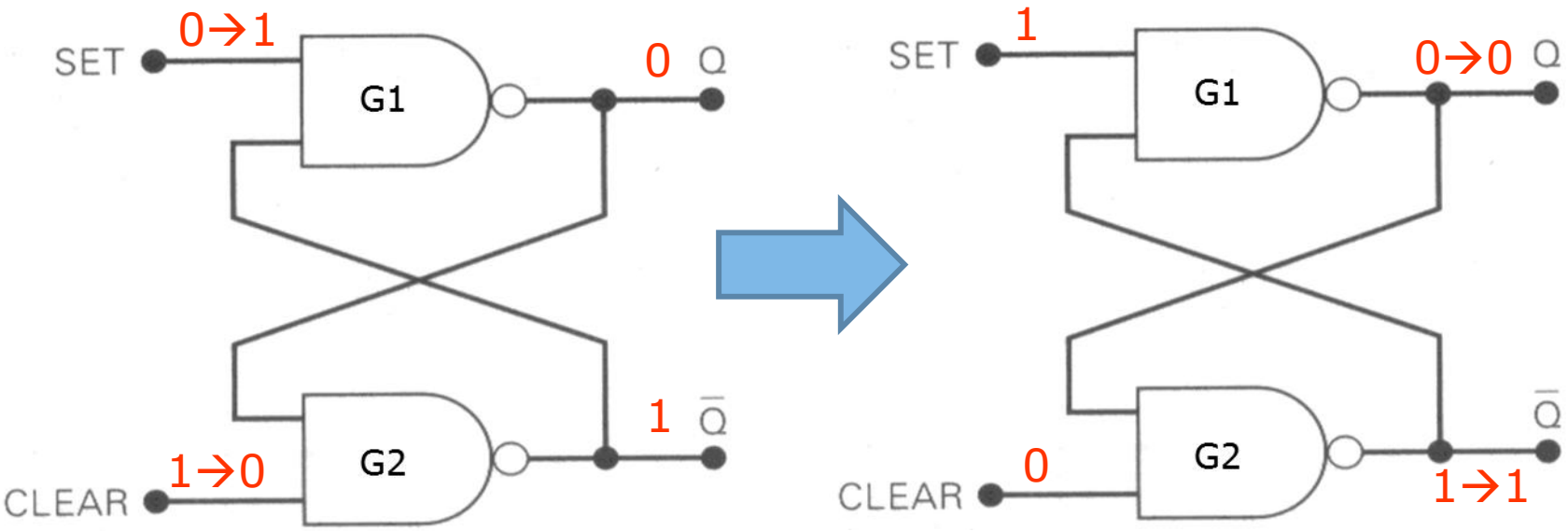
S'-R' latch – RESET state

- To switch the ALS-R latch to RESET (i.e resetting the latch), the R input is made LOW
- If the current state is SET, the following occurs



- When R is LOW, both inputs to G2 now result in a HIGH output Q'=1
- Both inputs to G1 are now HIGH and result in an output Q=0 thus resetting the latch

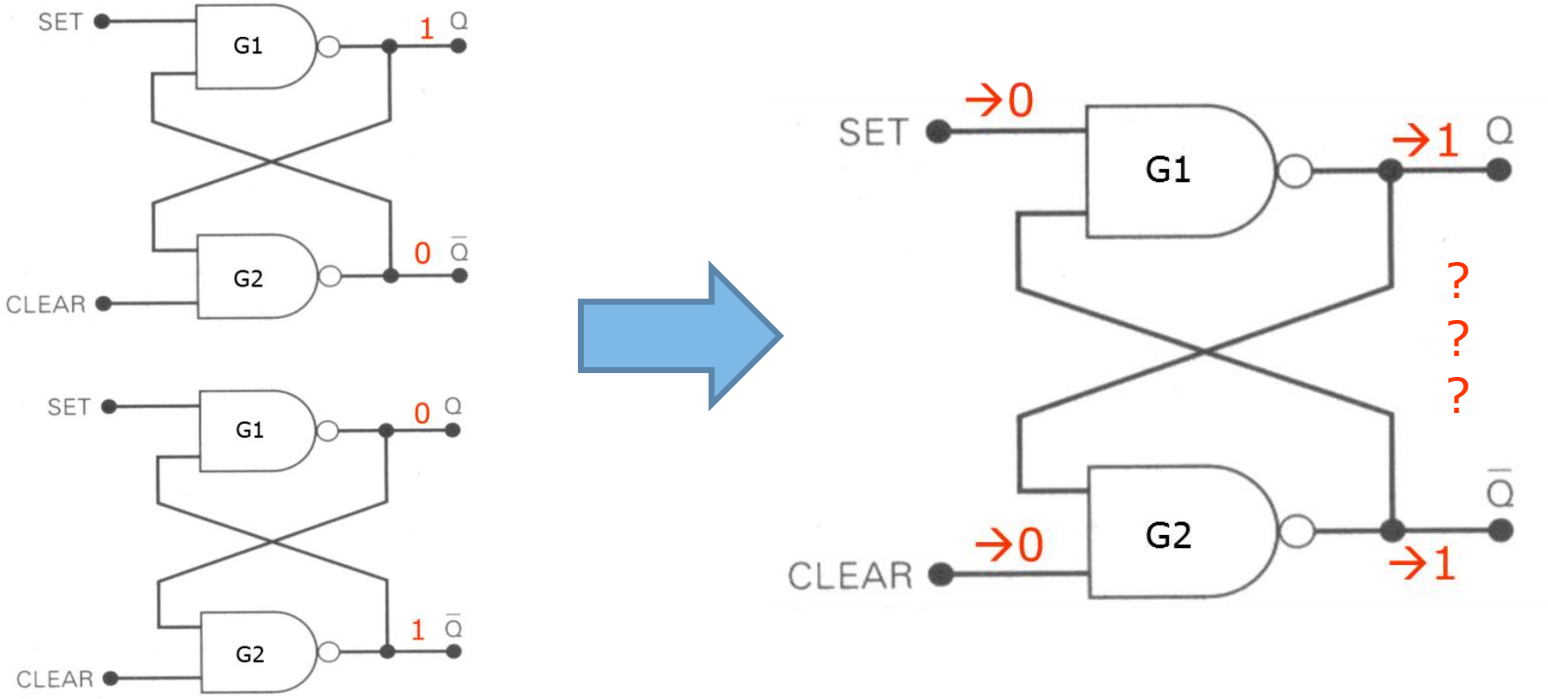
- If prior to input R being made LOW the outputs were Q=0 and Q'=7 (i.e. the latch is already in RESET state), the following occurs:



- As before, the LOW input to G2 does not affect the output of the latch and it remains RESET
- Summary of condition SET = 1 and RESET =0.
  - A LOW pulse on the RESET input will always cause the latch to end up in the Q = 0 state and Q' =1.
  - This operation is called clearing or resetting the latch

S'-R' latch – invalid state

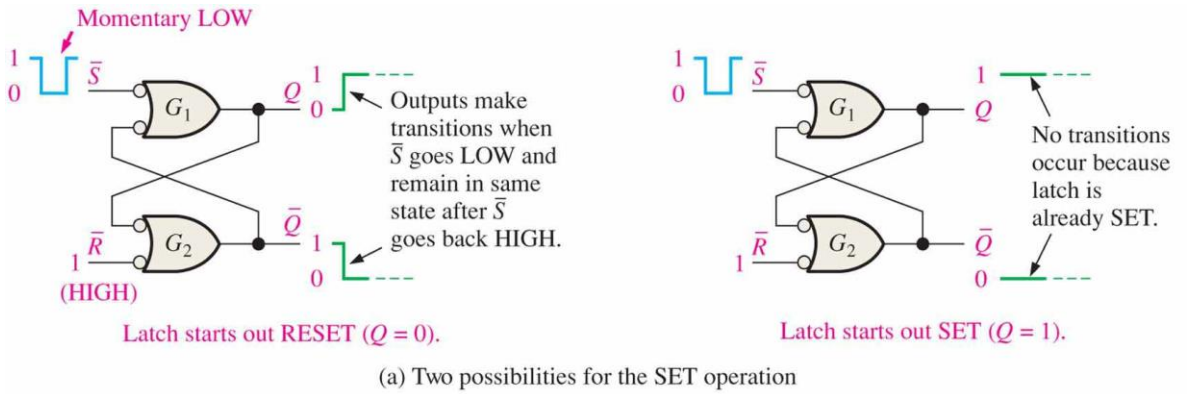
- When SET and RESET inputs are simultaneously made LOW, this will produce HIGH levels at both NAND output, Q = 1 and Q' = 1 and violating the complement nature of the outputs
  - This condition occurs no matter what state the latch was currently in
- This is an undesired condition because the two outputs are supposed to be inverses of each other



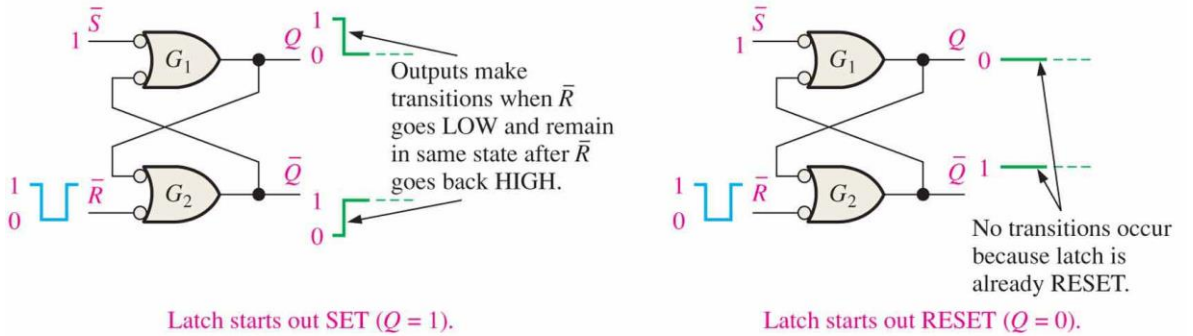
- When in invalid state, if both input LOWs are released (made HIGH) simultaneously both outputs will attempt to go LOW and thus propagating the invalid state.

- In reality, there is always *some* miniscule difference in the propagation time delay at the gates so one of the gates will dominate in its transition to the LOW (or HIGH) output state → the slower gate will then always be forced to be complement
    - In this scenario, you can NOT predict the next state of the latch

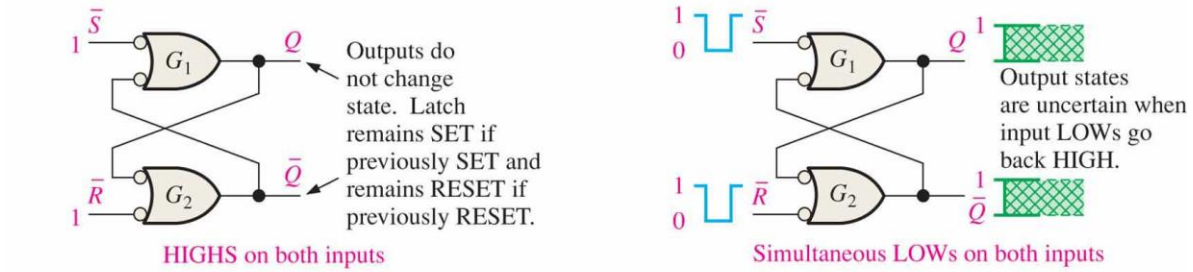
S'-R' latch – state summary



(a) Two possibilities for the SET operation



(b) Two possibilities for the RESET operation



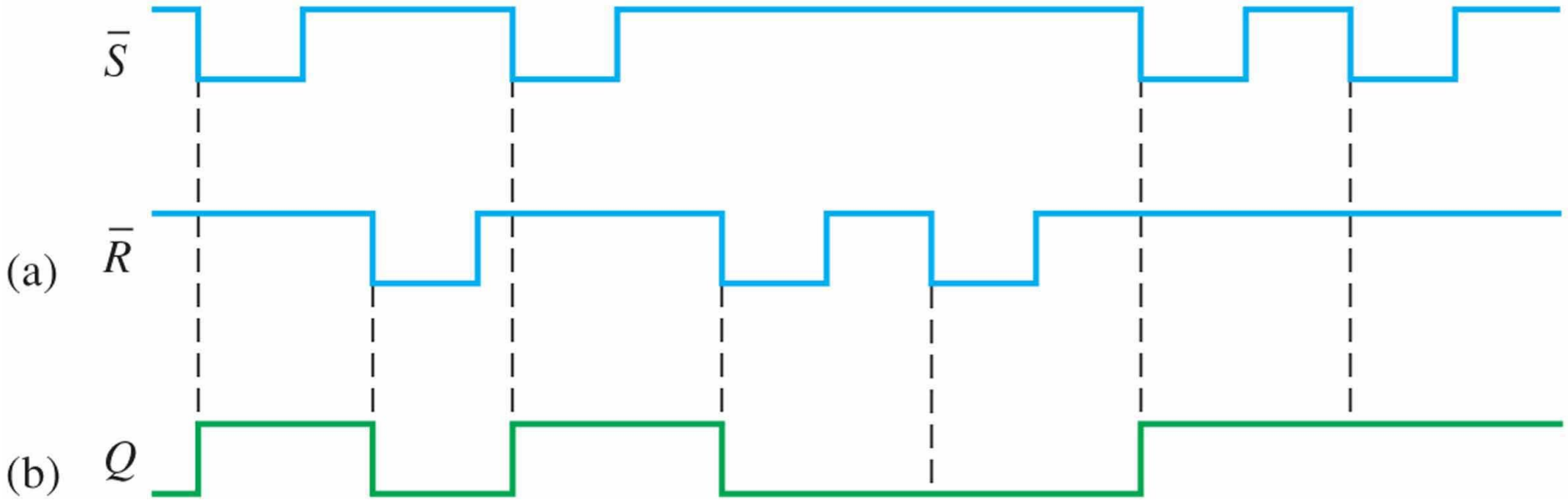
(c) No-change condition

(d) Invalid condition

S	R	Q
1	1	No change/resting
0	1	Q=1 and Q'=0
1	0	Q=0 and Q'=1
0	0	Invalid/unpredictable

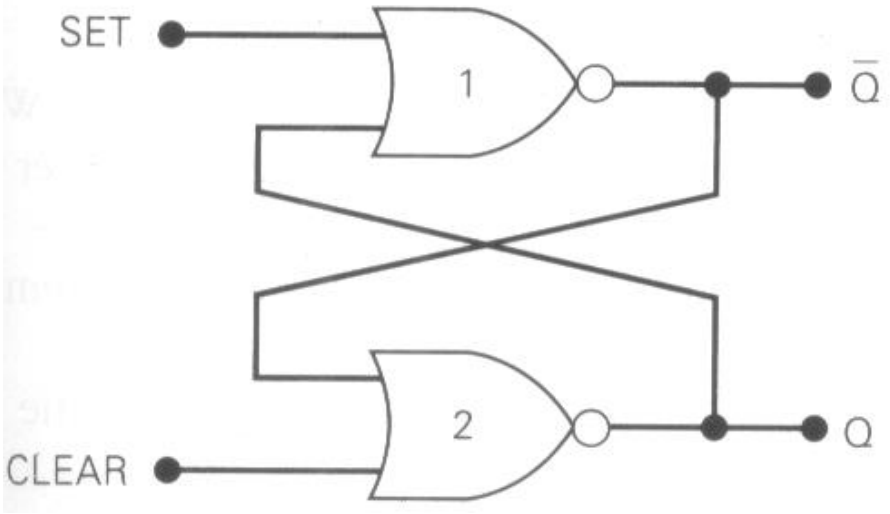
S'-R' Latch Example

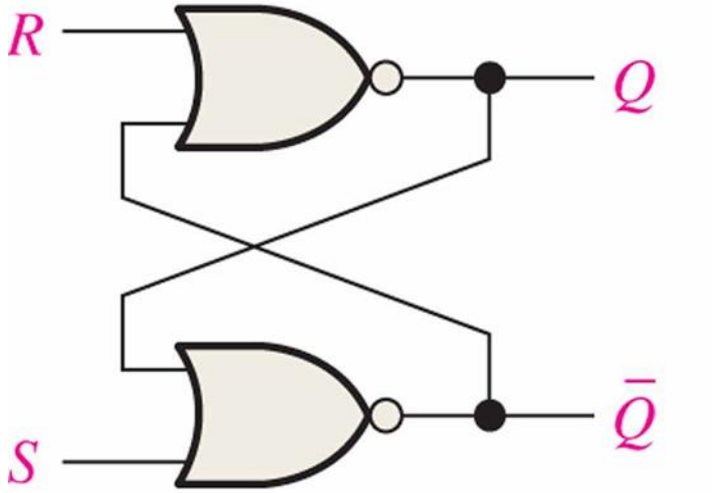
- Assuming that Q = 0 initially, determine the output Q for the NAND S'-R' latch inputs shown below



Active HIGH S-R latch

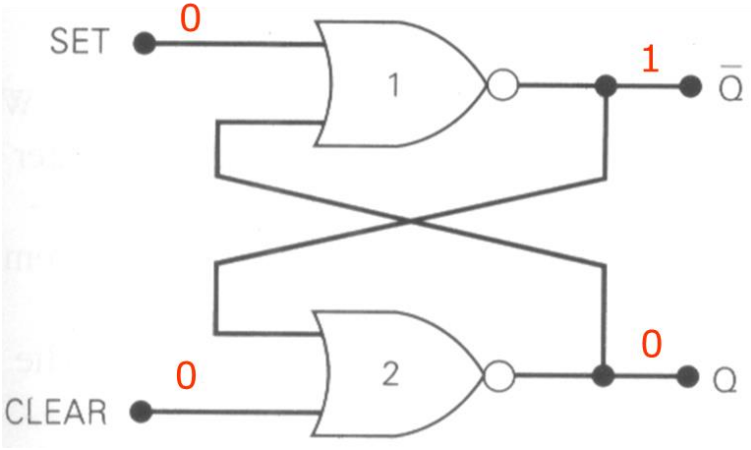
- Two cross-coupled NOR gates can be used as a active HIGH S-R latch (also known as a NOR gate latch)
- The arrangement is similar to the NAND latch except the Q and Q' outputs have reversed position against the inputs (i.e. S→Q' and R→Q)

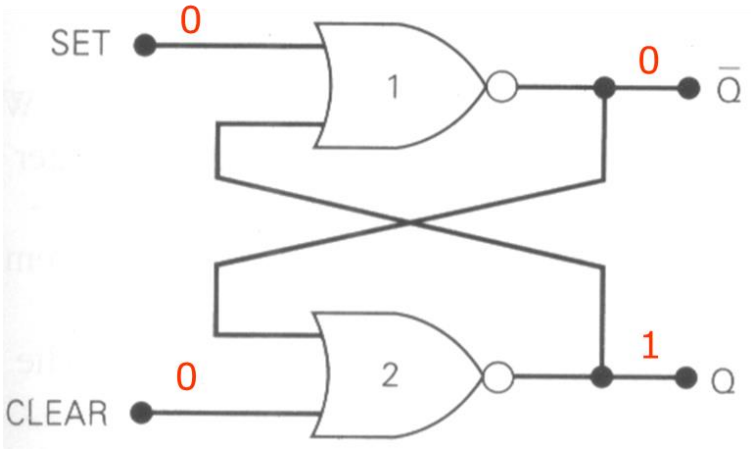




S-R latch – resting state

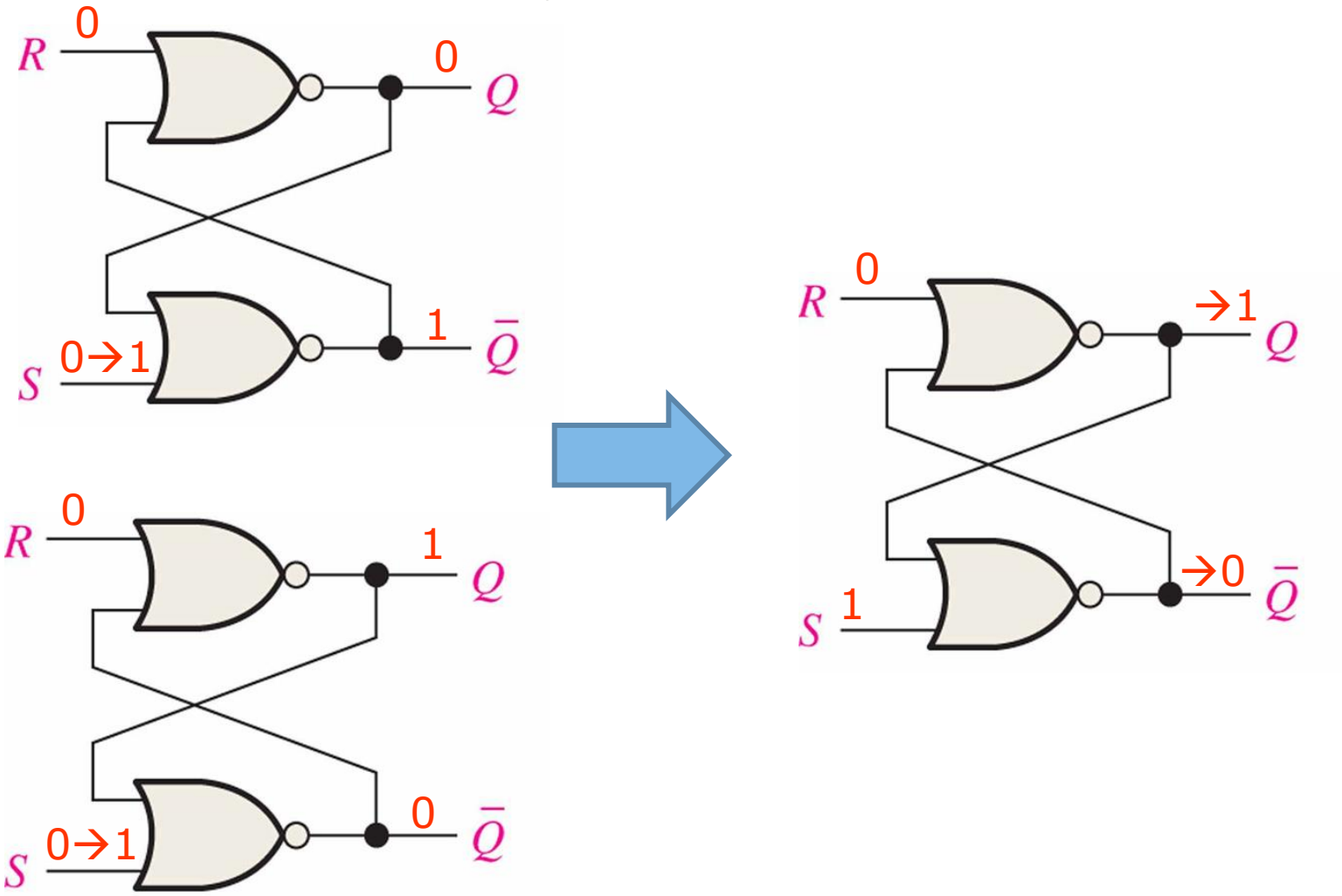
- In a resting/stable state, the inputs S and R are normally in LOW state → the latch remains in whatever state it is currently in/started with





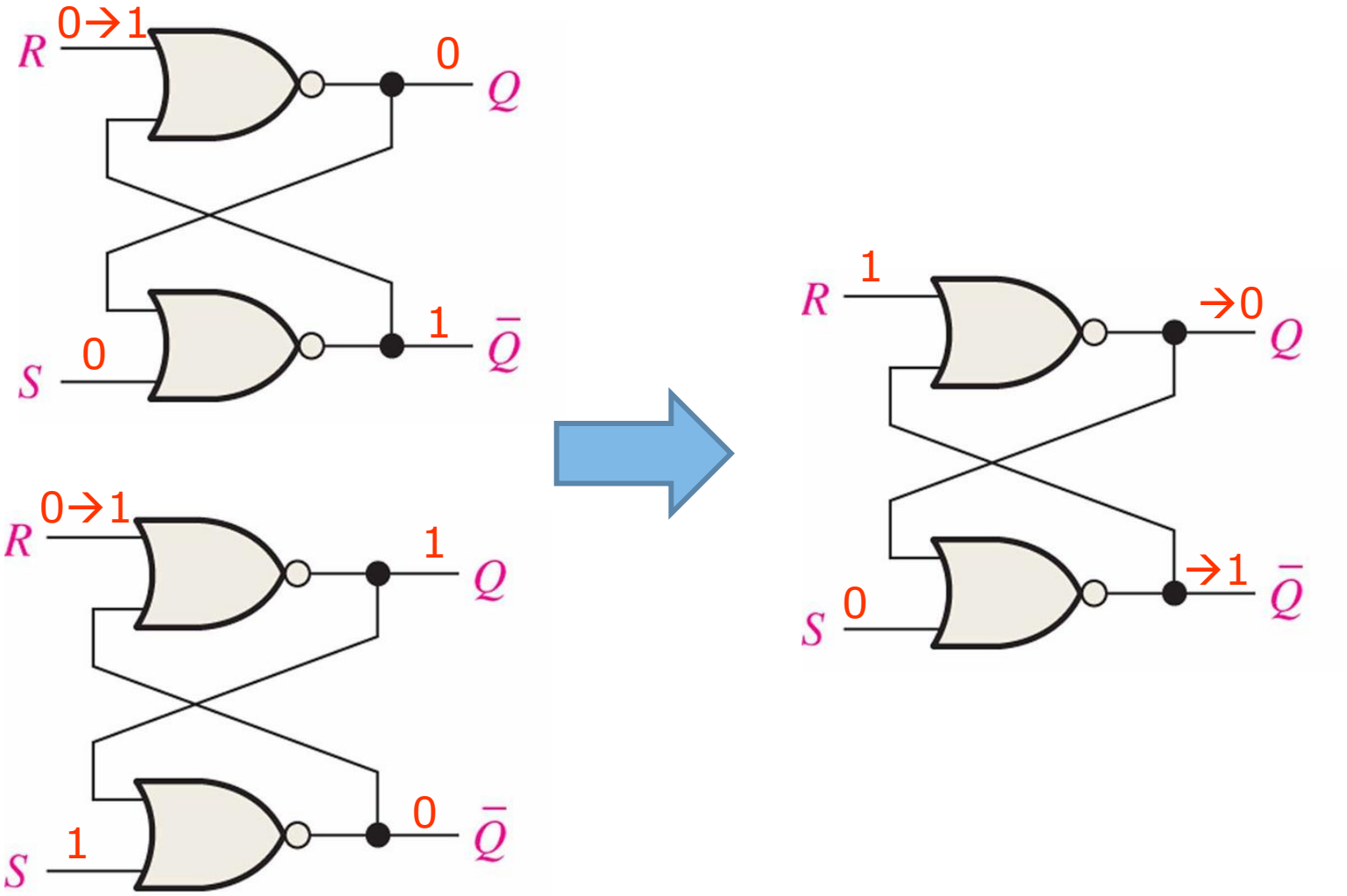
S-R latch – SET state

- The S-R latch moves into a SET state when the S input is made HIGH
- If the initial state was SET, the latch remains as SET



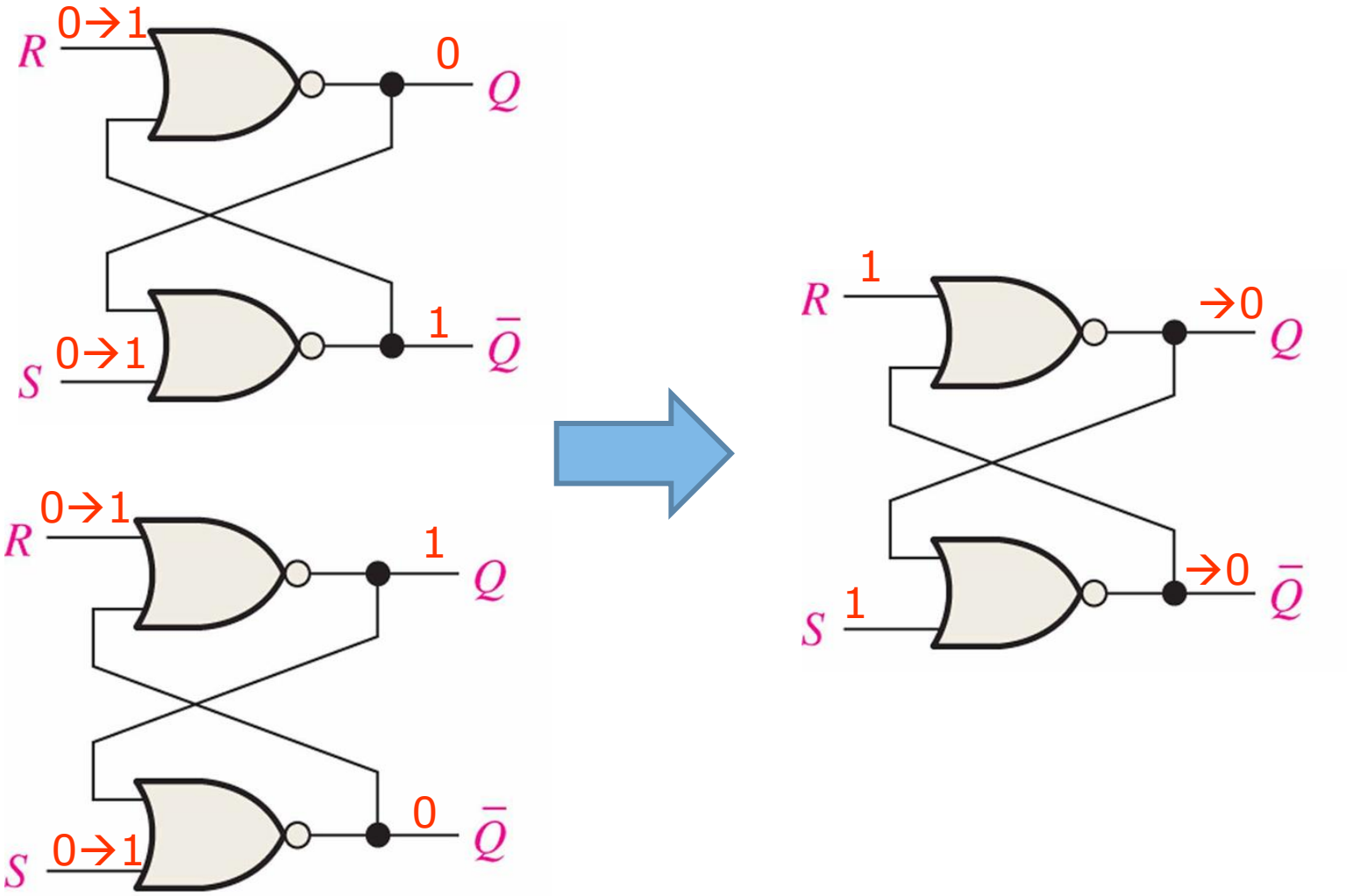
S-R latch – RESET state

- The S-R latch moves into RESET state when the R input is made HIGH
- If the initial state was RESET, the latch remains as SET



S-R latch – invalid state

- Similar to the S'-R' latch, the S-R latch also encounters an invalid state but this time when both inputs to S and R are HIGH simultaneously

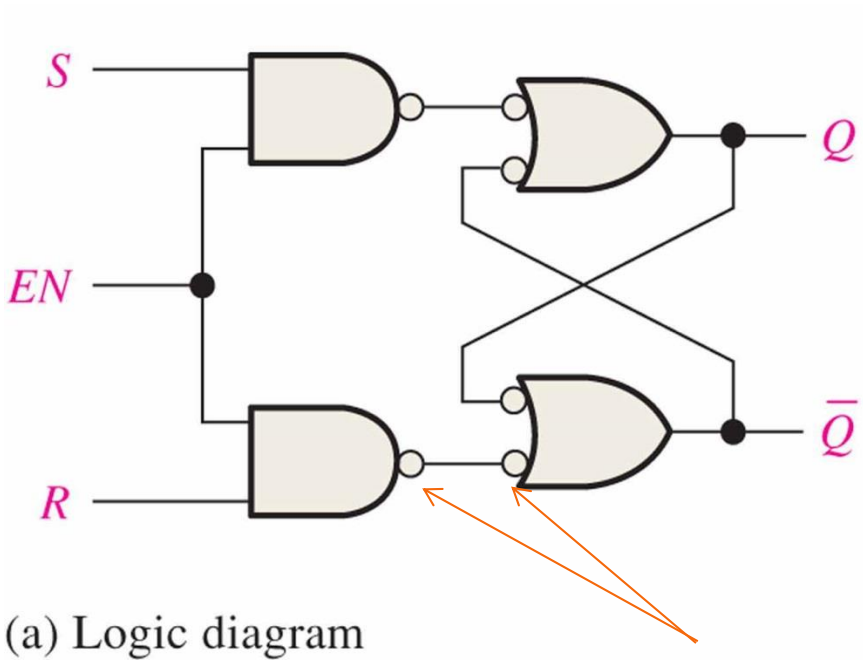


S-R latch – state summary

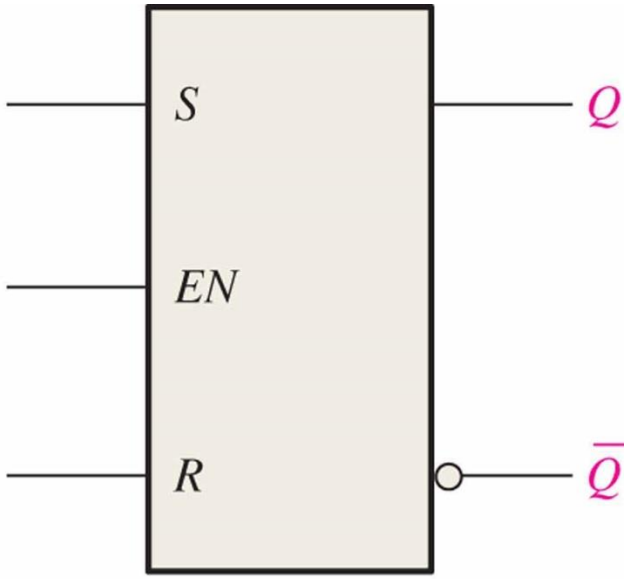
R	S	Q	Action
0	0	Last value	No change
0	1	1	Set
1	0	0	Reset
1	1	–	Invalid condition

Gated latch

- A gated latch (either S-R or S'-R') adds another input – ENABLE – to basically turn the latch 'on' or 'off'
- The following shows the gated S-R latch logic diagram and symbol



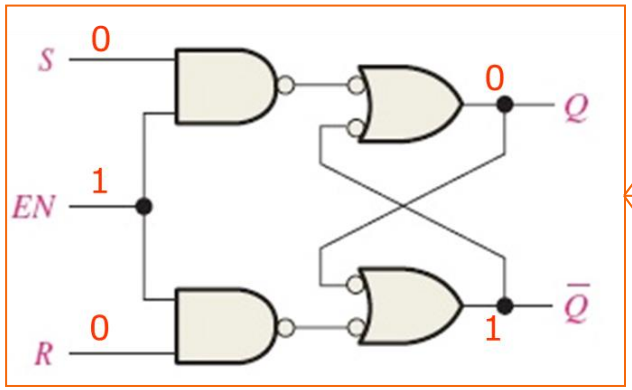
(a) Logic diagram



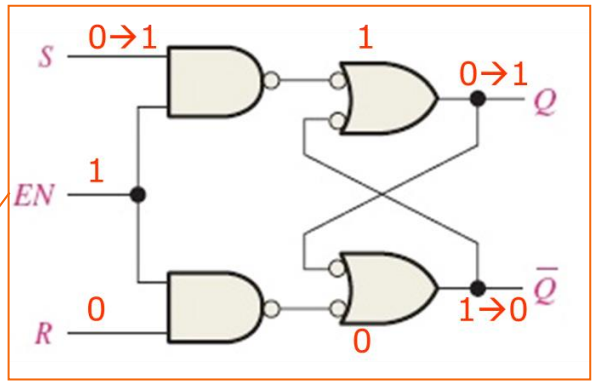
(b) Logic symbol

opposing bubbles cancel each other out!!

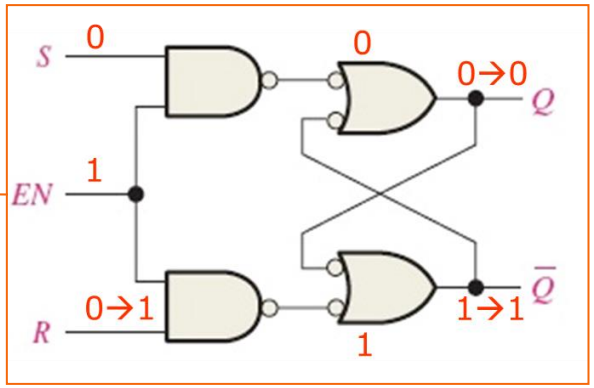
- In the gated latch shown, the latch will not change until EN is HIGH (=1)
- As long as EN=1, the output is controlled by the S and R inputs
  - Invalid state can continue to occur when both S and R are simultaneously HIGH



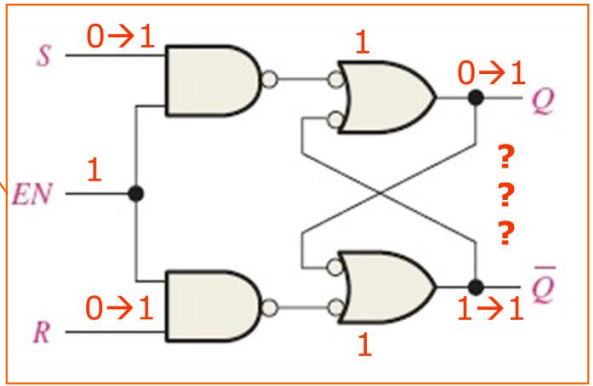
set



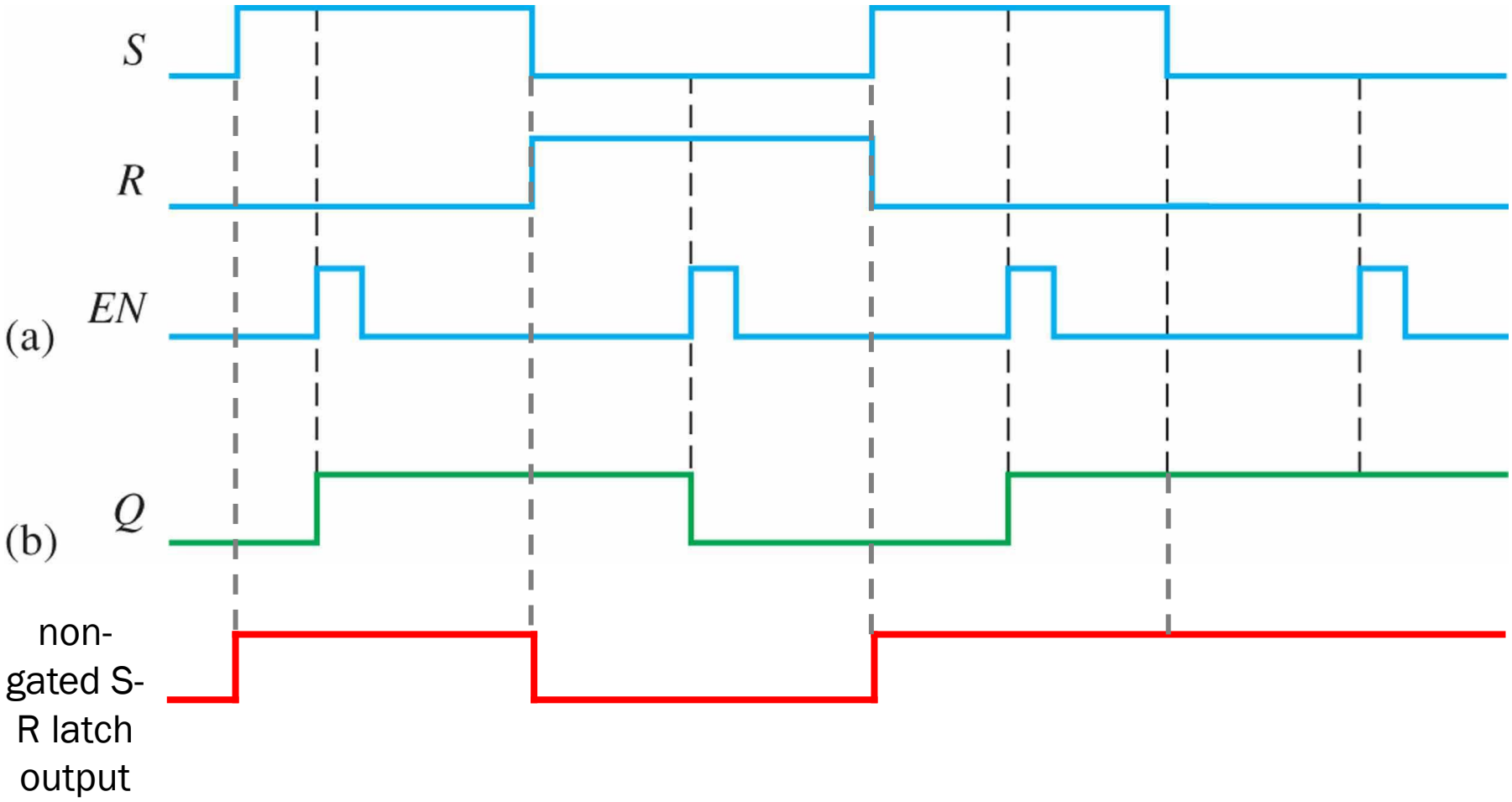
reset



invalid

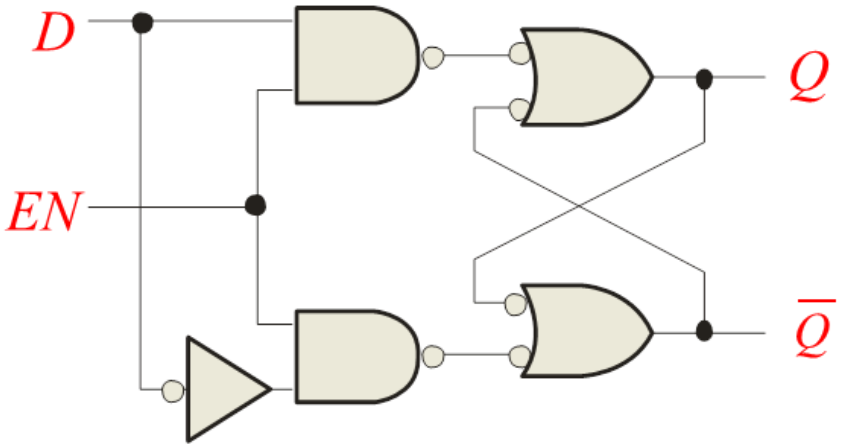


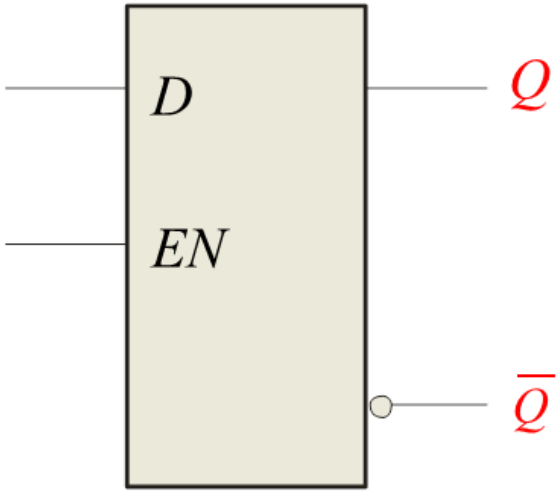
Gated S-R latch timing diagram



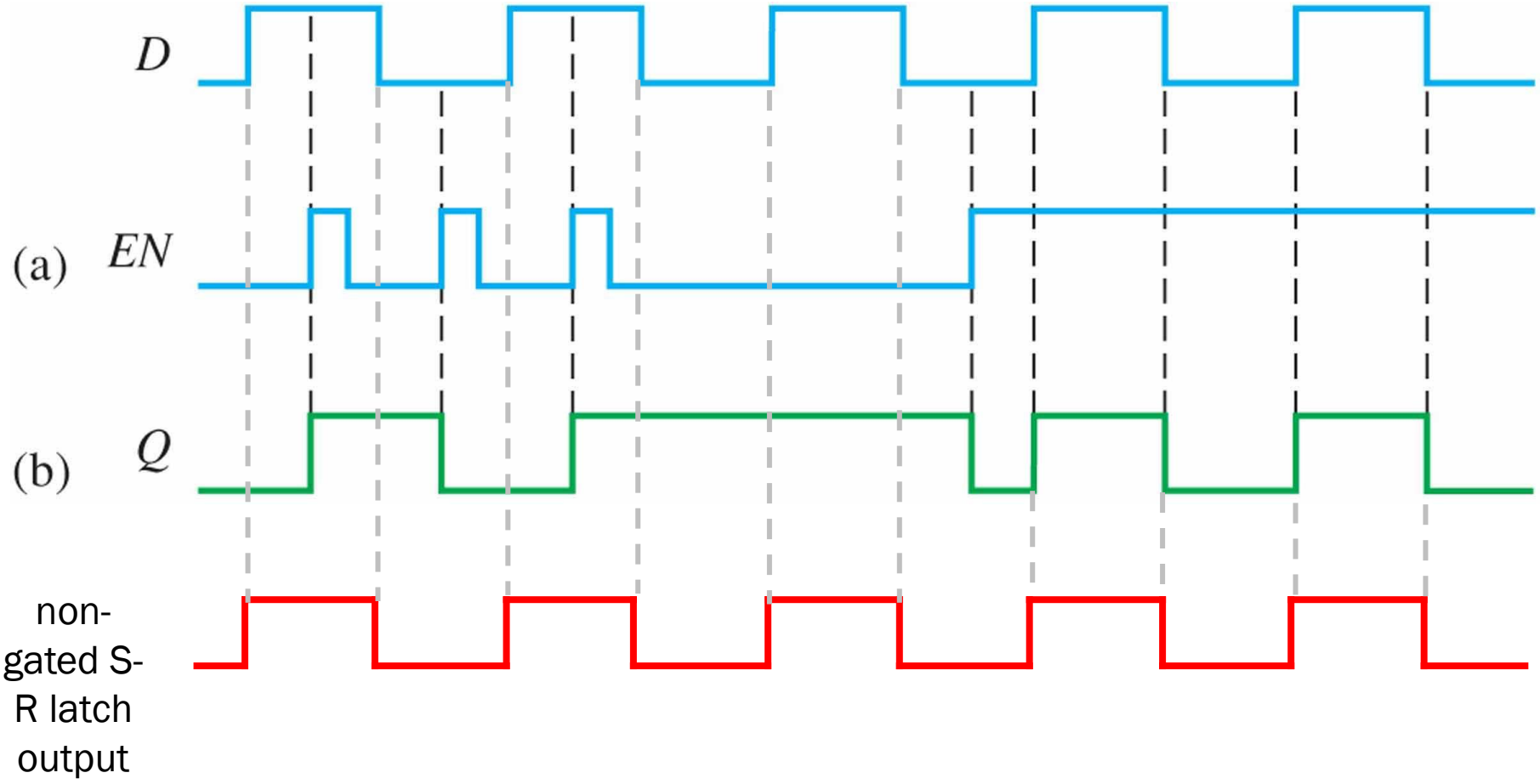
Gated D latch

- A variant of the gated latch is called the D latch
  - only has two inputs – EN for enable and D for data
  - when EN and D inputs are HIGH, the latch will set
  - when EN and D inputs are LOW, the latch will reset
  - There is no invalid condition since it is not possible to set both inputs to the latch gates to HIGH simultaneously
- A simple rule for the *D* latch is: *Q* follows *D* when the Enable is active.



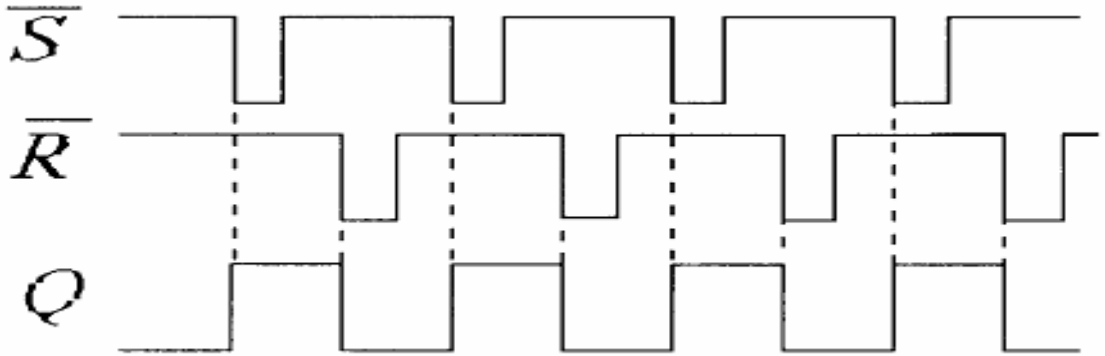


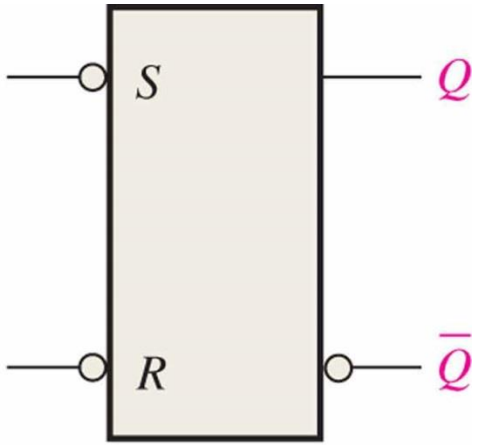
D latch timing diagram



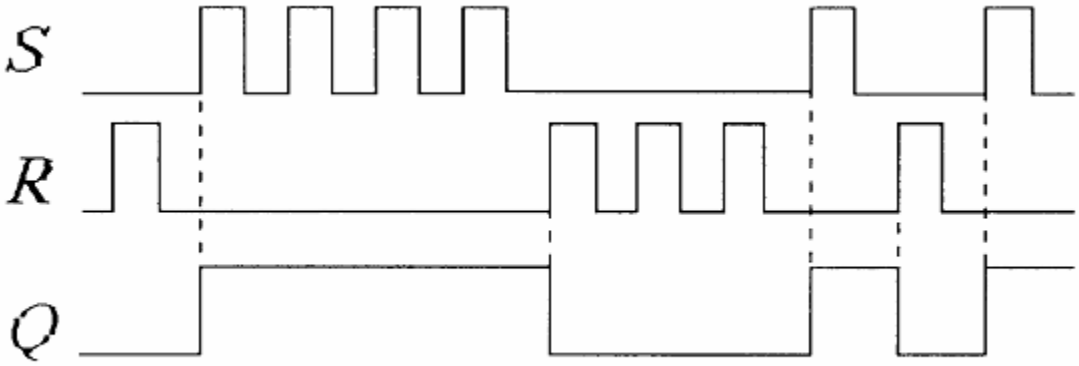
Exercise

- Draw the resulting Q output waveform of the latches below. Assume that Q state starts LOW



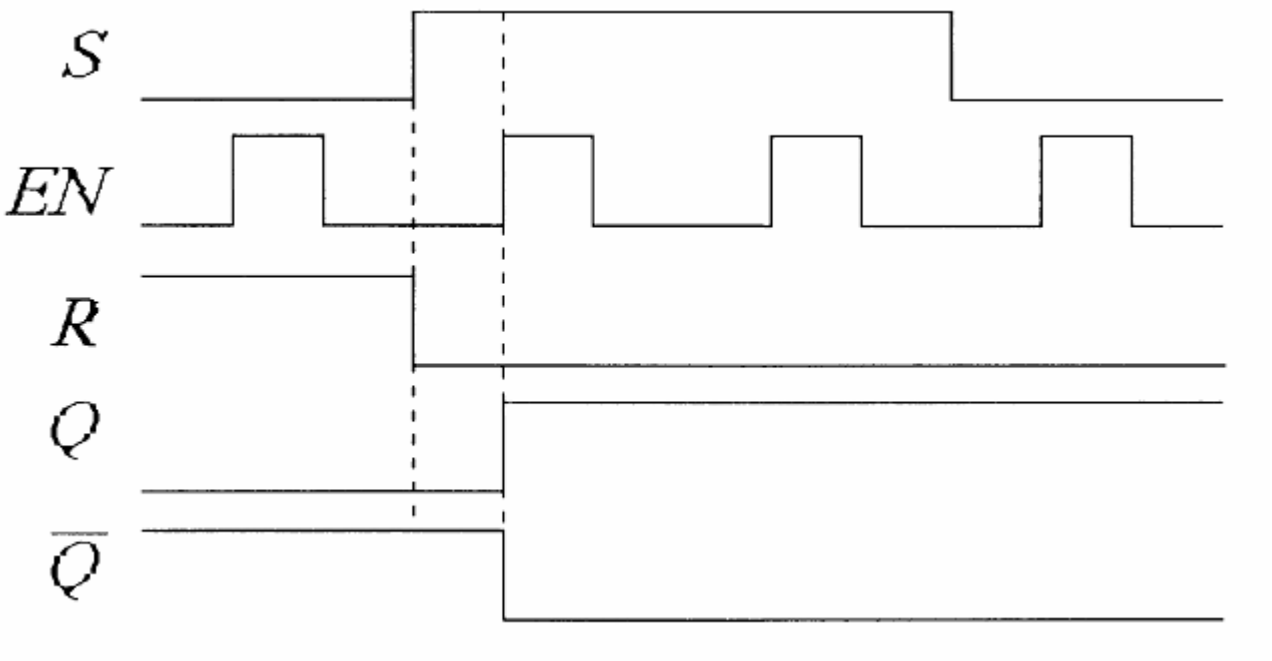


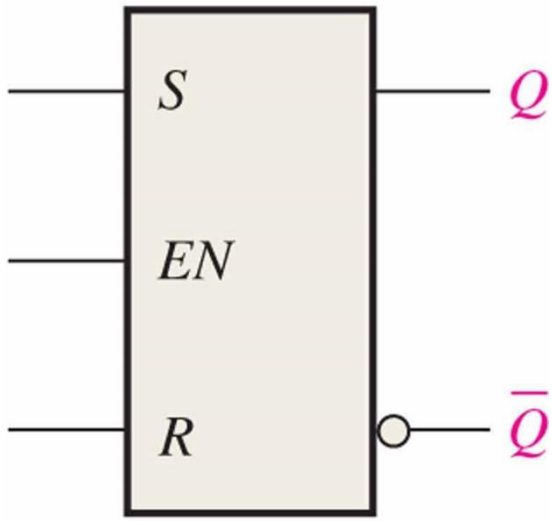
- Repeat the process with the inputs S and R below



Exercise

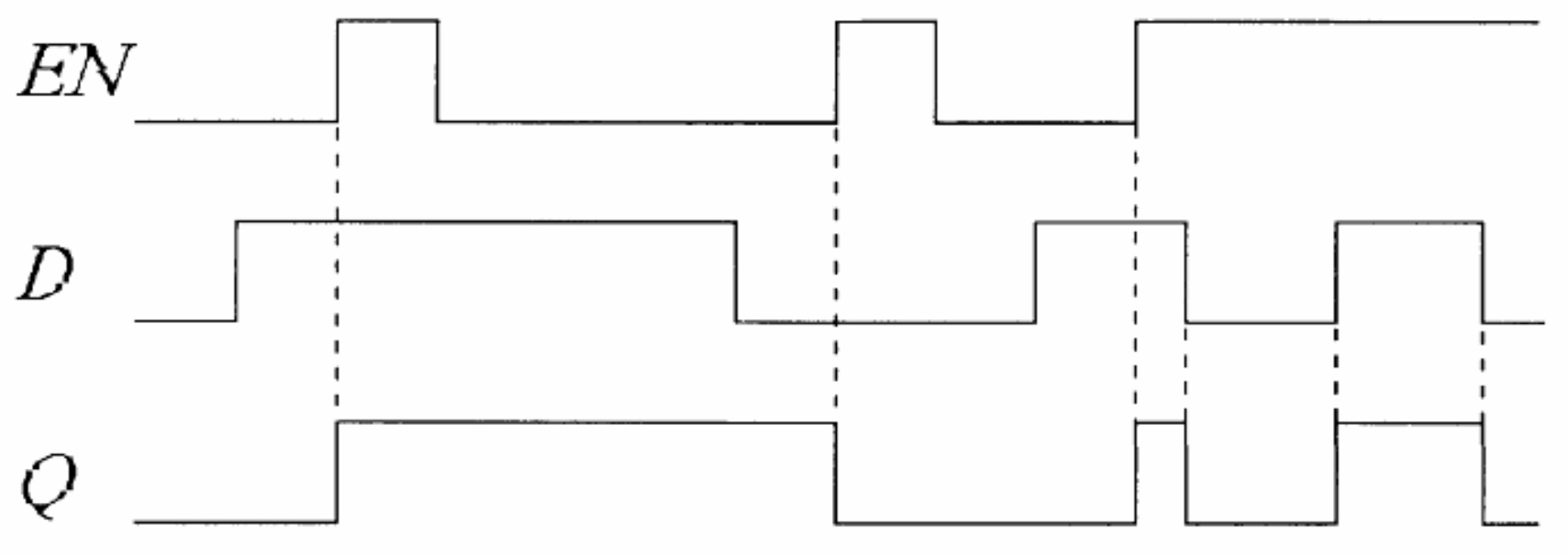
- Using the latch shown, determine outputs Q and Q' assuming that Q starts LOW





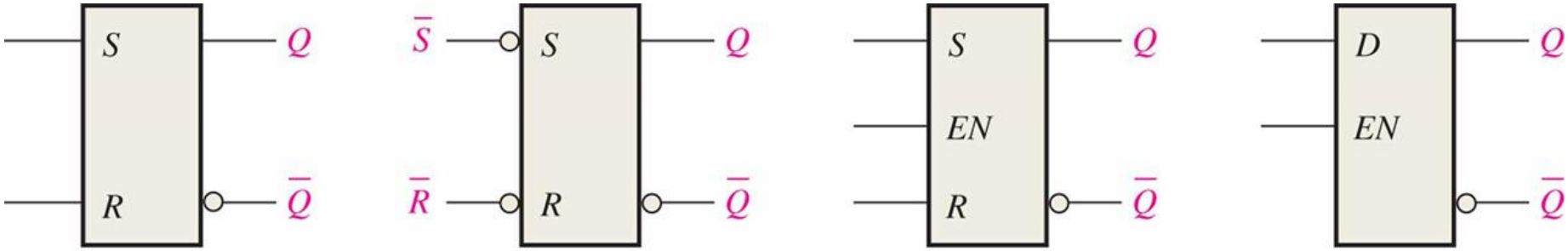
Exercise

- For a gated D latch, the waveforms below are used at the inputs D and EN. Draw the resulting timing diagram showing the output waveform you would expect to see at Q if the latch is initially RESET



Summary

- A latch forms a temporary storage device which retains its state until it is explicitly changed by its input signal (control)
- Latches can be in two states – SET and RESET
- The S-R and gated S-R latch has invalid condition
- Logic symbols for all the latches covered



(a) Active-HIGH input S-R latch

(b) Active-LOW input $\overline{S}$-$\overline{R}$ latch

(c) Gated S-R latch

(d) Gated D latch