MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER JULY/AUGUST 2024 (TERM ID: 2420)

CDS1114 – INTRODUCTION TO DIGITAL SYSTEMS

(TC1L)

10 OCTOBER 2024
9 a.m. – 11a.m.
(2 Hours)

INSTRUCTIONS TO STUDENTS

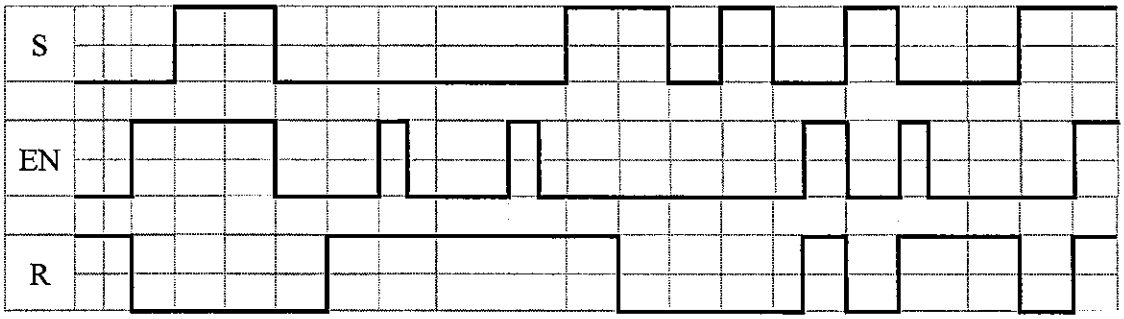
1. This Question paper consists of 5 pages excluding Cover with 4 Questions only.
2. Answer **ALL** FOUR questions. The distribution of the marks for each question is given.
3. Please write all your answers in this Question Booklet and submit this Booklet at the end of Examination.

QUESTION 1

a) Convert this equation to Standard SOP, then use K-Map to find the simplest SOP. [6 Marks]

$$\overline{a(b\bar{c} + \overline{ac})}$$

a) Determine the Q output for the gated active-high SR-latch below. Assume that Q is initially HIGH and enable is active. [4 Marks]



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QUESTION 2

a) Proof $A + \bar{A}B = A + B$ [4 Marks]

b) Based on question 2(a), construct the truth table and the resulting logic circuit simplification. [6 Marks]

c) Simplify the Boolean Expression:

$$\overline{AB + AC} + \bar{A}\bar{B}C$$

[5 Marks]

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QUESTION 3

a) Draw a circuit diagram for 3-bit asynchronous count-up counter, Q_0 for LSB, Q_2 for MSB. [3 marks]

b) Draw the timing diagram based on your answer in (a). [4.5 marks]

c) Design a synchronous counter using JK flip-flops that follows the sequence 100,010,001, 111 and repeats. The undesired states will go to 111 on the next clock pulse **EXCEPT** for 000 and 011. 000 and 011 will go to do-not-care.

i. Construct the state transition diagram for the above counter. [1.5 Marks]

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ii. Create the next state table according to the state diagram in (i) and use J-K flip-flop excitation table to define the J and K inputs for each flip-flop involved in the counter. [3 Marks]

iii. Perform K-map simplification for each flip-flop in the counter. [3 Marks]

Continued.....

QUESTIONS 4

a) Briefly explain the concept of Johnson counter. Provide an example of an application of Johnson counter. [3 Marks]

b) Design a 4-bit Johnson counter using D flip-flops. Provide the:
   i. truth table
   ii. circuit diagram
   iii. sequence of states for your design. [7 Marks]

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