MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER MARCH/APRIL 2024 (TERM ID: 2410)

CDS1114 – INTRODUCTION TO DIGITAL SYSTEMS

(All sections / Groups)

10 JULY 2024
9.00 AM – 11.00 AM
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 6 pages excluding Cover with 4 Questions only.
2. Answer **ALL** FOUR questions. The distribution of the marks for each question is given.
3. Please write all your answers in this Question Booklet and submit this Booklet at the end of Examination.

QUESTION 1

a) Convert this equation to Standard SOP, then use K-Map to find the simplest SOP. [6 Marks]

$$\overline{a(b\bar{c} + \overline{ac})}$$

b) Compute 8+9 in binary and draw the corresponding circuit with 4-bit parallel adder consisting of full-adder and half-adder. [4 Marks]

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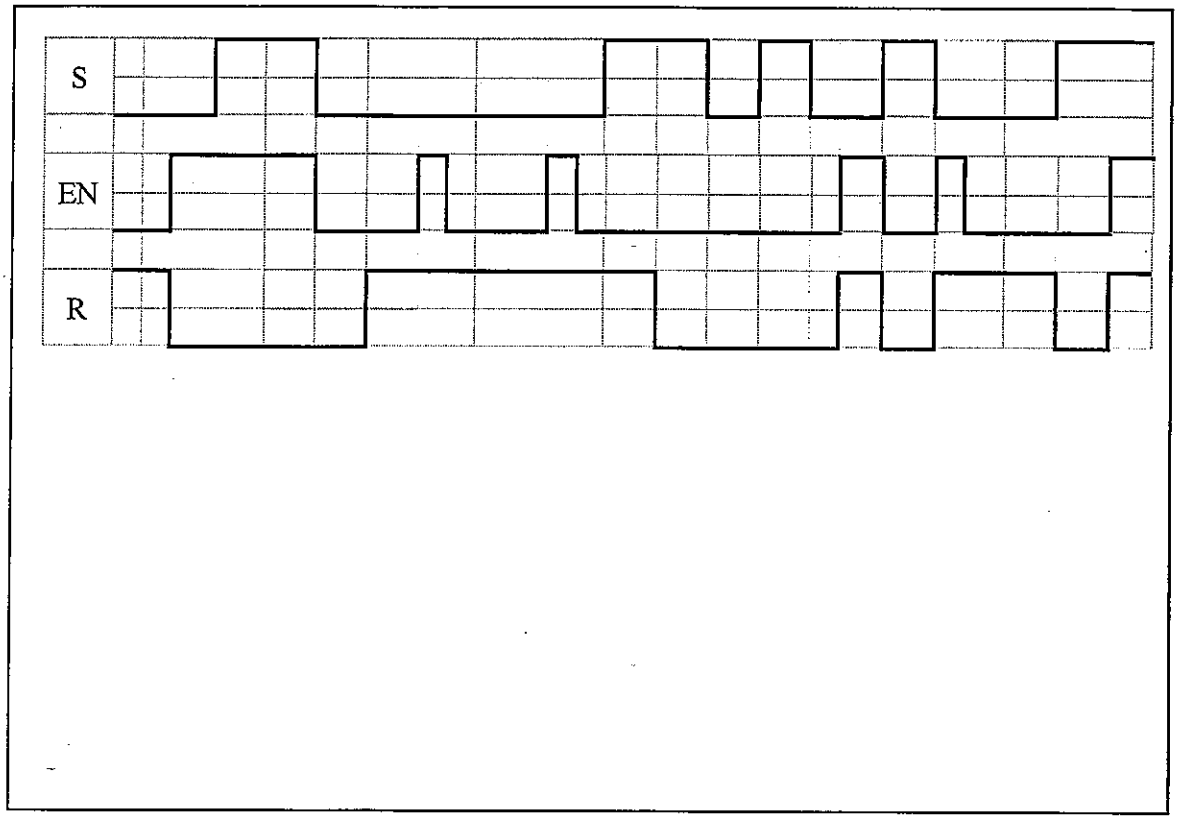
QUESTION 2

a) Determine the Q output for the gated active-high SR-latch below. Assume that Q is initially HIGH and enable is active. [4 Marks]



b) Based on the logic symbol provided in question (a), [2 Marks]

i. What is a disadvantage of the Gated active-high SR Latch?

ii. To activate the gated active-high SR Latch, what is the input needed for EN?

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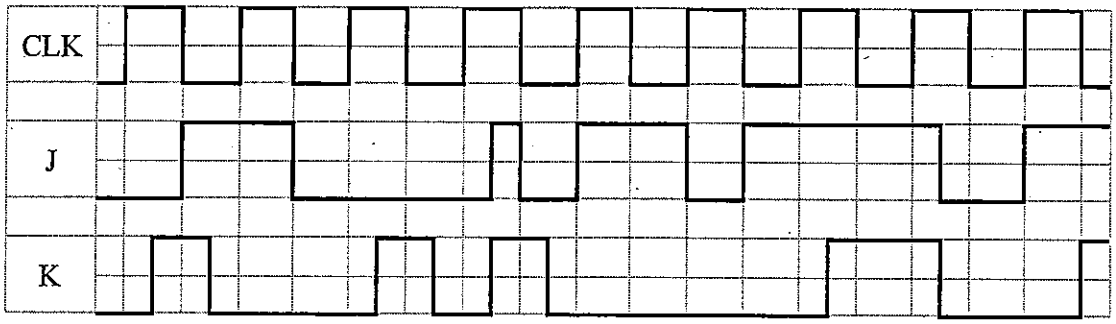
c) What is the difference between gated D latch and D flip-flop? Draw a logic symbol for both. [3 Marks]

d) For a negative edge triggered (NGT) J-K flip-flop with inputs as shown below, determine the Q output relative to the clock assuming that Q is initially HIGH. Draw a timing diagram to represent the output. Make sure you have vertical lines to show the edge triggered. [6 Marks]



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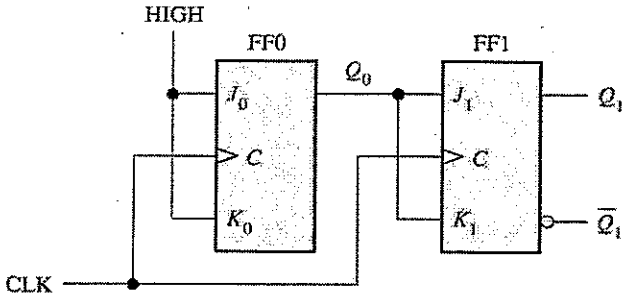
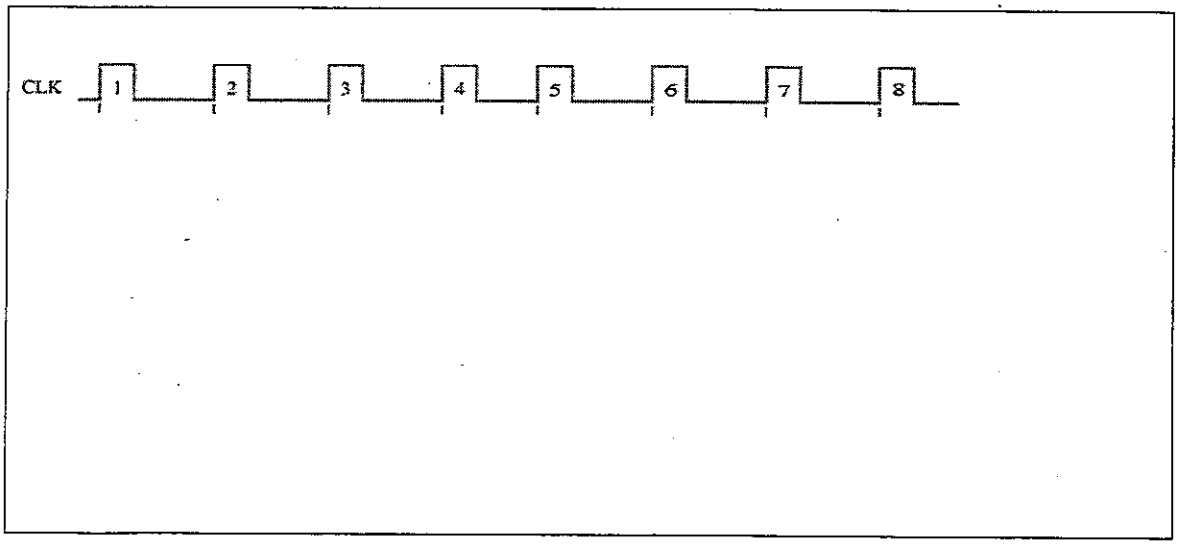
QUESTION 3

a) Construct an asynchronous clocked decade counter based on **FOUR** negative edge-triggered (NGT) JK Flip- flops and a NAND gate. [4.5 Marks]

b) For a positive edge triggered J-K flip-flop with inputs as shown below, determine the Q0 and Q1 output relative to the CLK assuming that Q0 and Q1 are initially LOW for the EIGHT clock pulses. [3 Marks]





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c) Design a synchronous counter using JK flip-flops that follows the sequence 001,011,000, 101, 010 and repeats. The undesired states will go to do-not-care stage on the next clock pulse.

i. Construct the state transition diagram for the above counter. [1.5 Marks]
ii. Create the next state table according to the state diagram in (i) and use J-K flip-flop excitation table to define the J and K inputs for each flip-flop involved in the counter. [3 Marks]
iii. Perform K-map simplification for each of the flip-flops in the counter. [3 Marks]

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QUESTION 4

a) Differentiate between a serial-in-serial-out (SISO) shift register and a parallel-in-parallel-out (PIPO) shift register. Provide examples of applications for each type. [2 Marks]

b) Design a 4-bit serial-in-parallel-out (SISO) shift register using JK flip-flops. Consider that all the stages are reset and a logical input 1011 is applied at the serial input line.

i. Provide the truth table for the shift register.
ii. Construct the circuit diagram for the shift register with JK flip-flops.
iii. Construct the timing diagram for the shift register. [8 Marks]

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