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Simple Model Based Dead Time Compensation Using Fast Current Measurement

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Abstract

Nowadays the increasing utilization of alternative energy sources demand three phase power converters capable of delivering high quality energy to the low voltage grid. Good dead time compensation hardware and software are essential to keep low order harmonics at acceptable levels even at light load conditions, at acceptable costs. Low current waveforms with multiple zero crossings within a switching period are still problematic with today's technology. Such operating conditions often happen in PWM inverters and in variable frequency drives at or below 10% load. This paper describes a new method which uses a model for calculating the voltage error caused by dead time for each phase leg. The method is completely software based, but requires fast current measurement. A model splits each half period of the triangular carrier to time segments where the slopes of the currents in all phases, and the output voltage of all semiconductor phase legs are constant. It determines the duration of each of the time segments, and integrates the volt-seconds for a half period of the triangular carrier. The model is capable of handling discontinuous conduction as well. The resulting error voltage can be used to calculate a new, compensated duty factor which can be applied to the PWM modulator. The described algorithm was tested via computer simulation. A comparison was made with other, previous methods using the same inverter model.

1. Introduction

In symmetric three phase PWM controlled voltage sourced inverters, as seen on Fig 1., the switch controller always drives both controllable switches in a phase leg to the off state for a small time interval

during switch-over to avoid shoot-through. This time is always more than what is needed for the switches to turn off for safety reasons. The remaining time is called effective dead time. It is marked with t_d in this paper.

During t_d only the anti-parallel diodes can conduct the output current. This will cause an error voltage on the output which needs to be compensated for, as recognized and described in [1]. If the dead time is long enough, discontinuous conduction may also appear. The presence of effective dead time thus introduces output waveform distortion and harmonic content in the output current of inverters. The effects become more severe at increased switching frequencies.

1.1. Existing compensation methods

The main circuit of a general three phase inverter with inductive load can be seen on Fig. 1. Most classical software based methods, such as the ones described in [1] [2] and [3] intervene based on the signum(I) function and thus are only capable of compensating for large positive or negative current waveforms. From this point of view, these methods share the same limitations, even if there are huge differences in the number of sensors used and in the methods of the calculation of error voltage or volt-seconds lost due to dead time.

Looking at the circuit diagram on Fig. 1. it can also be understood that for continuous current waveforms having zero crossings, most of the volt-seconds lost during one switch - over (which happens during positive current) are gained back during the next switch-over (during negative output current) within the same switching period. This state of operation is taken in to account in some compensation methods, like in [4].

There are methods which try to solve the problem by using extra detection hardware for each switching element as described in [5] and [6]. These are cheap compared to fast current measurement devices and fast A/D converters, but can detect the momentary current direction when a switch-over is initiated. This detection might be problematic for current waveforms having multiple zero crossings within one switching period.

1.2. Low current problems

Handling continuous current waveforms with zero crossings is not always possible using conventional methods; this already requires an accurate measurement or at least calculation of the inverter currents. The threshold between large positive or negative currents and nearly zero currents is defined by the current ripple.
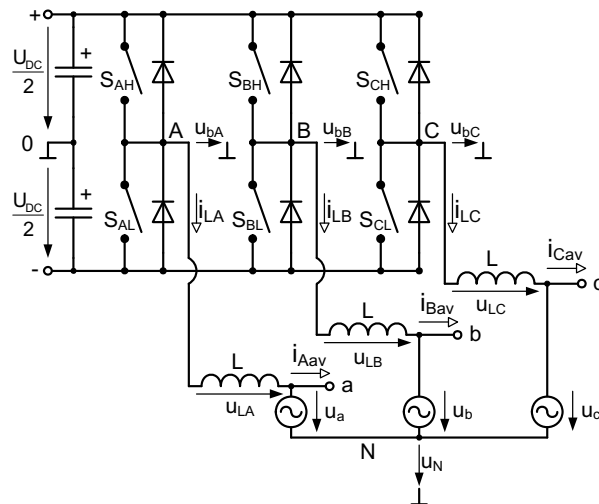

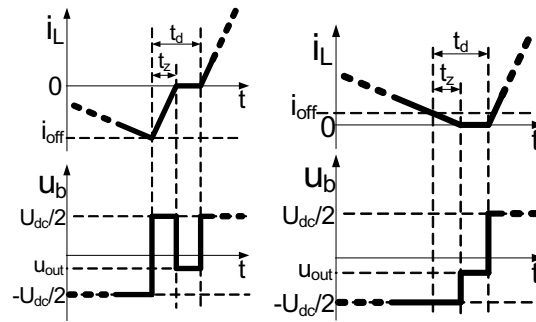Fig.1. Main circuit of a general three phase inverter.

Fig.2. Discontinuous conduction during dead time, (a) with zero crossing, and (b) without zero crossing.

The maximal current ripple can be calculated from closed formulae, as described in [11]. An attempt was made to use a new algorithm capable of calculating the actual current ripple for dead time compensation, in [12]. This way continuous currents could be handled, even if only slow current measurement is available.

More problematic current waveforms can include discontinuous conduction, as seen on Fig. 2. The error voltages caused by these were calculated from average phase current [10]. The problem is, that the complex formulae require large amount of computing power which makes such a dead time compensator expensive.

2. Model based compensation method

The basic idea behind this paper is to incorporate an accurate model into the controller which is capable of modeling low current situations and discontinuous conduction. The inputs of such a model are the instantaneous phase currents, the phase voltages, the relative slope of the triangular carrier (also marked with DIR, with values of +1 or -1), and the duty factor. The model generates the phase currents and phase leg voltage waveforms from these inputs for a half period of the triangular carrier. For that time period it also determines the resulting volt-seconds for each phase leg. A similar approach was described in D. Schröder's paper [8] for a thyristor based DC drive. A significant difference is, that for a DC drive it was relatively easy to determine the desired current waveform from the required average output current. In a three phase PWM system this is much harder, as the three phase legs affect each other through the potential of the neutral point. Because of this, the resulting voltage and current are determined instead for a given duty factor, and the intervention is done using an approximation formula.

2.1. Operation of the model

The operation of the model can be understood based on Fig. 3. The model splits each half period of the triangular carrier to time segments. Phase currents and the state of the semiconductor switches are available at the beginning of each iteration of steps 1-7; these are stored in the status vector as on Table 1. This vector is initialized on startup with the input measurement data. All initial switch states are determined by the slope of the triangular carrier (DIR) unless the duty factor is so small (or large) that the last switch-over has not been finalized. In the latter case, the phase leg is assumed as free-wheeling (state 0).

The model determines the voltages across the circuit for the actual time segment, and then it determines the length of the actual time segment (the time period for which the previously calculated voltages remain valid). When all information is available, it determines the currents and the switch states for the next iteration.

A time segment can end two ways. Either a switch-over happens, which can be detected based on the previously sorted switching sequence table (Table 2.), or one phase goes discontinuous. This decision is made

in step 5. If a switch-over happens, then the new switching state is loaded, and the switching sequence table is stepped one row further (i.e. the first row is removed).

Table 1. The status vector

time	bridge voltages			neutral voltage	inductor voltages			switch status			phase currents		
t_k	u_{bR}	u_{bS}	u_{bT}	u_N	u_{LR}	u_{LS}	u_{LT}	S_R	S_S	S_T	I_R	I_S	I_T

Table 2. The switching sequence table

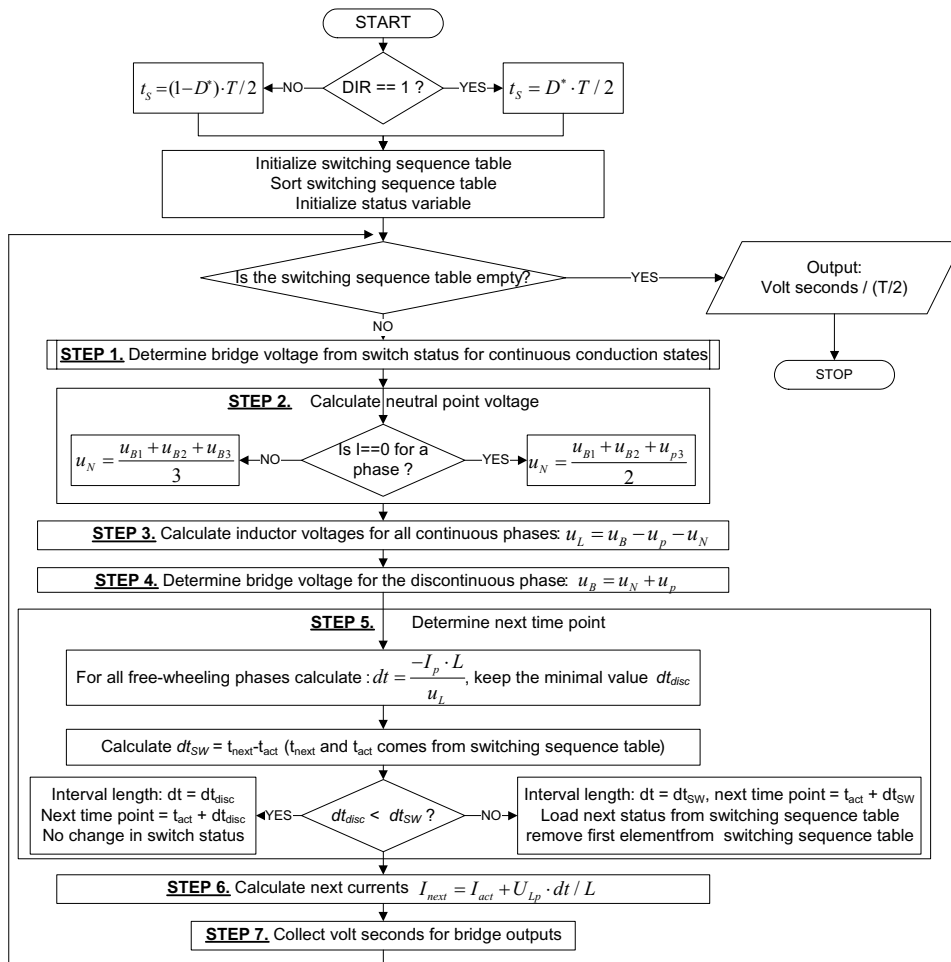| time	phase	state
t_{sR}	R	0
$t_{sR} + t_d$	R	-DIR
t_{sS}	S	0
$t_{sS} + t_d$	S	-DIR
t_{sT}	T	0
$t_{sT} + t_d$	T	-DIR
T/2	don't care	don't care

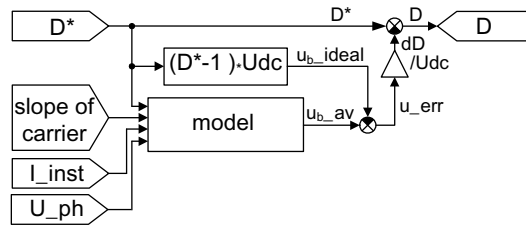Fig.3. Simplified flowchart of the model which determines the output voltage

Fig.4. Block diagram of the model based dead time compensator

The iterations are continued until the last element is cleared from the switching sequence table. A dummy element (T/2) is also added to the table, as seen on Table 2. to make sure that the output contains all volt-seconds for the corresponding half switching period. During initialization, it is made sure that this dummy element is the last in the list (i.e. all time values are smaller).

2.2. Using the model for dead time compensation

The model described in the previous section requires the following constants: switching frequency, circuit parameters, dc bus voltage, and the value of the effective dead time. The input variables are the phase voltages, the instantaneous phase currents, and the ideal duty factors (D*) which are the outputs of the current controller, and are valid for a linear (ideal) inverter. The model is run twice in every switching period: once at the upper corner of the triangular carrier, and once at the lower corner.

The compensator uses the output of the model to calculate a new duty factor, which - if applied on the inputs of the PWM generator - will result in approximately the same output voltage on the real inverter, as D* would on an ideal one. The bock diagram of this compensator can be seen on Fig. 4. It can be seen, that this method can only result in an estimation even if the model is correct, as the method on Fig. 4. gives accurate results only for the continuous cases; for discontinuous conduction this is only an approximation.

3. Simulation results

To be able to test the method, the algorithms of Fig. 3. and Fig 4. have been implemented in Matlab Simulink. It was integrated into a test system which simulates the inverter seen on Fig. 1. The controller used in the simulation uses Park transformation and PI controllers for D and Q currents. A symmetrical / space vector modulator was also used. The simulation was run with settings for 400V 50Hz three phase grid connected operation. The component values were calculated for 50A nominal peak output phase current, using an inductor of 5% nominal load impedance. In the simulation, the carrier frequency was fixed at 8kHz and the effective dead time was 3μs. Fig. 4. shows the resulting THD values at various active (wattful) loads. The THD values were calculated for the first 40 harmonics.

A linear interpolation based dead time compensator on Fig. 5a. has also been used for reference using the current ripple formula from [11]. From the results on Fig. 5a. it can be seen that the new method is generally better than the linear interpolation based method if the load is at least 7%. Inaccuracies at very low loads can come from the direct calculation in the compensator on Fig. 4. Further plans are being considered to avoid this drawback, and give good THD values down to 1% load.
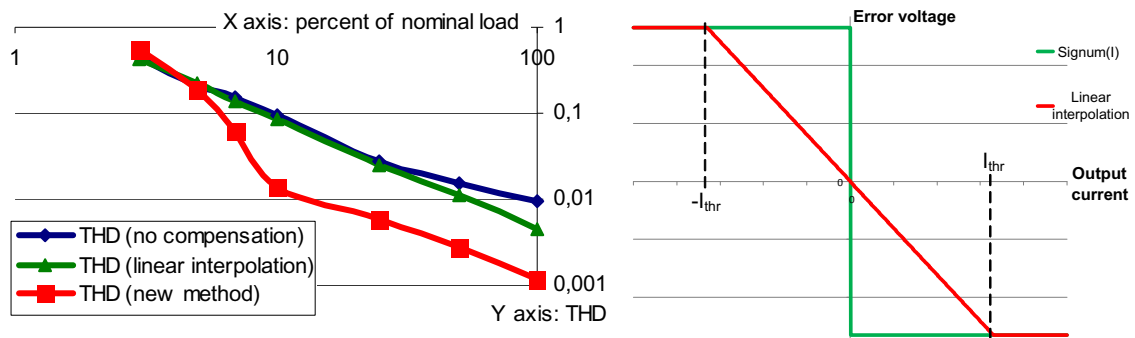
Fig.5. (a) simulation results: THD from different compensation methods, LOG-LOG scale. (b) Linear interpolation method as reference

Acknowledgements

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