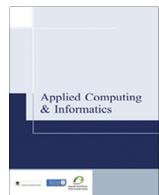




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## Original Article

# Fast routing verification with complexity effect for SOC

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## ABSTRACT

Integrated circuit (IC) fabrication technology has improved to 7 nm resulting that IC can accommodate more transistors to implement system-on-a-chip (SOC). SOC generally consists of a great quantity digital circuits with specific functions. Diverse signals not only convey inside but also communicate outside among circuits. For hundreds of thousands interlaced and complicated signals, it is an extreme big challenge to route in shrink channel. In this work, we propose a complexity effect routing algorithm based on the Lee algorithm to achieve fast verification for SOC. The advantages are to gain fast evaluated for various architectures of route, trace path from origin to destination and set diverse complexity to simulate SOC architectures. Experimental results demonstrate the achievements on five complexity sets of routing benchmarks.

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## 1. Introduction

Advance fabrication brings the inclusion of *system-on-a-chip* (SOC) that coexist processor and all the necessary components. As follow the latest technology of semiconductors nanometer process, the length of transistors is designed inside SOC that improves capacity, performance and reliability. At the same time, more and more circuit modules are integrated into SOC resulting in routing through all modules and becomes a lot much difficult.

## 2. SOC routing

Routing technique is continuously studied in designing SOC. In pre-SOC stage, Farooq et al. [1] presented a novel exploration flow with optimized inter-FPGA routing on multi-FPGA platform. Also, Kan et al. [2] addressed RAS validation on NoC routing issue. As intellectual property (IP) core SOC, El-Naggar et al. [3] adopted *network on chip* (NoC) to route among IP blocks and proposed *universal verification methodology* (UVM) to verify design. In post-routing stage, Tsai et al. [4] presented DVI-X algorithm with consideration of single via and redundant-via candidates of chips. Moreover, Fan [5] implemented a routing tool based on line-probe routing

algorithm. In *internet-of-things* (IoT) network, Fan [6] presented that clique-first adaptive routes approach had gained high performance. Additionally, he pointed power saving to demonstrate a routing-aware approach in [7]. Other routing algorithms addressed in [8]. Moreover, Xu et al. [9] solved the maze routing problem in the routing stage by redundant-via insertion method. On the other hand, Lembach et al. [10] focused on high quality routing to physical design. In Manhattan path research, Zhao et al. [11] paid more attention to a path-counter method with low time complexity to fault-tolerant minimal paths. The proposed approach can apply to arbitrary fault distribution. Also, the existing paths can be checked and the fault blocks effect does not affect available nodes. For dedicated routing and XY routing issue, Agrawal et al. [12] presented two algorithm to solve the test-delivery and dynamic programming problems. The proposed method was separately tested by 1000 and 1600 cores experiments for test scheduling of power constraints. Ren et al. [13] also adopted two-phase routing algorithm for routing on-chip traffic problems. The effectiveness of the proposed method was tested by extensive experiments, and was compared with previous algorithms.

## 3. Complexity effect routing

Advance nano-process integrated circuit technology produces an extreme tiny transistor to achieve lighter and faster products. Minimized transistors expand capacity to accommodate more and more digital circuits but shrink the path among elements. Moreover, the area of chip is either the same or smaller than previous products. In other words, new technology makes the design

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chip becoming more difficult resulting from tiny transistor, more circuits and narrow paths. Besides, within same area which places more circuits result in the usable communicating path are greatly decreased. As a modern chip with more and more circuits but less and less usable path, nano-process technology obviously brings a new challenge on exacerbating routing problem.

#### 4. Complexity effect routing algorithm

In this paper, we present a *complexity effect routing algorithm* (CERA) based on the Lee algorithm [8] with the aim of fast routing verification with visual stepping propagation, graphical trace and retrace and the shortest path. The Lee algorithm adopts breadth-first search to communicate from origin to destination. It routes on either horizontal or vertical direction on grid plane. A well-known routing technology, Manhattan routing, also obeys horizontal or vertical way which is the de facto routing standard in chip [14]. On the other hand, the Lee algorithm has three advantages. One is visual stepping propagation from origin to target. Another is from destination to source or vice versa to graphical trace or retrace. The other is the shortest path for link if the route exists. Despite Lee's algorithm was proposed in 1991, its route approach corresponded to cross section which was as same as some commercial tools such as Laker of Synopsys [15] or Virtuoso of Cadence [16]. Both academic research and commercial company notice that the route of chip will be more and more complex and complicated in the future. Therefore, the CERA adds the complex effect to route so as to observe the effect of block circuits. Specifically, it is combined complexity into Lee algorithm to gain the complex routing effects with the function of visual examination, graphical trace and shortest path in chip designs. Those features make CERA valuable in comparison to commercial CAD tools.

On the basis of aforementioned explanations, the routing problem of SOC is defined as follows. For a SOC design in grid plane, the number of cross points of chip for Manhattan plane is defined in the following

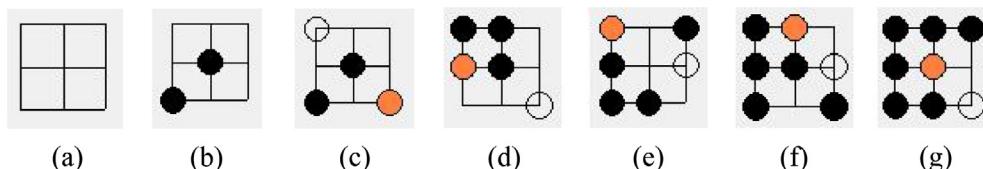
$$P(i,j) = i \times j \quad (1)$$

where  $i$  is the number of lines in  $x$ -axis and  $j$  is the number of lines in  $y$ -axis.

**Fig. 1** illustrates the Manhattan plane on blocking route between source and destination. **Fig. 1(a)** shows the Manhattan plane with  $3 \times 3$  cross point and **Fig. 1(b)** displays two obstacles in Manhattan plane. The obstacles may be irrelevant circuits which must be isolated from source and destination to avoid short circuit. Therefore, the link between origin and target must bypass obstacles. Otherwise, the SOC design works incorrectly caused by short circuits. **Fig. 1(c)** shows the source and destination using two obstacles in Manhattan plane. Based on **Fig. 1(c)**, the number of usable points for link between source and destination can be derived as follow

$$U(i,j) = P(i,j) - \sum o - k \quad (2)$$

where  $o$  is the obstacle and  $k$  represents the number of points of source and destination.



**Fig. 1.** (a) Manhattan plane. (b) Two obstacles. (c) Source and destination and two obstacle. (d) Three obstacles. (e) Four obstacles. (f) Five obstacles. (g) Six obstacles.

From **Fig. 1(d)** to **(g)** are the more obstacles result the less path to link from source to destination. One key factor of successful route depends on the number of obstacles. Therefore, we define the ratio of  $P$  and  $U$  as complex effect in the following

$$C(P, U) = \frac{(P - U) - k}{P} \times 100\% \quad (3)$$

where  $P$  is the number of cross points,  $U$  is the number of usable points and  $k$  is the number of points for source and destination.

After placing the obstacles and determine location of source and destination, the route can only walk on the vacant points rather than move to the blocks. Consequently, those vacant points form a set of class  $V$ , which is defined in the following

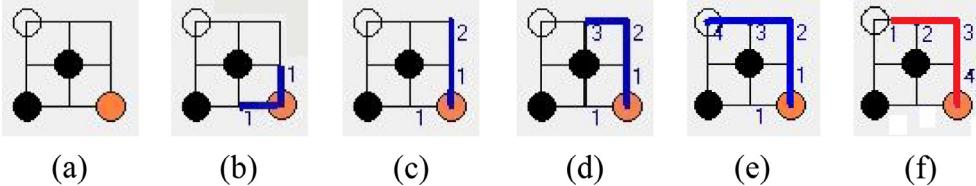
$$V = \{v_1, v_2, v_3, \dots, v_u\} \quad (4)$$

where  $v_1, v_2, v_3, \dots, v_u$  are vacant points of XY coordination, subscript  $u$  is the number of  $U$ .

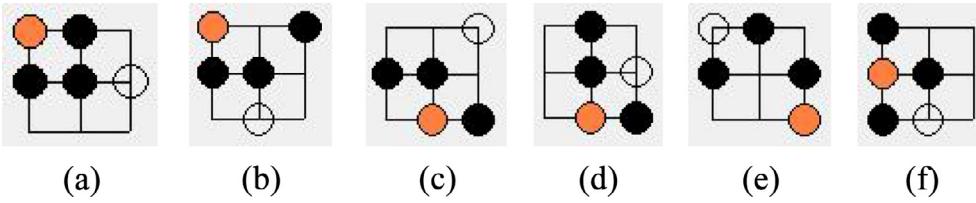
**Fig. 2** exhibits the procedures of the CERA approach and the three advantages, which are visual stepping propagation, graphical retrace and the shortest path. **Fig. 2(a)** displays the complexity as 22% based on Eq. (3) for a given routing plane. The first stepping propagation departs from orange point to west and north as shown in **Fig. 2(b)**. On mark 1 as location west of orange point, there is no path with other neighbours. Therefore, the other mark 1 as location north of orange point steps one from source. **Fig. 2(c)** shows the route direction to north due to the only one vacant in north. Similarly, the way for **Fig. 2(d)** and (e) are as same as **Fig. 2(c)**. Only one vacancy locates at west so that walks to left to arrive destination that is shown in **Fig. 2(e)**. Finally, the retrace route from destination to source is exhibited in **Fig. 2(f)**. Those procedures demonstrate a significant characteristic, that is, a link will be connected if the path exists. As a result, it is valuable for high complexity routes of SOC. On the other hand, six different inherent unconnected routing cases are exhibited in **Fig. 3**. In summary, the link is unconnected while no path passes from source to destination.

**Fig. 4** presents the *complexity effect routing algorithm* (CERA) for SOC. For a given source point  $s$ , destination point  $d$  and the number of complex effect  $C$ . The proposed CERA discovers its neighbours of source  $s$  (line 5). For each neighbour  $s_x$  of  $s$  (line 6), it travels to neighbour as  $s_y$  for each  $s_x$  (line 7). In case of  $s_y$  meets obstacle, it changes to another direction (line 8). Otherwise, the  $s_y$  goes to next stop and save  $s_y$  information to vacant class (line 9). If the  $s_y$  arrives  $d$ , the route exists (line 10) and then retraces from destination to source (line 13). In the contrary, if the vacant class does not be set, no path links from source to destination. On the basis of aforementioned explanations, the time complexity of CERA is  $O(mn)$  where  $m$  is the number of lines in  $x$ -axis and  $n$  is the number of lines in  $y$ -axis.

**Fig. 5** exhibits one of SOC designs with the complexity effect as 10, 35 and 60 in the  $20 \times 20$  grids individually. The difference is the number of obstacles among **Fig. 5(a), (b)** and (c) that is calculated by Eq. (3). Those obstacles are randomly generated by the proposed method. By randomly generating benchmarks, we can fast simulate diverse SOC and then discover the route. For example, the CERA can fast generate another SOC with complex effect from



**Fig. 2.** (a) Given routing plane. (b) Visual first stepping propagation. (c) Visual second stepping propagation. (d) Visual third stepping propagation. (e) Visual 4th stepping propagation. (f) Graphical retrace and the shortest path.



**Fig. 3.** Six different inherent unconnected routing cases.

```

Algorithm: Complexity effect routing algorithm ( $s, d, C, R$ )
Input: source point  $s$ , destination point  $d$ , the number of complexity  $C$ 
Output: route from source to destination point  $R$ 
begin
1:  $s$  = randomly generated location in XY coordination;
2:  $d$  = randomly generated location in XY coordination;
3:  $C$  = randomly generated the number of complexity of obstacles;
4: path=false;
5: while  $s$  have neighboring do
6:   for each neighboring  $s_x$  in  $s$ 
7:     for each neighboring  $s_y$  in  $s_x$ 
8:       if  $s_y$  of XY route  $\notin U$ 
9:         save  $s_y$  route to vacant class  $V$ ;
10:        if  $s_y$  of XY route =  $d$  then
11:           $R$ =True;
12:        exit while;
13: if  $R$ =True then RETRACE from  $d$  to  $s$ ;
14: else  $R$  does not exist;
end

```

**Fig. 4.** Complexity effect routing algorithm.

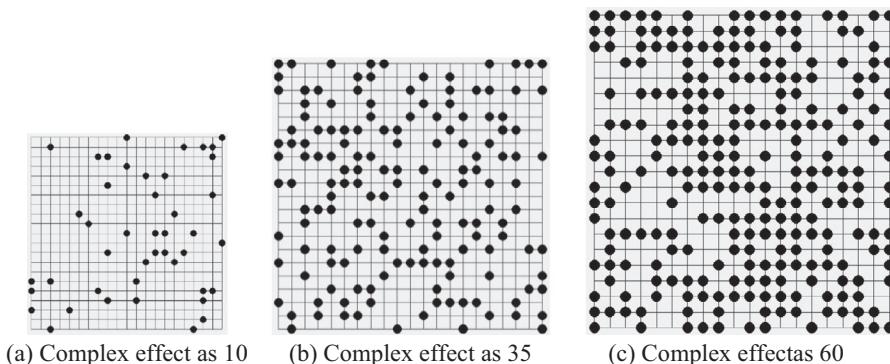
10 to 60 that is displayed in Fig. 6. Therefore, the CERA can rapidly serve a set of placement prototyping for designers. This study contributes not only fast generation but also rapid verification which is corresponding to route for both even more benchmarks. In comparison with complex effect from 10 to 60, higher complexity obviously results in the less paths from origin to destination. Although the complex effect exacerbates the route, the CERA can discover

any existed links between source and destination no matter how the complex effect is set. In addition, the route is the shortest path that implies the fast execution time to be achieved.

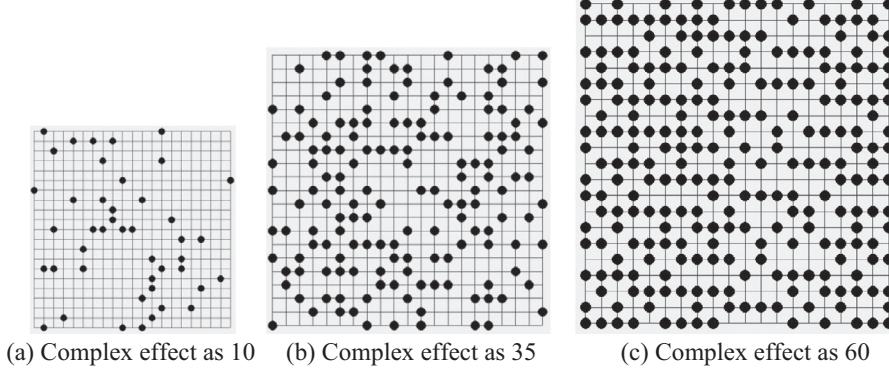
## 5. Simulations

Fig. 7(a) to (c) separately demonstrates three SOC architectures with a successfully completed route where the complexity is individually set as 20, 40 and 50 in the  $20 \times 20$  grids. A successfully completed route indicates that has a path from a start point to an end point. In contrast, there are no paths to communicate from origin to destination. The successful recursive route detects paths around an origin point. Label “1” is used to point one distance from source. It is called one step. Next, the CERA departs from source to label “1” and then find a possible vacancy around itself and run to next stop. These steps form wave propagation from source to destination. From the viewpoint of the distance of route, Fig. 7(a), (b) and (c) are separately cost 15, 37 and 24 steps from origin and destination. On the other hand, Fig. 7(d) shows the CERA stops stepping at label “1” in north and label “2” in south. Besides, the CERA stops stepping at label “4” in southeast and label “8” in northwest due to no paths.

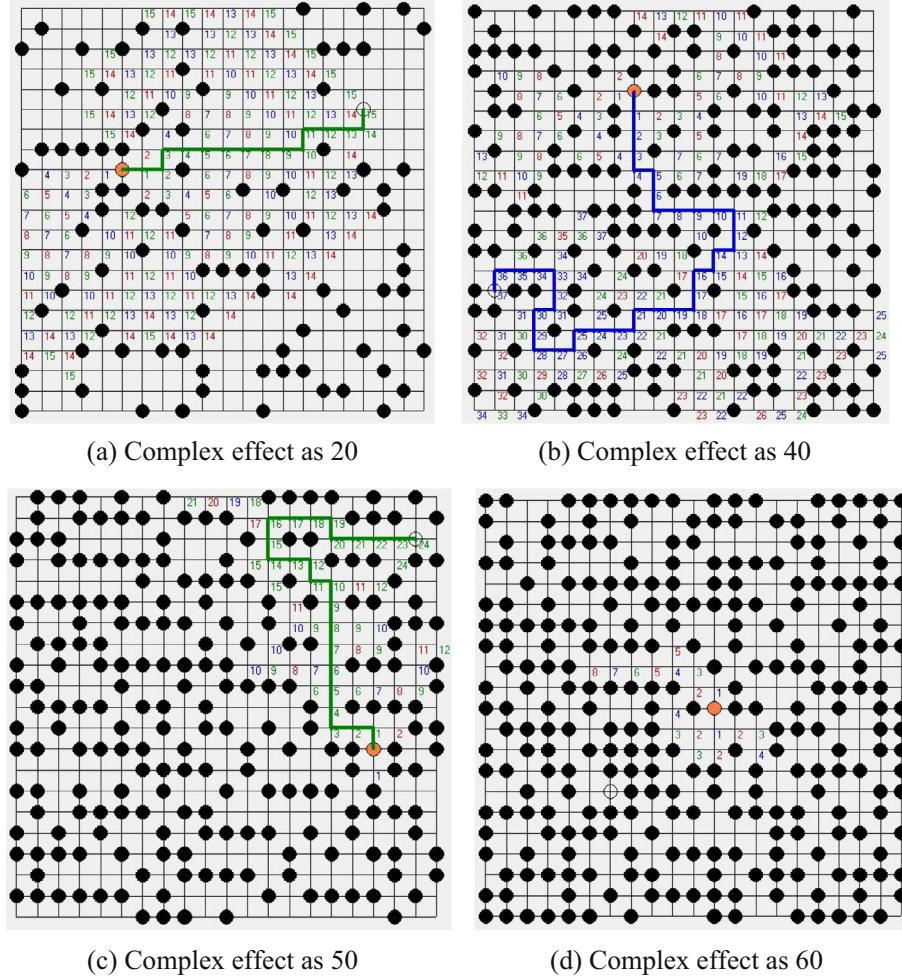
Table 1 shows that the experimental results of the CERA method with complex effect set as 20, 30, 40, 50 and 60 in the  $20 \times 20$  grids. Each set consists of 30 test benchmarks named c1, c2, c3 to c30. Each benchmark simulates a SOC with various obstacles from origin to destination. Those obstacles are randomly gen-



**Fig. 5.** Random generation SOC layouts with complex effect from 10 to 60.



**Fig. 6.** Arbitrary generation SOC layouts with complex effect from 10 to 60.



**Fig. 7.** Fast routing verification with complex effect from 10 to 60 in  $20 \times 20$  grids.

erated by the CERA. Due to the blocking locations cannot be predicted, the ability of the CERA can be effectively measured. Label “Y” represents that the CERA completes route from source to destination. In the contrary, label “–” denotes unconnected from origin to target. The “Avg” column shows that the ratio is 100%, 86.7%, 76.6%, 43.3% and 20% which obviously demonstrates a decreased trend due to available paths are less and less.

Table 2 shows the stepping propagation of experimental results. First, in the Complex set 20, each benchmark is successfully completed and routed via various steps. In the Complex set 30, the

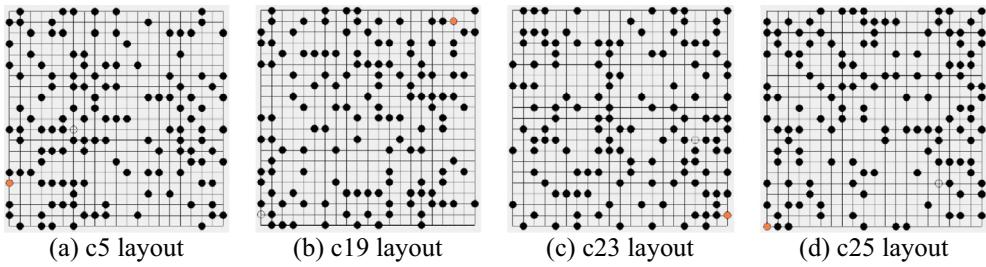
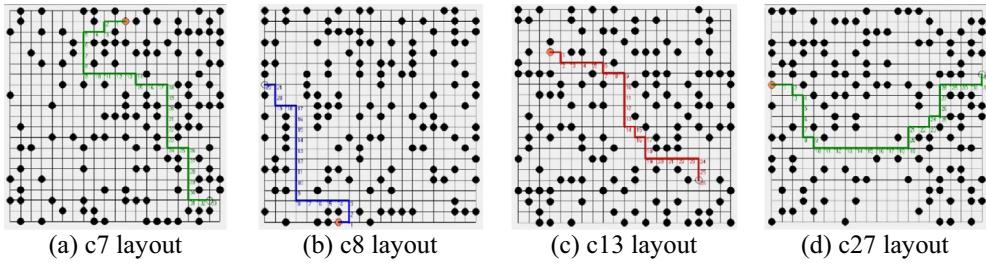
benchmarks of c5, c19, c23 and c25 are unable to link from source to destination because there are no paths. Their layouts are shown in Fig. 8. On the other hand, other benchmarks such as c7, c8, c13 and c27 successfully depart from source to destination that is demonstrated in Fig. 9. Thirdly, in the Complex set 40, there are no any paths in c1, c3, c4, c5, c13, c14 and c15 which are partly shown in Fig. 10. In the contrast, there are 23 benchmarks with completed route such as c2, c8, c20 and c26 that are illustrated in Fig. 11. For the Complex set 50, more spaces are used to place digital circuit and cause that the usable paths are decreased. Thus,

**Table 1**Fast routing verification of CERA for  $20 \times 20$  grids.

Benchmarks	Complex effect					Benchmarks	Complex effect					Benchmarks	Complex effect					Avg. (%)
	20	30	40	50	60		20	30	40	50	60		20	30	40	50	60	
c1	Y	Y	–	Y	–	c11	Y	Y	Y	Y	–	c21	Y	Y	Y	Y	–	–
c2	Y	Y	Y	–	–	c12	Y	Y	Y	Y	–	c22	Y	Y	Y	–	–	–
c3	Y	Y	–	–	–	c13	Y	Y	–	Y	–	c23	Y	–	Y	–	–	–
c4	Y	Y	–	–	–	c14	Y	Y	–	Y	–	c24	Y	Y	Y	–	Y	–
c5	Y	–	–	–	–	c15	Y	Y	–	–	–	c25	Y	–	Y	–	–	–
c6	Y	Y	Y	–	Y	c16	Y	Y	Y	Y	Y	c26	Y	Y	Y	–	–	–
c7	Y	Y	Y	Y	–	c17	Y	Y	Y	Y	–	c27	Y	Y	Y	–	Y	–
c8	Y	Y	Y	Y	Y	c18	Y	Y	Y	Y	–	c28	Y	Y	Y	–	–	–
c9	Y	Y	Y	Y	–	c19	Y	–	Y	–	–	c29	Y	Y	Y	–	–	–
c10	Y	Y	Y	Y	–	c20	Y	Y	–	Y	–	c30	Y	Y	Y	Y	–	–
Ratio (%)	100	90	60	50	20		100	90	70	70	20		100	80	100	10	20	100
																		86.7 76.6 43.3 20
																		20

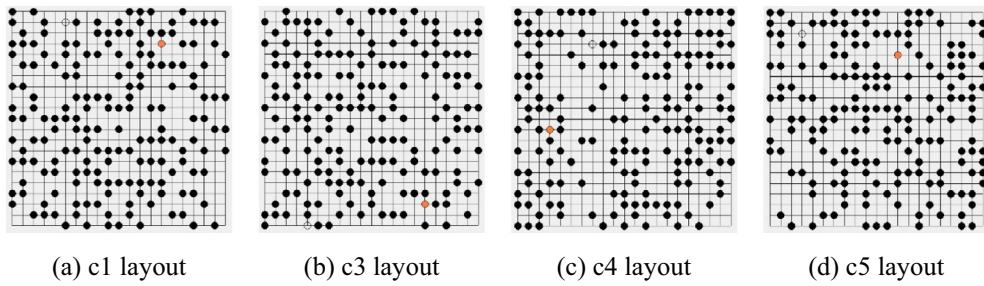
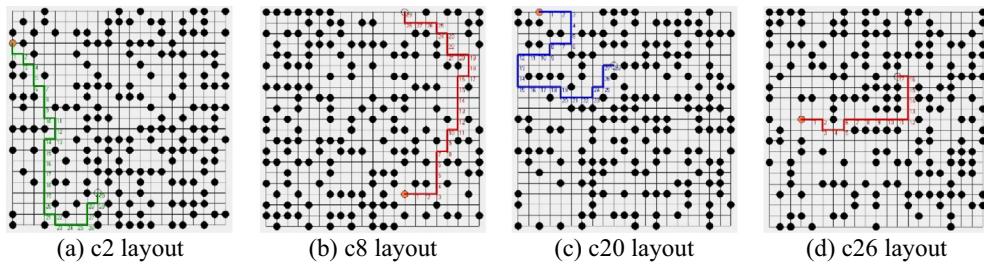
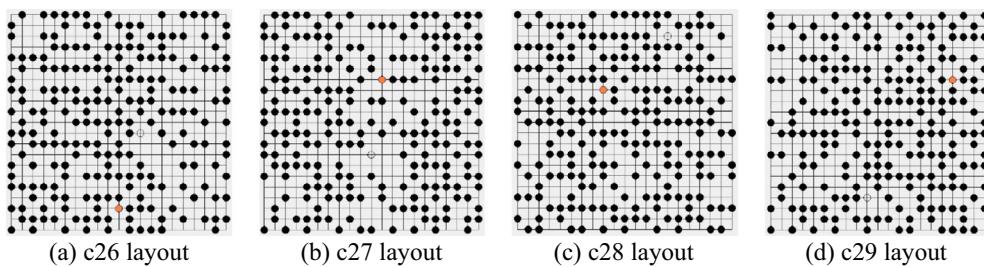
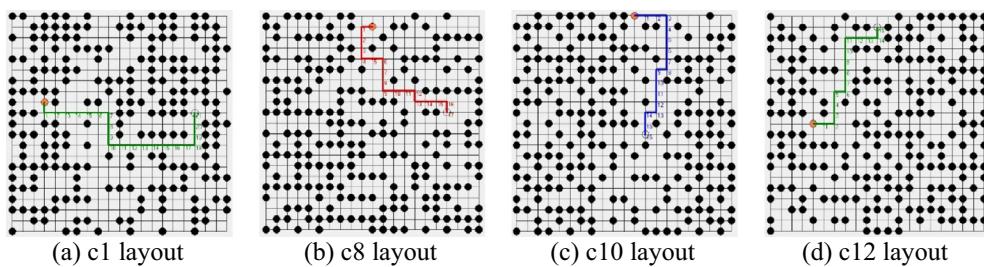
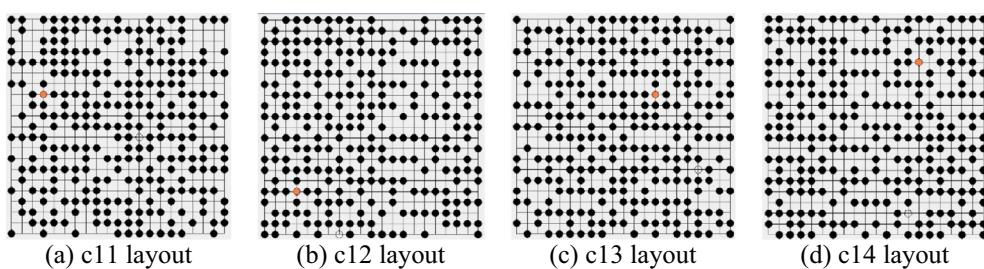
**Table 2**Stepping propagation of CERA for  $20 \times 20$  grids.

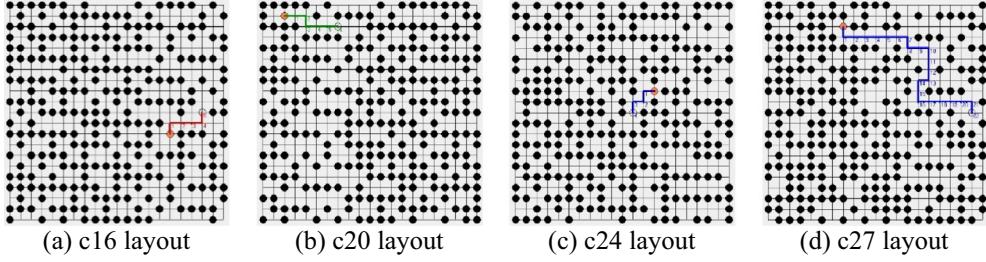
Benchmarks	Complex effect					Benchmarks	Complex effect					Benchmarks	Complex effect					Avg. (%)
	20	30	40	50	60		20	30	40	50	60		20	30	40	50	60	
c1	23	17	–	21	–	c11	13	21	30	11	–	c21	29	26	8	13	–	–
c2	18	15	20	–	–	c12	24	29	12	15	–	c22	19	16	29	–	–	–
c3	18	20	–	–	–	c13	12	26	–	13	–	c23	29	–	13	–	–	–
c4	19	14	–	–	–	c14	11	21	–	15	–	c24	8	22	13	–	4	–
c5	23	–	–	–	–	c15	18	18	–	–	–	c25	21	–	14	–	–	–
c6	8	21	5	–	3	c16	9	33	17	8	5	c26	5	17	28	–	–	–
c7	13	33	16	14	–	c17	12	15	12	15	–	c27	23	33	16	–	22	–
c8	8	22	30	17	2	c18	10	25	18	18	–	c28	24	7	17	–	–	–
c9	13	13	15	4	–	c19	18	–	14	–	–	c29	15	27	22	–	–	–
c10	6	5	17	16	–	c20	11	10	29	–	6	c30	11	9	9	15	–	–

Fig. 8. CERA results of no path in complex effect 30 for  $20 \times 20$  grids.Fig. 9. CERA results in complex effect 30 for  $20 \times 20$  grids.

the number of cases with no paths has 17 designs that is partially demonstrated in Fig. 12. Conversely, Fig. 13 illustrates 4 of the 13 routing completion designs. Finally, in the Complex set 60, the routing results with completion and incompleteness are partly displayed in Figs. 14 and 15 respectively.

In order to simulate the route of advance IC fabrication, the number of grids is set to  $40 \times 40$  grids to accommodate more modules in SOC. Table 3 displays the experimental results for five kinds of complex sets in  $40 \times 40$  grids. Each set consists of 30 benchmarks named c31, c32, c33 to c60. Each benchmark randomly gen-

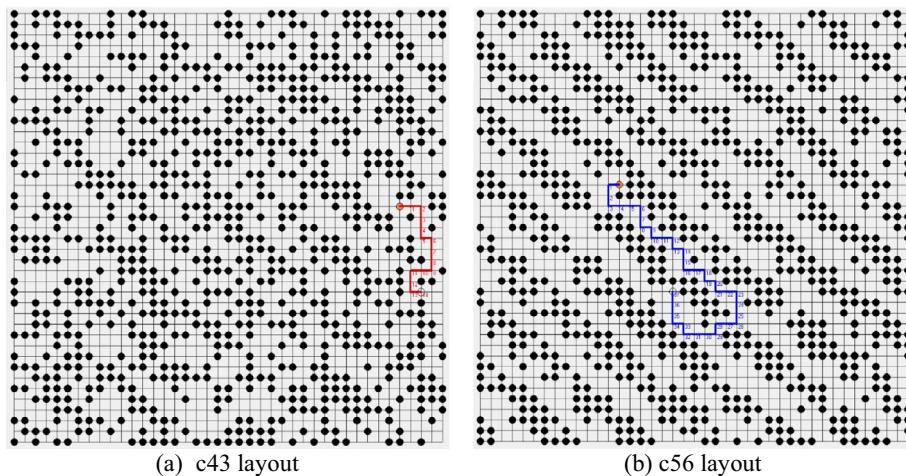
Fig. 10. CERA results of no path in complex effect 40 for  $20 \times 20$  grids.Fig. 11. CERA results in complex effect 40 for  $20 \times 20$  grids.Fig. 12. CERA results of no path in complex effect 50 for  $20 \times 20$  grids.Fig. 13. CERA results in complex effect 50 for  $20 \times 20$  grids.Fig. 14. CERA results of no path in complex effect 60 for  $20 \times 20$  grids.

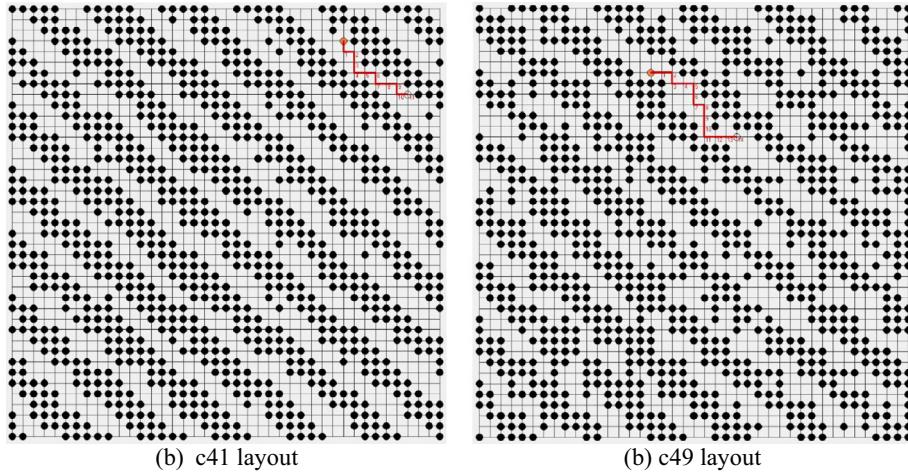
Fig. 15. CERA results in complex effect 60 for  $20 \times 20$  grids.**Table 3**Fast routing verification of CERA for  $40 \times 40$  grids.

Benchmarks	Complex effect					Benchmarks	Complex effect					Benchmarks	Complex effect					Avg.
	20	30	40	50	60		20	30	40	50	60		20	30	40	50	60	
c31	Y	Y	Y	–	–	c41	Y	Y	Y	–	Y	c51	Y	Y	Y	Y	–	–
c32	Y	Y	–	–	–	c42	Y	Y	Y	Y	–	c52	Y	Y	–	–	–	–
c33	Y	–	–	–	–	c43	Y	Y	–	Y	–	c53	Y	Y	–	Y	Y	–
c34	Y	Y	–	–	–	c44	Y	Y	–	Y	–	c54	Y	Y	Y	–	–	–
c35	Y	Y	–	–	–	c45	Y	Y	–	–	–	c55	Y	Y	–	–	–	–
c36	Y	Y	Y	–	–	c46	Y	Y	Y	–	–	c56	Y	Y	–	Y	–	–
c37	Y	Y	Y	–	–	c47	Y	–	–	–	–	c57	Y	Y	–	–	Y	–
c38	Y	–	Y	–	–	c48	Y	Y	–	Y	–	c58	Y	Y	–	–	–	–
c39	Y	Y	Y	–	–	c49	Y	Y	Y	–	Y	c59	Y	Y	Y	–	–	–
c40	Y	Y	Y	–	–	c50	Y	Y	–	–	–	c60	Y	Y	–	Y	–	–
Ratio (%)	100	80	60	0	0		100	90	40	40	20		100	100	30	40	20	100 90 43.3 40 26.7 13.3

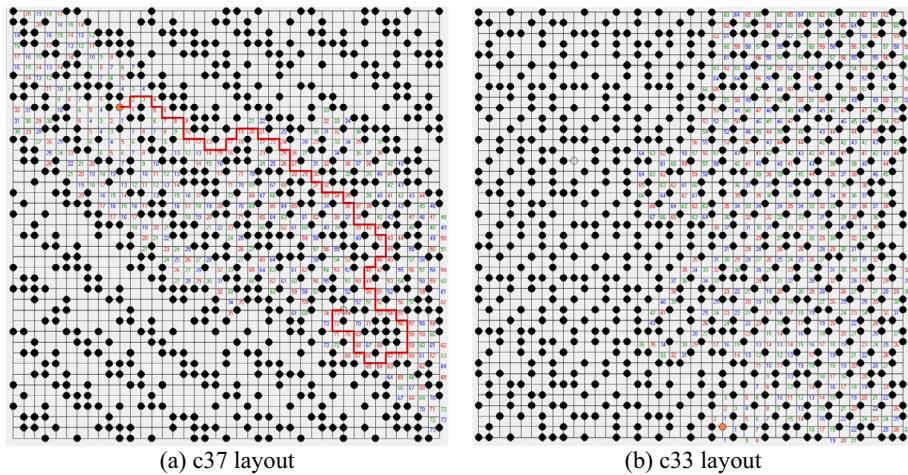
erates a set of obstacles which depends on the complex effect. First, in the Complex set 20, all benchmarks have successfully completed routing by CERA method. In the Complex set 30, c33, c38 and c47 are routed incompletely unless circuit placement is adjusted. Thirdly, in the Complex set 40, the routing completion and incompleteness is separately 13 and 17 designs. In the Complex set 50, there are 22 in total benchmarks without path between source and destination. On the other hand, the CERA approach completes 8 benchmarks which are partly shown in Fig. 16. Finally, in the Complex set 60, only four layouts have been routed which are partly shown in Fig. 17. The “Avg” column points the ratio is 100%, 90%, 43.3%, 26.7% and 13.3% which shows a decreased trend owing to the blocking obstacles are more and more.

Table 4 shows the number of steps of experimental results. To comparison Table 4 with Table 2, more steps are needed in  $40 \times 40$  grids. This phenomenon is caused by more candidates and the longer distance between origin and destination. Not only distance but also path is key factors in route. First, in the Complex set 20, the shortest and the longest steps are 15 and 54 individually. It is caused that the former is near than the latter for source and destination. In the Complex set 30, the shortest and the longest steps are c45 and c37 benchmarks that separately cost 3 and 70 steps. Thirdly, in the Complex set 40, c49 has the shortest routed due that the location of origin and destination is the nearest among benchmarks. In contrast, c37 has the longest path that is shown in Fig. 18 (a). For unconnected benchmarks such as c33, it stops stepping at

Fig. 16. CERA results in complex effect 50 for  $40 \times 40$  grids.

Fig. 17. CERA results in complex effect 60 for  $40 \times 40$  grids.**Table 4**Stepping propagation of CERA for  $40 \times 40$  grids.

Benchmarks	Complex effect					Benchmarks	Complex effect					Benchmarks	Complex effect				
	20	30	40	50	60		20	30	40	50	60		20	30	40	50	60
c31	17	53	8	–	–	c41	42	26	40	–	11	c51	51	34	28	8	–
c32	37	63	–	–	–	c42	33	16	43	6	–	c52	42	61	–	–	–
c33	54	–	–	–	–	c43	15	14	–	14	–	c53	30	33	–	7	4
c34	38	53	–	–	–	c44	31	14	–	9	–	c54	49	14	18	–	–
c35	34	43	–	–	–	c45	19	3	–	–	–	c55	15	23	–	–	–
c36	46	59	14	–	–	c46	24	20	32	–	–	c56	38	24	–	37	–
c37	50	70	74	–	–	c47	52	–	–	–	–	c57	15	5	–	–	8
c38	41	–	45	–	–	c48	49	59	–	5	–	c58	22	10	–	–	–
c39	40	49	29	–	–	c49	45	41	2	–	14	c59	35	61	63	–	–
c40	45	51	30	–	–	c50	45	48	–	–	–	c60	43	56	–	9	–

Fig. 18. CERA results in complex effect 40 for  $40 \times 40$  grids.

label “68” that is demonstrated in Fig. 18(b). In the Complex set 50 and 60, more spaces are used by digital circuit result in less paths than the Complex set 40. On the basis of those results, the route of high complexity SOC becomes more and more difficult in the future.

## 6. Conclusion

This work presents a fast routing verification with complex effect approach that is based on the algorithm of Lee. It can be applied to evaluate various layouts in SOC. Once all

modules are determined their placements in SOC, the CERA performs the routing scheme from origin to destination. The result may be either successfully completed route or disconnected. The former report is useful for designers to further consider of delay and driver issue. In the contrary, the latter points the stop stepping from origin to destination to help designers to adjust placement. In order to demonstrate the effectiveness of the CERA, we conduct five complex sets experiments in  $20 \times 20$  and  $40 \times 40$  grids. Experimental results show that the CERA achieves fast routing verification for diversity architectures in SOC.

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