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ESD Reliability Improvement of an HV nLDMOS by the Bulk FODs Engineering

Shen-Li Chen* and Min-Hua Lee

Department of Electronic Engineering, National United University, Miaoli City 36003, Taiwan

Abstract

The high voltage (HV) lateral double-diffused MOS (LDMOS) has a much lower on-resistance, a higher tolerance to breakdown voltage and a higher output power used for automotive ICs and high-frequency communication modules. However, its shortcomings are evident, including a high trigger voltage (V_{t1}), low holding voltage (V_h), low ESD discharge capability per unit length and multi-fingers unable to fully turn-on, which are serious impacted the ESD reliability capability. In this paper, the HV-nLDMOS device with adding field-oxide-devices (FODs) in the bulk area to make the trigger voltage effectively decreased, and in order to increase the ESD capability is investigated. Furthermore, the influence of bulk P^+ area which was replaced by FODs in the bulk region on snapback parameters in a 0.25- μm 60-V high voltage process is evaluated. After that, the ESD capability has grate increased while the device with adding any FOD structures in the 0.25- μm 60-V high voltage process. The I_{t2} value is $> 7\text{A}$ and to be increased $> 111.74\%$ than that of a reference group. Noteworthy, this structure may make the trigger voltage (V_{t1}) too low to operate normally. Therefore, it should be careful considered that the problem of maximum FOD occupied ratio while using this methodology.

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Keywords: Electrostatic discharge (ESD), Field oxide device (FOD), Latch-up (LU), Lateral-diffused MOS (LDMOS), Trigger voltage (V_{t1}), Secondary breakdown current (I_{t2}), Turned-on resistance (R_{on})

* Corresponding author. Tel.: +886-37-381525; fax: +886-37-362809.

E-mail address: jackchen@nuu.edu.tw.

1. Introduction

With the rapid process technologies development, high voltage control circuits or high power driver devices/circuits are widely used in automotive ICs, high-frequency communication modules, power switches, power management circuits, LED illuminations and LCD drivers [1-4]. The power devices can sustain a high voltage and current, and can be integrated with low voltage logic circuits that not only minimized the chip area but also lowdown the production costs and power consumptions. In order to provide better reliability quality on an HV BCD process for the customer [5-9], the wafer foundries enhance the device electricity and reliability on the layout and design due to the extreme operating environment. There are many kinds of solutions to increase the reliability on source, drain, N-well and NBL [5-6] in the HV device, such as a source-side embedded with the bulk zone [7], and the stripe source-side and bulk electrode are far separated by an FOD. Then, is there any other solutions?

2. Layout Design of DUTs

In this paper, the FOD structures will be applied to the source- and bulk-sides of the HV devices whose experimental structure and schematic layout are shown in Figs 1~ 3. This experiment, we aim to increase the R_{bulk} value of an nLDMOS from source-to-bulk side, hoping not only to reduce the trigger voltage (V_{ti}) and increase ESD robustness, but also to have no impact on the device area. Therefore, under the minimum design rules in this paper, some FODs which are extended into the contact region of the bulk-side, from only one contact replaced shown in Fig. 2(a), gradually increasing the extending contact numbers shown in Figs 2(b)~ 3(a), and finally the contact numbers of an end-to-end in the bulk region have only two contacts shown in Fig. 3(b). It is in order to observe the FOD structure of bulk-side effects on an HV LDMOS device.

In the design of an HV nLDMOS device, a layout symmetrical idea is considered, therefore, for this case whose contact number is set to be 164 in the bulk side. Then, the FODs extend into the bulk region, the upside and lower part of the entire bulk-side can have a contact at least. Therefore, after calculating, while the contacts number is equal to 2, 8, 12, 30, 52, 162 in the bulk side can be replaced by the FODs. However, the total contacts number of the bulk region is equal to 164 on planning, which was due to it not only needs to conform with the distance rule of a contact to the oxide definition (OD) boundary and the distance rule of a contact to the y-direction, but also the contacts number can not be too few. Therefore, the experimental planning groups with adding FODs structure in the bulk region are listed in Table 1. Here, the devices under testing were fabricated by a TSMC 0.25- μm 60-V BCD process. The channel length (L) is kept to be 2- μm , channel width of each finger (W_f) is 100- μm , finger numbers $M=6$, and the total channel width (W_{tot}) is kept a constancy, 600- μm .

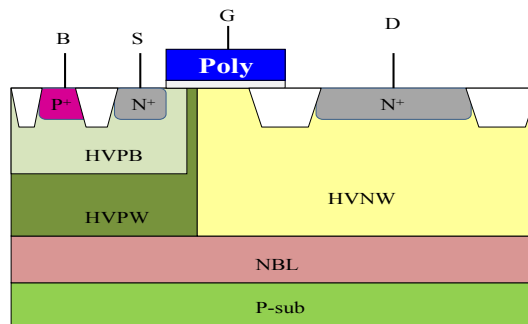


Fig. 1. Cross-sectional view of an HV nLDMOS as FODs adding in the bulk region.

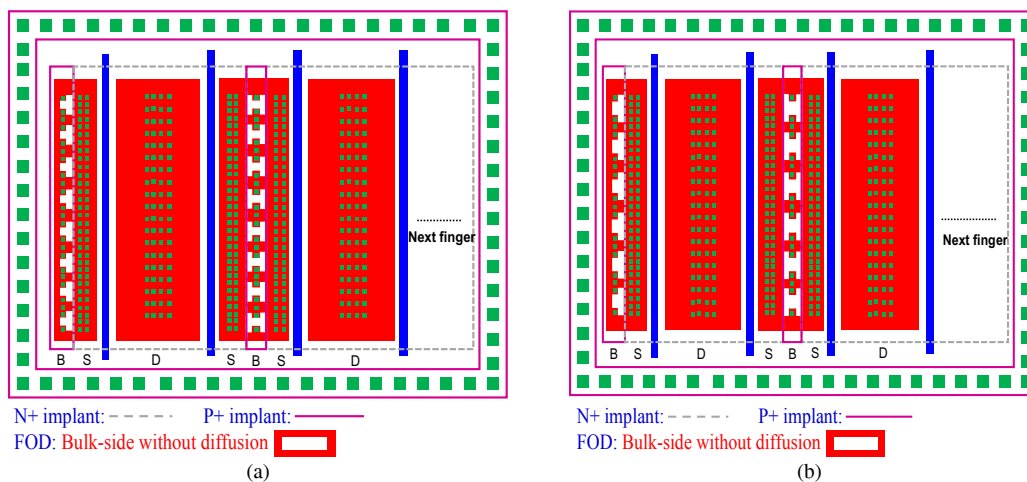


Fig. 2. Schematic layout of an HV nLDMOS as FODs adding in the bulk region (# of contact replaced by FODs in bulk region is (a) 1; and (b)2).

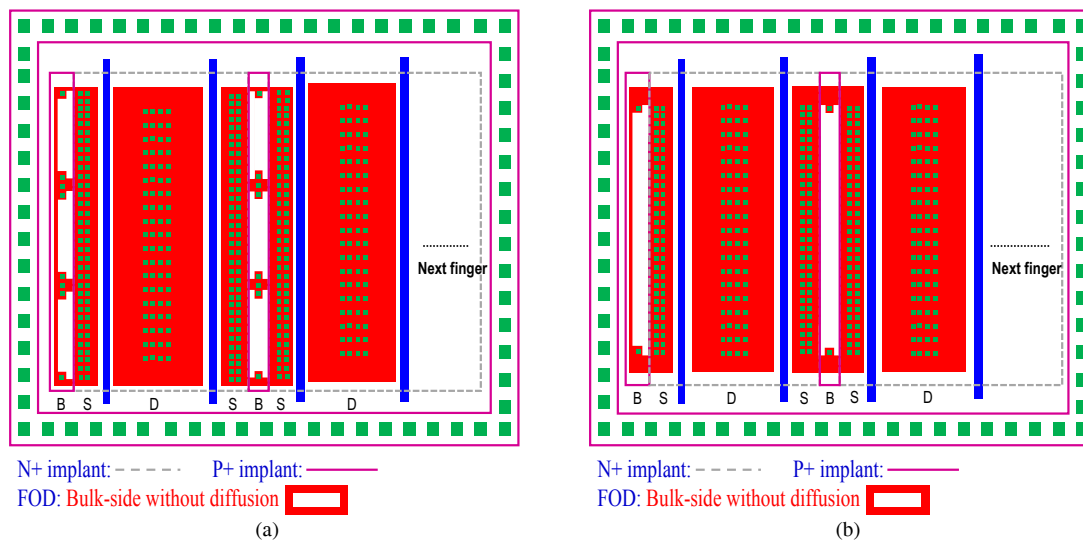


Fig. 3. Schematic layout of an HV nLDMOS as FODs adding in the bulk region (# of contact replaced by FODs in bulk region is (a) 8; and (b)162).

Table 1. Experimental groups of the HV nLDMOS as FODs adding in the bulk region.

Total Contact # in Bulk: 164							
Sample no.	1	2	3	4	5	6	7
Contact # be replaced	1	2	8	12	30	52	162

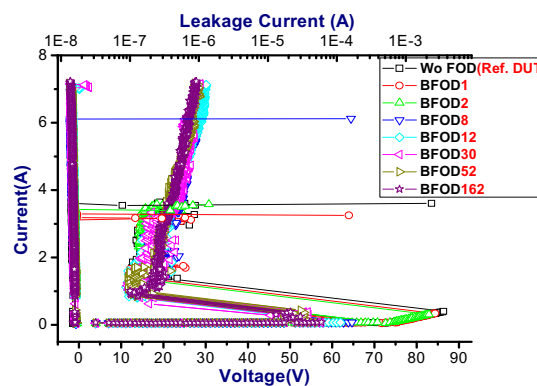
3. Testing Equipment System

A transmission-line-pulse (TLP) system for experimental testing is controlled by the LabVIEW software. It managed the subsystem electrical machine such as the ESD pulse generator, the high-frequency digital oscilloscope and the digital power electric meter instruments to achieve the automatic measurement. This machine can provide a continuous step-high square wave to device, and short raise time of the continuous square wave can also simulate transient noise of ESD. This HBM-like system has used the short square wave with 100 ns pulse widths and 10 ns rising/falling times to evaluate the voltage and current response of device.

4. Measurement Results and Discussion

As the FOD structures are applied to bulk region, the TLP data can be obtained and shown in Fig. 4(a) and Table 2. From these data, it can be clearly seen that when the component is added FODs in the bulk side, the I_{t2} value will increase rapidly as the total area of FODs in the bulk side is larger. Due to the power limitation of TLP equipment, the I_{t2} value of component reaches 7-A (the equivalent HBM immunity greater than 10-kV), we labeled it as > 7-A on Table 2. Meanwhile, it can find that when the contacts number of bulk side was replaced by FODs and was greater than 30, that is, the total area ratio of FODs in the bulk side was greater than 93/100, it will appear a secondary-breakdown phenomenon shown in Fig. 4(b). As the area ratio of FODs in the bulk side is enhanced more, the bulk-to-source resistance (R_{bulk}) will be greater, which will result in the trigger voltage (V_{t1}) smaller, and the trigger voltage decreased as the area ratio of FODs increased. When the area ratio of FODs is reached 93/100, the trigger voltage has down to about 60-V, thus making the other fingers easier to turn on, and then that will cause many snapback conduction phenomena, and the I_{t2} value became higher.

Our proposed structure can effectively enhance ESD capability of element, but the trigger voltage of device might be less than 60-V, which may cause internal circuit performance abnormal. Therefore, we must notice the area limitation in FODs in the bulk region to enhance device ESD ability. The V_{t1} , V_h versus FOD area ratio relationship is shown in Fig. 5(a). Here, the V_h values seem to be a U-shaped distribution. When the occupied area ratio of FODs structure is 86/100, the holding voltage (V_h) is existed a lowest value. Nevertheless, the V_h was increased gradually again as the FOD area ratio was > 86/100. Therefore, the FOD occupied area ratio in the bulk region will be judged in the ESD ability and latch-up immunity considerations. In Fig. 5(b), with a suitable ratio of FODs adding, nLDMOS structures possess a stronger I_{t2} value, improved about 1.12% ~ >117.74% as compared with the reference group. So, it can be concluded that an FOD adding in the bulk region is good for ESD robustness.



(a)

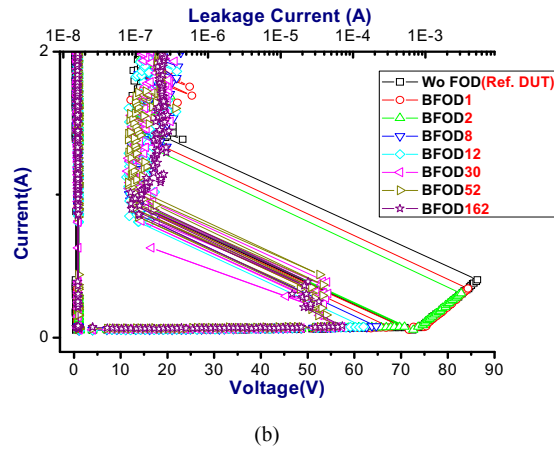
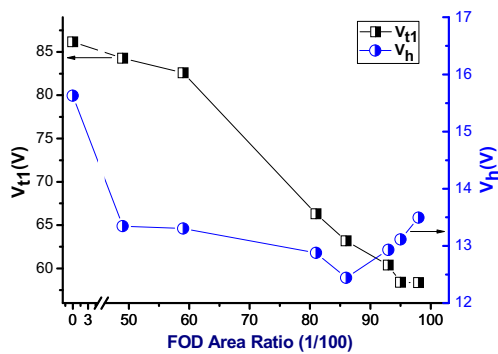


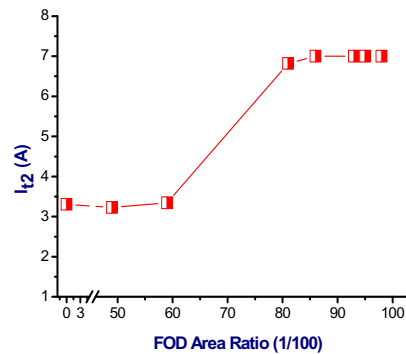
Fig. 4. (a) Normal; and (b) magnified diagram of snapback I-V curves & leakage currents of nLDMOS DUTs as FODs adding in the bulk side (red # indicated contacts be replaced by FODs).

Table 2. Snapback key parameters of nLDMOS DUTs as FODs adding in the bulk side (σ was averaged by 5 DUTs and red # indicated contacts be replaced by FODs).

FOD in Bulk	V_{th} (V)	V_h (V)	I_{D2} (A) (mean $\pm \sigma$)	FOD Area Ratio
Wo FOD (Ref. DUT)	86.156	15.629	3.306 \pm 0.323	0
BFOD1	84.269	13.345	3.228 \pm 0.206	49/100
BFOD2	82.586	13.304	3.343 \pm 0.229	59/100
BFOD8	66.317	12.878	6.820 \pm 0.865	81/100
BFOD12	63.174	12.442	>7	86/100
BFOD30	60.388	12.931	>7	93/100
BFOD52	58.401	13.114	>7	95/100
BFOD162	58.355	13.496	>7	98/100



(a)



(b)

Fig. 5. The relationship diagram of (a) V_{th} , V_h ; (b) I_{D2} values vs. FOD area ratio as FODs adding in the bulk side.

5. Conclusion

This paper proposed an HV nLDMOS device with FODs structures in the bulk side to observe ESD reliability. With the FOD structure in the bulk region can effectively enhance the anti-ESD ability of these 60-V nLDMOS devices. The I_{t2} average value can be improved about 1.12% ~ >111.74% as compared with the reference group value. Moreover, we should also pay attention to the trigger voltage of a DUT might not be too small and less than the operation voltage 60-V as with increasing FOD structure occupied area. Therefore, with these FODs adding in the bulk region can extremely effective enhance the ESD ability; however, we should take care about the maximum FODs area limitation.

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