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A SoC for Pressure Balance Measurement Application in Total Knee Arthroplasty*

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Abstract

This paper describes a System-on-Chip(SoC) for pressure balance measurement in total knee arthroplasty (TKA). This SoC consists of 8051 processor, ADC, RF transceiver with 3Mbps MSK transmitting and 64kbps OOK receiving, SPI interface for transmitting the data between the SoC and EEPROM, SRAM acting as memory buffer and some other peripherals. Fabricated in 0.18μm CMOS, the area of the SoC with pads is up to 3 mm^2*3 mm^2.

Keywords: SoC, 8051, Total Knee Arthroplasty, pressure balance measurement;

1. Introduction

It's reported that 90% of the population over the age of 40 suffers from some degree of degenerative joint disease[1]. Artificial biological material is used to replace the bone and cartilage of the knee that has been damaged in total knee arthroplasty. It has a more than 30-year history in the treatment of arthritis of one compartment of the tibiofemoral joint. The total of knee replacement surgery had been more than 600,000 in 2007. There will be nearly 1.4 million knee replacement performed in the year 2015[2].

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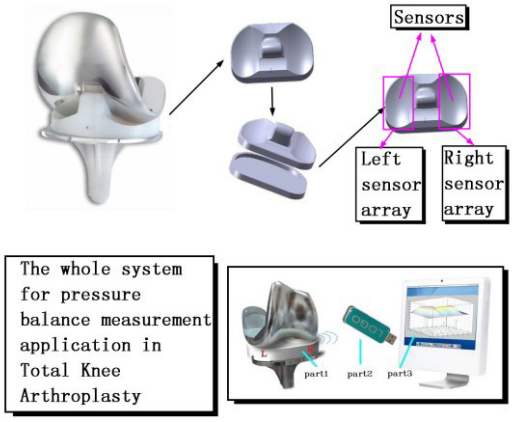

Fig. 1 The whole device

The artificial knee implant may fail because of attrition, loosening or misalignment. As a result, recover surgery is needed, which will bring more pain to the patient. In order to diagnose the implanted knee, to evaluate operating method of TKA, or to evaluate design of knee implants, many researchers have investigated the problems of total knee arthroplasty. [3]-[7] The imbalance of knee implants will induce the life of the artificial knee implants. And in this paper, we propose a SoC design for pressure balance measurement in total knee arthroplasty. Fig. 1 shows the designed device performances as a monitor by measuring the pressure on both sides of the knee implant. There are 3 sensors each side. The sum of the sensors is the pressure values. In this paper, we will focus on the implementation of the SoC.

This paper is organized as follows: Section 2 presents the whole system architecture. Section 3 highlights the implementation of the SoC. Some simulation results will be presented in Section 4. Section 5 provides the concluding remarks.

2. System overview

Figure 1 shows the system architecture of the device. The device consists of 6 sensors, an EEPROM and a design SoC chip. The sensors are divided into a couple of parts equally. The range of each sensor is 0~1.5Kg, and then the range of each side is 4.5Kg. At first, the designed SoC chip receives the data from the sensors. Second, the received data will be packaged by some encoders integrated in the SoC chip. At last, the packaged data will be transmitted by the RF transmitter integrated in the SoC chip to the base station outside the device.

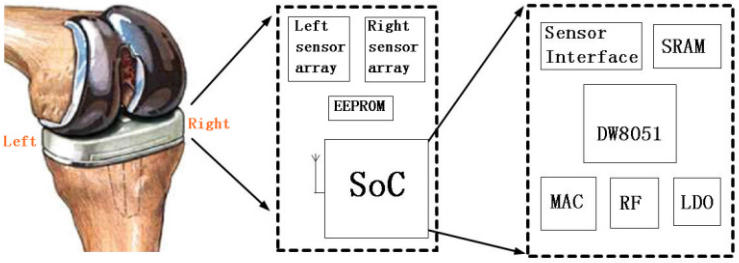

Fig. 2 System architecture

Fig. 2 shows the system architecture of the design device. The top-level system architecture of the SoC is illustrated in figure 3. It includes an 8051 microcontroller. EEPROM memories are not available in the CMOS process used to fabricate the chip, and an EEPROM chip is used to storage the software. Once the system powers up, the software is loaded from the EEPROM to the 4KB SRAM integrated in the designed SoC. The SoC features a Serial Peripheral Interface (SPI). The SPI interface is used to communicate with the EEPROM. A boot-loader block is designed to download the software from the EEPROM. Because the signals collected from the sensors are analog signal, we need an ADC to convert the analog signal to digital signal. The RF transceiver is also included.

The implementation will be discussed in Section 3.

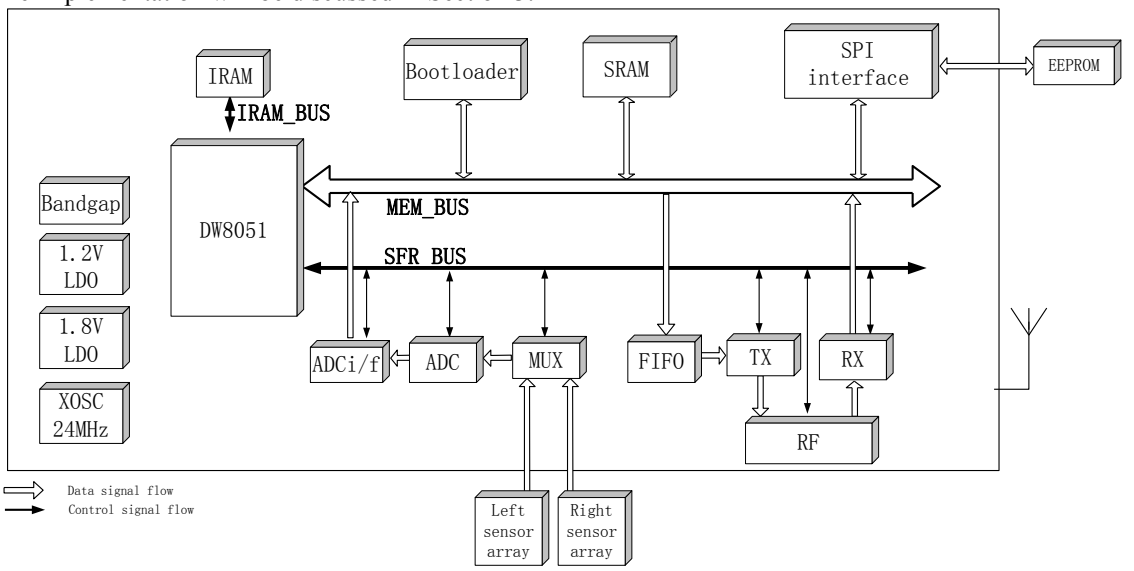

Fig. 3 Top-level system architecture of the SoC

3. Implementation of the SoC

3.1. Microcontroller and memory on chip

The digital core of the SoC is designed based on DW8051 IP core which is higher performance than traditional 8051 microcontroller. [8] The DW8051 IP core executes per instruction in a 4-clock bus cycle, as opposed to the 12-clock bus cycle in the traditional 8051. And this microcontroller manages the MAC, SPI interface, ADC interface and other digital blocks by reading/writing Special Function Registers (SFRs).

The system clock is 12MHz. The ADC works at 150kHz and the EEPROM works at 500kHz. In order to provide the clocks to ADC and EEPROM, the clock distribution is designed.

This SoC integrates a 4KB SRAM and a 256B SRAM. The size of the SRAM is determined by recognition task, while the size of the SRAM is determined by the size of program. Because the size of software is less than 4KB, we utilize a 4KB SRAM to storage the software. Once the system is powered up, it initializes. The boot-loader is executed to download the software from the EEPROM chip to the 4kB SRAM of the SoC.

3.2. Media access controller (MAC) and FIFO

The MAC consists of transmission and receiving processing block. Figure 4 shows us the main functions of the MAC. In the transmission processing block, the transmitted data converts to the cyclic redundancy check (CRC) code and then the Reed-Solomon (RS) code. The RS code will be whitened before transmission. The receiving processing is inverse process of the transmission processing. The received data will be decoded by the RS decoder and the CRC decoder. The main function of the MAC is to package the data received from the sensor array.

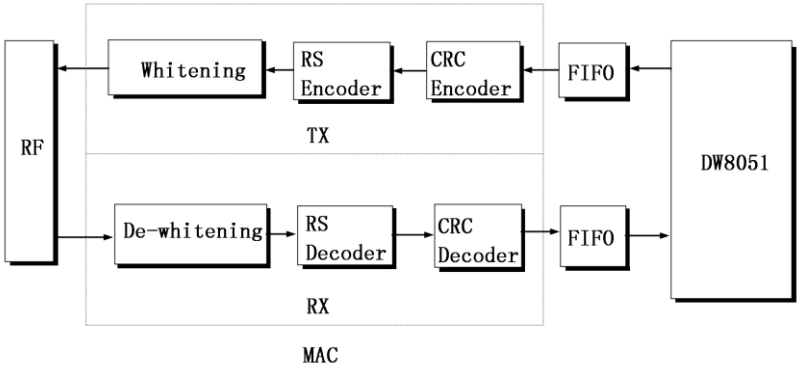

Fig. 4 Architecture of the MAC

Figure 5 shows the format of the package. The complete package consists of a preamble, a header and two data blocks. And each data block contains a data part, a CRC part and a RS part. In the data part of the data clock, 112 bits is valid, and the last bit is invalid.

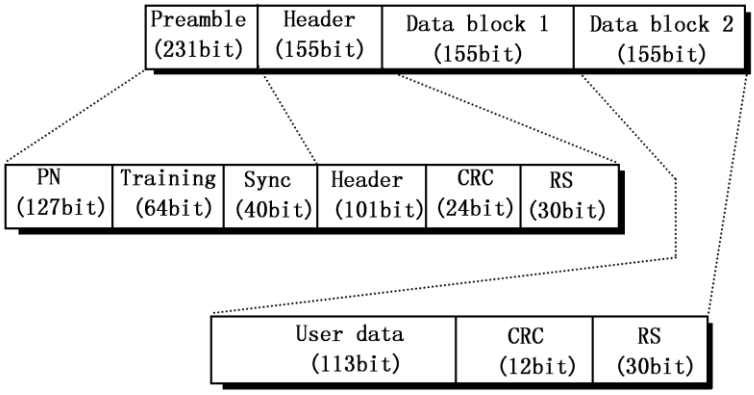

Fig. 5 Format of the complete package

FIFO memory is a key component of the SoC, which is commonly used for buffer and flow control. A classical asynchronous FIFO is implemented. [9] Asynchronous FIFOs are used to safely pass data from one clock domain to another clock domain. The FIFO design in this paper uses 6-bit pointers with 32 write-able locations to handle full condition, and uses 4-bit pointers with 8 read-able locations to help handle empty

condition. The data to be written is one byte (8 bits), while the data to be read is four bytes (32 bits). Figure 6 shows the full and empty conditions of the FIFO. On reset, both pointers are reset to zero. As soon as the first data is written, the empty flag is cleared. When the write pointer has wrapped around one more time than the read pointer, the FIFO is full. If the high 3 bits of the write pointer is equal to the read pointer, the FIFO is empty.

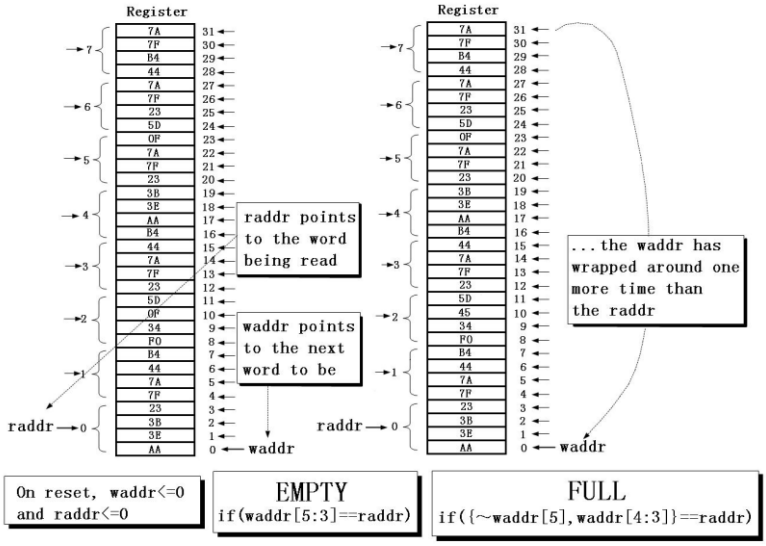

Fig. 6 Full and empty conditions of the FIFO

The SoC receives the data from the sensors one by one. Each data received from a single sensor is 2 bytes. In order to distinguish a sensor from each other, we mark each sensor with a unique label. All the sensors are marked from 0 to 5. As a result, the received data will be marked with an additional byte, and the data will be 3 bytes. For example, the data from the second sensor is 0x1231, and the data sent to FIFO will be 0x101231. The depth of the FIFO is 32 bytes. If the FIFO is full, an interrupt will be created. At that time, the data of the FIFO will be packaged by the MAC and transmitted by the RF. As soon as the FIFO is not full, the data will continue to be passed to FIFO. Figure 7 shows the data processing.

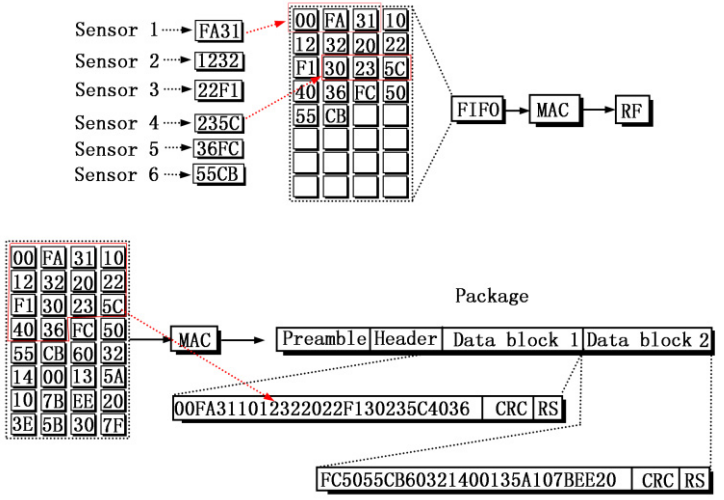

Fig. 7 Data processing

3.3. Power management, RF transceiver and ADC

The SoC has 3 power domains, 3.3V for the I/O pads, 1.8V for the digital core, and 1.2V for the RF transmitter. Actually, the RF transmitter uses both the 1.2V and the 1.8V. There are 2 LDOs which one converts 3.3V to 1.8V and the other converts 3.3V to 1.2V. Figure 8 show the power management.

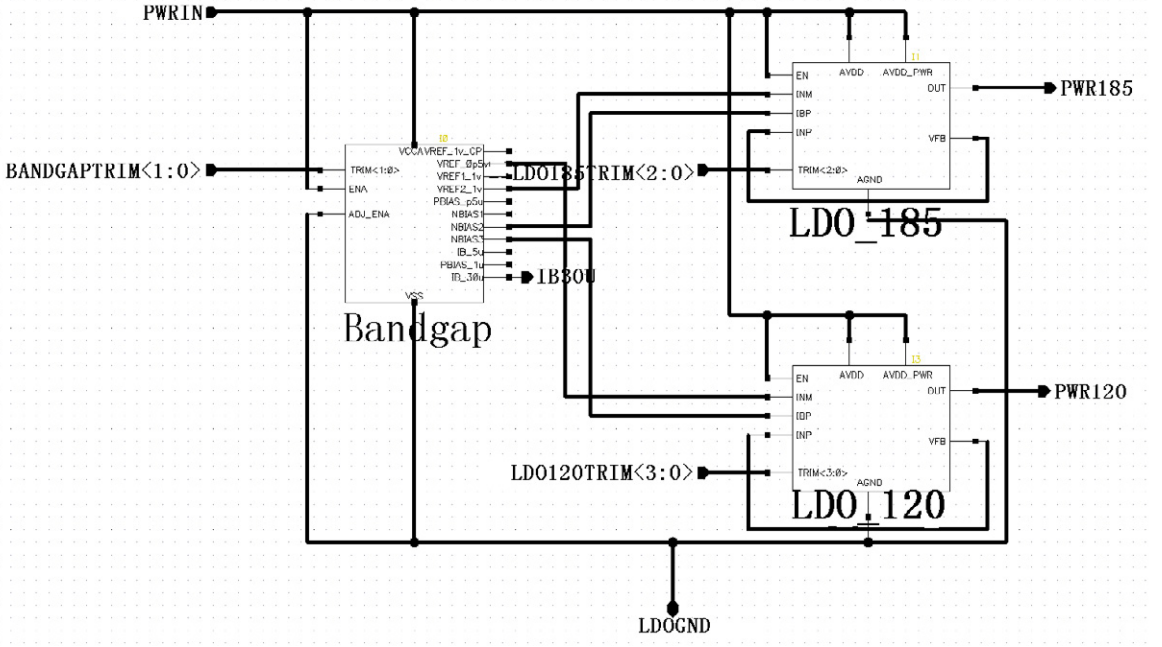

Fig. 8 Power management

The RF transceiver transmits data using 3Mbps MSK modulation and receives data using 64kbps OOK in the half-duplex mode. It is comprised of up- and down-converter, phase-locked loop (PLL), a classical DAC, a VCO.

The ADC consists of a 4-bit ramp-down converter and a residue amplifier with gain of 2^4. And the power supply voltage is 1.2V~3.6V.

3.4. Integrated circuit

The SoC was fabricated in UMC 0.18μm CMOS technology with a die size of 3mm×3mm. The circuit layout and annotated floorplan of the complete chip is shown in Figure 9.

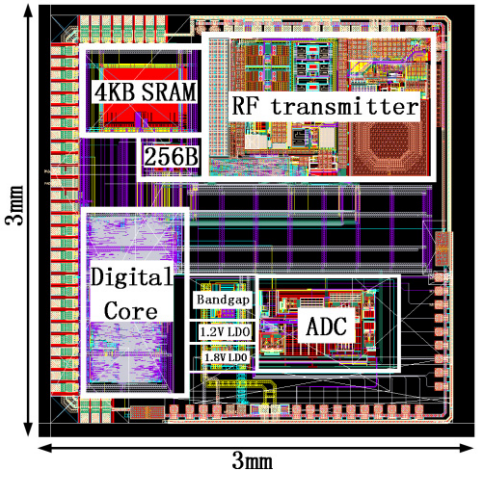

Fig. 9 Layout of the SoC

4. Simulation Results

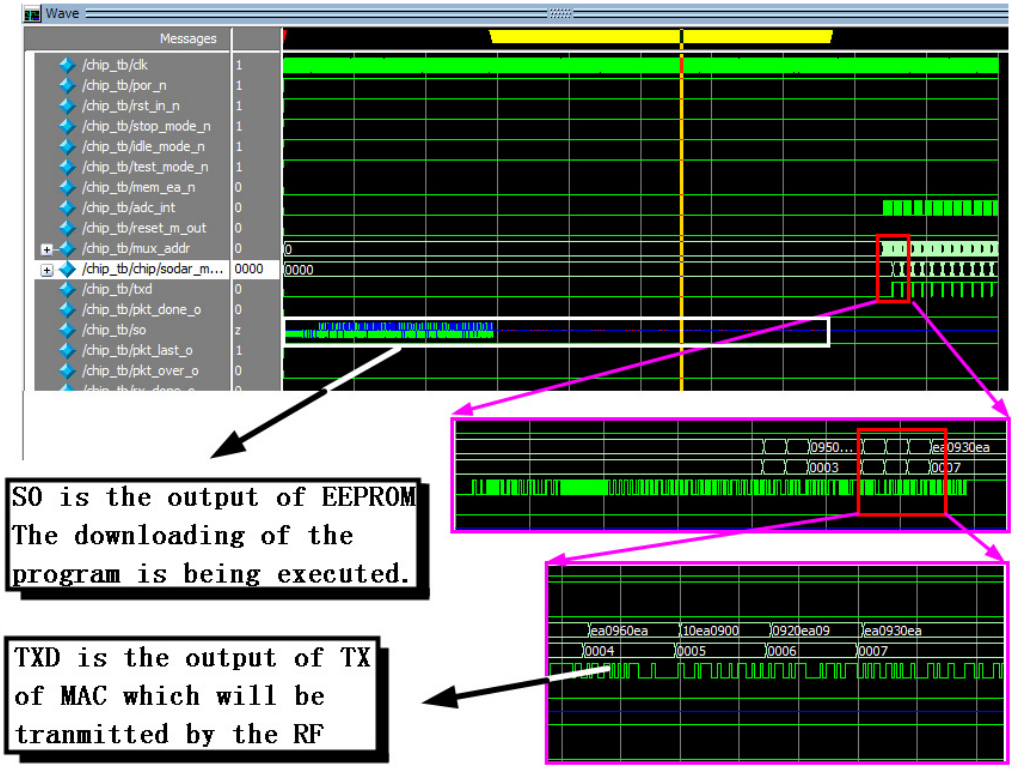

Fig. 10 The simulation result

The whole integrated SoC is realized based on a 0.18μm CMOS process using the above described circuit principles. The final layout is shown in Figure 10. The die size is 3mm*3mm. Figure 8 shows the simulation result of the digital core of the SoC. SO is the output of EEPROM, and the figure in the white block shows the downloading of the program. TXD is the output of TX of MAC which will be transmitted by the RF, and it is a key signal to judge the output of the SoC wrong or right.

Table 1 shows the summary of the SoC, and Table 2 shows the performance summary of the SoC compared with the chip nRF24LE.

Table 1 Summary of the SoC

Item	Description
Microcontroller	DW8051
Gate count of digital core	47700 gates
Memory	4KB SRAM, 256B SRAM
Peripherals	MAC, RF, ADC, MUX, Boot-loader, ADC I/F, FIFO
Fabrication	0.18μm CMOS process, die size: 3mm×3mm

Table 3 performance summary of the SoC compared with the chip nRF24LE1 [10]

Parameters	This work	nRF24LE1
Supply voltage	1.9V~3.6V	1.9V~3.6V
Microcontroller	DW8051	Fast 8-bit microcontroller
Memory	4KB SRAM	16KB flash memory and 1KB on-chip RAM memory
RF channel	404~432MHz	2.4~2.4853GHz
ADC	16-bit resolution	6,8,10 or 12 bit resolution
Oscillators	Off-chip 24MHz crystal oscillator	On-chip oscillators: 16 MHz crystal oscillator XOSC16M 16 MHz RC-oscillator RCOSC16M 32.768 kHz crystal oscillator XOSC32K 32.768 kHz RC-oscillator RCOSC32K

5. Conclusion

The SoC designed for pressure balance measurement applications in total knee arthroplasty is fabricated in UMC18 CMOS process with a die size of 3mm*3mm. The SoC integrates all building blocks---including RF transmitter, ADC, DW8051, ADC interface, MAC, MAC controller, boot-loader, SPI interface for EEROM, MUX, LDOs and BandGap. We can use this chip to measure the pressure applications in total knee arthroplasty. And it is high level of integration.

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