

Reversible Computer Hardware

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Abstract

Conventional logic gates (e.g. AND gates) cannot be used for building a reversible computer. An appropriate design approach is necessary. Both small building blocks and a more complex circuit in MOS technology are presented. Today, these are useful in low-power digital electronics. Tomorrow, these may be useful in quantum computers.

Keywords: reversible computer, MOS technology.

1 Introduction

Reversible computing [1] is useful both in lossless classical computing [2] [3] and in quantum computing [4]. It can be implemented in both classical and quantum hardware technologies.

Reversible logic circuits distinguish themselves from arbitrary logic circuits by two properties: (1) the number of output bits equals the number of input bits and (2) for each pair of different input words, the two corresponding output words are different. For instance, it is clear that an AND gate is not reversible, as (a) it has only one output bit, but two input bits and (b) for three different input words, the output words are equal. See Table 1a. On the other hand, Table 1b gives an example of a reversible truth table. Here, the number of inputs equals the number of outputs, i.e. three. This number is called the width w of the reversible circuit. The table gives all possible input words ABC . We see how all the corresponding output words PQR are different. For this reason, there can exist only $8! = (2^w)!$ different reversible truth tables of $w = 3$. They form a mathematical group.

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		<i>ABC</i>		<i>PQR</i>	
		0 0 0		0 0 0	
		0 0 1		0 0 1	
0 0		0 1 0		0 1 0	
0 1		0 1 1		1 0 0	
1 0		1 0 0		0 1 1	
1 1		1 0 1		1 0 1	
		1 1 0		1 1 0	
		1 1 1		1 1 1	
(a)		(b)		(c)	

Table 1
Truth table for (a) AND gate, (b) MILLER gate, and (c) CONTROLLED NOT gate.

2 Implementation

For physical implementation, dual logic is very convenient. It means that any logic variable X is represented by two physical quantities, the former representing X itself, the latter representing NOT X . Thus, e.g. the physical gate realizing the logic gate of Table 1b has six physical inputs: A , NOT A , B , NOT B , C , and NOT C , or, in short-hand notation: A , \overline{A} , B , \overline{B} , C , and \overline{C} . It also has six physical outputs: P , \overline{P} , Q , \overline{Q} , R , and \overline{R} . Such approach is common in electronics, where it is called dual-line or dual-rail electronics.

Dual-line hardware allows very simple implementation of the inverter. It suffices to interchange its two physical lines in order to invert a variable, i.e. in order to hardwire the NOT gate. Conditional NOTs are NOT gates which are controlled by switches. A first example is the CONTROLLED NOT gate:

$$P = A$$
$$Q = A \oplus B \text{ ,}$$

where \oplus stands for the logic operation XOR (EXCLUSIVE OR). See Table 1c. These logic relationships are implemented into the physical world as follows:

- output P is simply connected to input A ,
- output \overline{P} is simply connected to input \overline{A} ,

- output Q is connected to input B if $A = 0$,
but connected to \overline{B} if $A = 1$, and
- output \overline{Q} is connected to input \overline{B} if $A = 0$,
but connected to B if $A = 1$.

The connections from B and \overline{B} to Q and \overline{Q} are shown in Figure 1a. In the figure, the arrows show the switch positions if the accompanying label is equal to 1. A second example is the CONTROLLED CONTROLLED NOT gate or TOFFOLI gate:

$$\begin{aligned} P &= A \\ Q &= B \\ R &= AB \oplus C, \end{aligned}$$

where AB is a short-hand notation for A AND B . Its implementation is shown in Figure 1b. The above design philosophy can be extrapolated to a control gate with arbitrary control function f :

$$\begin{aligned} P &= A \\ Q &= B \\ R &= f(A, B) \oplus C. \end{aligned}$$

Suffice it to wire the appropriate series and parallel connections of switches. There exist $16 = 2^{2^{w-1}}$ such control gates. They form a mathematical subgroup [5].

Now that we have a hardware approach, we can realize any reversible circuit in hardware. Any reversible circuit of width w can be decomposed into a cascade of $2w - 1$ control gates, each with an appropriate control function [6] [7]. See Figure 2 for $w = 4$. It is possible to prove that this synthesis method is ‘almost optimal’, as $2w - 4$ blocks cannot suffice. This design is reminiscent of the so-called banyan networks of telecommunication (named after an Asian tree species) [7] [8].

In electronic circuits, a switch is realized by two MOS transistors in parallel (one n-MOS transistor and one p-MOS transistor). So, for a CONTROLLED NOT, we need 8 transistors and for a CONTROLLED CONTROLLED NOT sixteen. Figure 3 shows an application: a 4-bit ripple adder, built from four circuits called ‘full adders’, each constructed from two CONTROLLED NOTs and two CONTROLLED CONTROLLED NOTs. The complete circuit thus contains 192 transistors [9]. This chip is able to perform computations both from left to right and from right to left.

Switches not only can decide whether an input variable is inverted or not, but equally well decide whether two input variables are swapped or not. This concept leads to the CONTROLLED SWAP or FREDKIN gate:

$$\begin{aligned} P &= A \\ Q &= B \oplus AB \oplus AC \\ R &= C \oplus AB \oplus AC. \end{aligned}$$

Figure 1c shows the physical realisation, with 8 switches, i.e. 16 transistors.

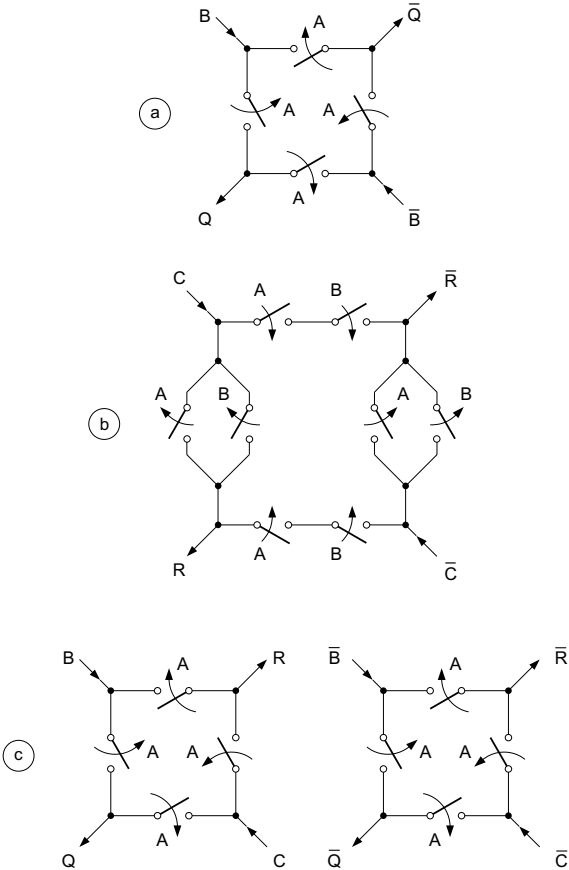


Fig. 1. Schematic for (a) CONTROLLED NOT gate, (b) CONTROLLED CONTROLLED NOT gate, and (c) CONTROLLED SWAP gate.

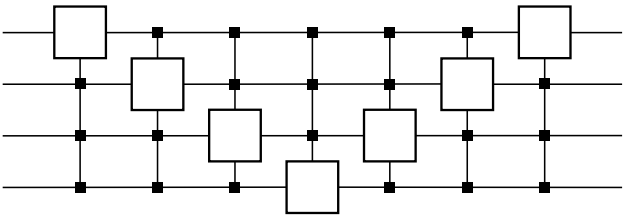


Fig. 2. Decomposition of a reversible circuit of width $w = 4$ into $2w - 1 = 7$ control gates.

3 Energy consumption

The continuing shrinking of the transistor sizes (i.e. Moore’s law) leads to a continuing decrease of the energy dissipation per computational step. This heat generation Q is of the order of magnitude of CV_t^2 , where V_t is the threshold voltage of the transistors and C is the total capacitance of the logic gate [10]. We see how Q becomes smaller and smaller, as transistor dimensions shrink. However, dissipation in electronic circuits still is about four orders of magnitude in excess of the Lan-

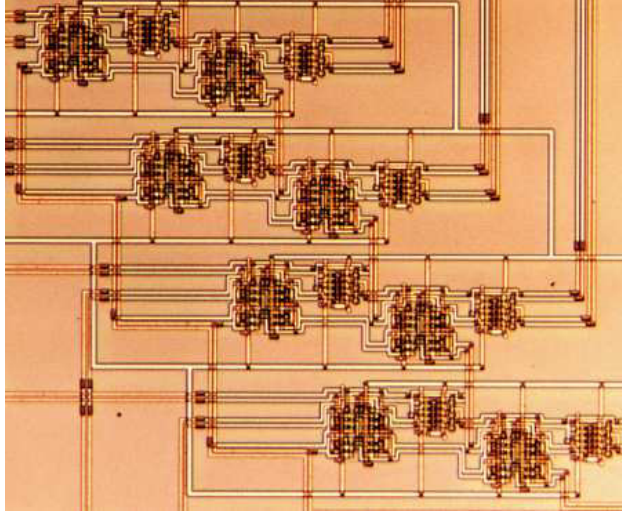


Fig. 3. Microscope photograph ($140\ \mu\text{m} \times 120\ \mu\text{m}$) of a 4-bit reversible ripple adder.

dauer quantum $kT \log(2)$, which amounts (for $T = 300\ \text{K}$) to about $3 \times 10^{-21}\ \text{J}$ or 3 zeptojoule.

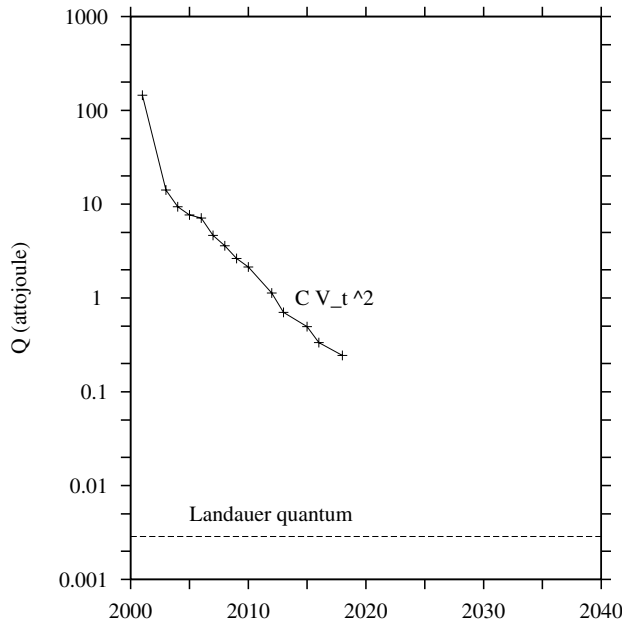


Fig. 4. Heat generation Q in future technologies.

Further shrinking of transistor width and length and further reduction of V_t ultimately will lead to a Q value in the neighbourhood of $kT \log(2)$. That day, digital electronics will have good reason to be reversible, because entropy generation, caused by throwing away bits of information, will then be the main source of heat

generation in chips. According to the *International Technology Roadmap of Semiconductors* [11], we may expect this to happen around 2036. See Figure 4. Only reversible computers will be able to cross the ‘Landauer barrier’.

This, however, does not mean that the reversible MOS circuits are useless today. Indeed, as they are a reversible form of pass-transistor topology, they are particularly suited for so-called adiabatic addressing. Here, all signals are gradually set, first to an intermediate level, then to their final values. In practice, such procedure leads to a factor of about 10 in power reduction [10].

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