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Design of Signal Distortion Measurement System Based on TMS320F2808

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Abstract

TMS320F2808 DSP chip as the core, combined with signal conditioning and keyboard scan peripheral circuits, made up the hardware circuit of the measuring system. As for software,DSP as the main controller, realized the data display ,controlment and management about the whole system， Using the DSP internal integrated ADC module to achieve the data collection, while using its internal resources to complete the FFT algorithm and optimization. The field test results show that this measuring system of digital signal distortion realizes the amplitude and frequency display in time domain and frequency domain when the setting signal passed the test system, and the measuring error is less than 0.8dB.

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Keywords: DSP; data collection; FFT algorithm; signal distortion

1. Introduction

It is usually used in circuit analysis, production, repair, measurement and other fields that the signal source as incentive source. It has high requirements about the quality of provided signal, therefore, it is particularly important for the signal distortion measurement, which usually measured by using the distortion measurement instrument, but the instrument is expensive and inconvenient to carry. According to the traditional simulation method of testing the signal distortion measurement can not adapt to the current situation of the developing

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new technology. This paper introduces a digital test method which used simple electronic circuit to measure the signal distortion. This method has the characteristics of simple, convenient testing and high precision.

2. Implementation

It is using the real fast Fourier transform (RFFT) optimization algorithms for the design of digital signal distortion measurement system. The overall block diagram of digital signal distortion measurement system shown in Figure 1.The given signal into the analog channel through the test circuit, after being conditioned, signal is sampling high speed by the DSP internal ADC. Combined with the FFT algorithm , the sampled data are sent to the LCD for display by using the DSP processor.

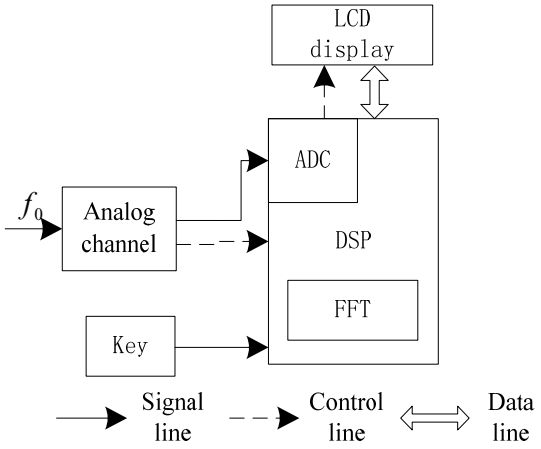

Fig. 1. Overall system block diagram

3. Algorithm Selection of Spectrum Analysis

Normally, the input sequence is pure real, but the input sequence of the FFT operation is plural, this must be form a plural sequence by replaced imaginary part with a zero manually. But the amount of its calculation will increase, computation time will be longer , memory space will increase, the system is not conducive to real-time processing. In view of this, we made some improvements about the original real number FFT algorithm, namely RFFT optimization algorithm. The specific contents are as follows:

If a finite sequence of CKH $x(n)$， $n = 0,1,...,2N-1$,decomposed it into even items $g(r) = x(2r)$ and odd items $h(r) = x(2r+1)$, the even one as the real part of the N point plural finite-length sequence, and the odd as the imaginary part of the N point plural finite-length sequence, then composed a sequence like this:

$$y(r) = g(r) + jh(r), r = 0,1,..., N-1 \quad (1)$$

FFT the N point plural finite-length sequences can obtained:

$$Y(k)=\sum_{r=0}^{N-1} y(r)e^{-j\frac{2\pi}{N}kr}=Y_R(k)+jY_I(k) \quad , \quad k=0,1,...,N-1 \tag{2}$$

From the conjugate symmetry of the fast Fourier transform we know :

$$G(k)=\frac{1}{2}\left[Y(k)+Y^*(N-k)\right]=\frac{1}{2}[Y_R(k)+Y_R(N-k)]+j\frac{1}{2}[Y_I(k)-Y_I(N-k)] \quad k=0,1,...,N-1 \tag{3}$$

$$H(k)=-\frac{j}{2}\left[Y(k)-Y^*(N-k)\right] \quad =\frac{1}{2}[Y_I(k)+Y_I(N-k)]+j\frac{1}{2}[Y_R(N-k)-Y_R(k)] \quad k=0,1,...,N-1 \tag{4}$$

Since the first half N point FFT of the real sequence $x(n)$ whose length is $2N$ is:

$$X(k)=G(k)+W_{2N}^{k}H(k)=X_R(k)+jX_1(k) \quad , \quad k=0,1,...,N-1 \tag{5}$$

The second half N point FFT of $X(k)$ is:

$$X(2N-k)=X_R(2N-k)+jX_1(2N-k) \quad =X_R(k)-jX_1(k) \quad , \quad k=0,1,...,N-1 \tag{6}$$

The (3), (4) type substitution (5) type available:

$$\begin{aligned} X_R(k)&=\frac{1}{2}[Y_R(k)+Y_R(N-k)]+\frac{1}{2}\cos(\frac{\pi k}{N})[Y_I(k)+Y_I(N-k)] \\ &-\frac{1}{2}\sin(\frac{\pi k}{N})[Y_R(k)-Y_R(N-k)], \quad k=0,1,...,N-1 \end{aligned} \tag{7}$$

$$\begin{aligned} X_I(k)&=\frac{1}{2}[Y_I(k)-Y_I(N-k)]-\frac{1}{2}\cos(\frac{\pi k}{N})[Y_R(k)-Y_R(N-k)] \\ &-\frac{1}{2}\sin(\frac{\pi k}{N})[Y_I(k)+Y_I(N-k)], \quad k=0,1,...,N-1 \end{aligned} \tag{8}$$

Equation (1) form a N point plural sequence $y(r)$,from equation (2) we obtained the FFT results $Y(k)$ of $y(r)$,according formula (7) , (8) ,we obtained the real part and imaginary part of the first half of $X(k)$ by using the real part and imaginary part of $Y(k)$ .Since the symmetry of FFT spectrum , we only need to calculate the spectrum of the first half of the N point $X(k)$ [1][2].

Compared to calculate the real FFT directly, RFFT optimization algorithms reduce nearly half amount of the computation, while saving memory space. Obviously, RFFT optimization algorithm is a method of saving computation, speed nearly doubled. It is the core algorithms of our design.

4. Hardware Design

4.1. Bias module

Using TL431 chip to design The 1.5V DC bias source ,the aim is lift the input voltage to ADC input range. Bias module shown in Figure 2. TL431 is a three-terminal programmable shunt regulator diode, whose programmable voltage is 36V,output impedance is 0.22 Ohms, and it has low output noise voltage. When it is working properly, there is a reverse current between 3-pin and 2-pin, and generate a 2.5V reference voltage at the third pin, we will obtain a 1.5V reference voltage by adjusting the variable resistor R41[3].

The output reference voltage is connected to the voltage follower that designed with integrated operational amplifier OPA2134, to achieve the function high input impedance, low output impedance. OPA2134 is the operational amplifier that applied in the audio range with the superiorities of Ultra-low distortion, low noise , unity gain stable, it can be suppled by dual power ,its bandwidth is 8MHz.It provides excellent common-mode rejection and maintain low input bias current, and minimizing distortion over a wide input voltage range[4].

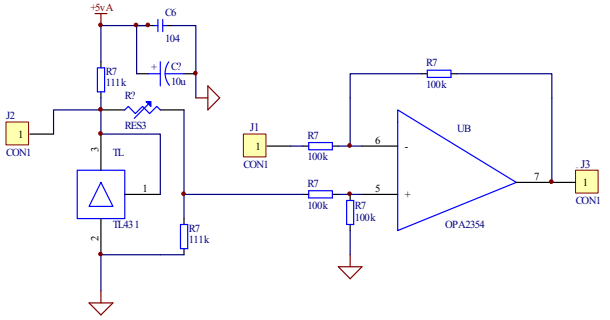

Fig. 2. Bias Module Schematic

4.2. ADC driver module

ADC driver module schematic diagram shown in Figure 3.If the input signal into the ADC acquisition directly, digital signal of DSP will do interference to the input analog signal, even a serious distortion of the input signal. Therefore, we added a voltage follower before the signal into the ADC of integrated DSP to realize the function of isolate the interference signal .This module uses the integrated operational amplifier chip OPA340 on the circuit (ADC circuit) design. OPA340 is a rail to rail amplifier with CMOS technology, single power supply, 5.5MHz bandwidth. It is the characteristic of rail to rail input / output and high-speed processing that made it be the ideal chip of ADC driver[5].Because the voltage range of DSP internal integrated ADC is 0~3V,So we use a resistor divider limits the supplied voltage of operational amplifier for 0~3V,that is, the output voltage of operational amplifier is0~3V,Thereby protecting the DSP internal integrated ADC.

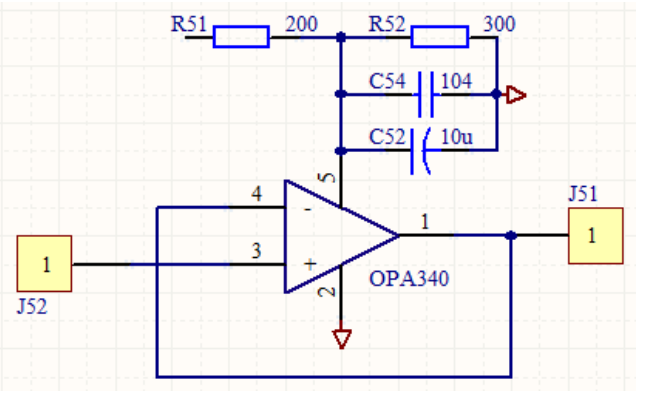

Fig. 3. ADC Driver Module Schematic

5. Software Design

Software design flowchart of the digitized signal distortion test system shown in Figure 4.

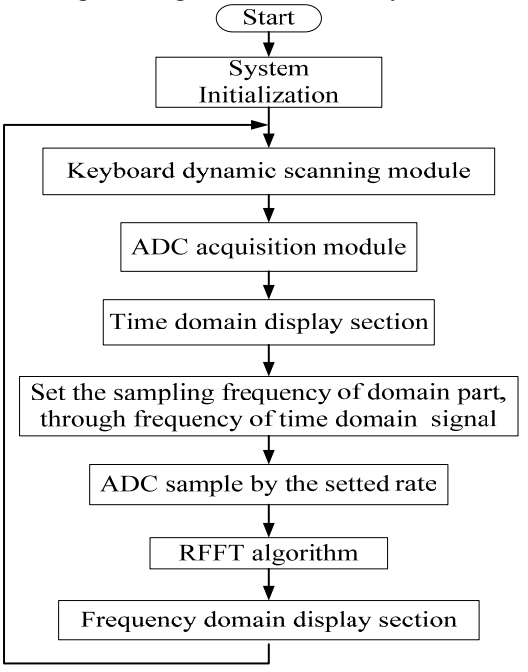

Fig. 4. Software design flowchart of program controlled frequency spectrum analyzer

From Figure 4 we know that, firstly, the system initializes, secondly, perform dynamic keyboard was scanned, then the waveform of ADC sampling and time-domain were displayed, the sampling frequency of frequency domain portion according to the time-domain signal frequency was setted that LCD displayed, ADC sample was taken using the previous setted frequency, the sampled data by FFT optimization algorithm

was processed, the corresponding parameters were obtained ,finally, the processed data was displayed on LCD.

5.1. ADC Sampling module

DSP internal integrated ADC is the bridge connected with external analog signal, the clock must be setted below 12.5MHz, or the data of ADC conversion would be unstable. In this paper, the ADC clock setted at 12.5MHz,triggered by software, controlled the sampling rate of ADC with timer 0. ADC acquisition module flowchart of Frequency domain shown in Figure 5.

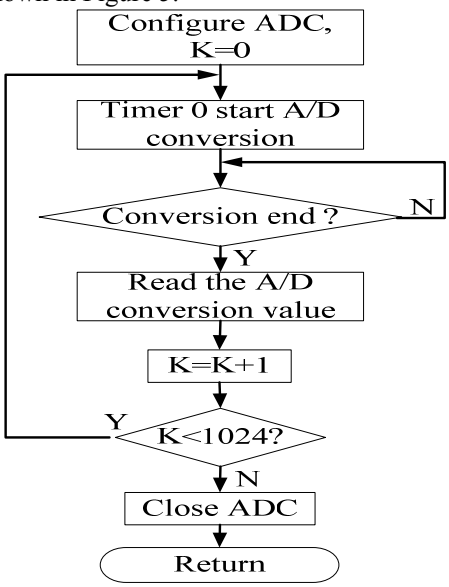

Fig. 5. ADC acquisition module flowchart of Frequency domain

5.1.1 Accuracy of ADC sampling

It is 12 bit that the ADC integrated inside DSP, but the actual sampling number is less than 10,the sampling precision is very low. To obtain a higher sampling precision, we need to separate the digital power design and analog power design. To avoid the digital signal line we connected the ADCINxx pin, and we use external reference.

5.1.2 Frequency of ADC sampling

In this design, ADC sampling frequency is divided into the time domain and frequency domain. Time domain sampling rate sets as:500Hz,1KHz,5KHz,10KHz,50KHz,100KHz,500KHz and 1MHz. System works at 1KHz initially, displayed according to the graphics, adjusted the sampling frequency using the keys of instrument.

In the frequency domain signal analysis, considering the spectral resolution , LCD resolution, spectral leakage ,finally we selected the sampling points 1024,the grade of sampling frequency setted according to an integer multiple of the sampling points (or divisibility).In this way, we can guarantee sampling the general

signal periodically, reducing the spectrum leakage of test signal, getting better spectral waveform. Specifical Classification shown in Table 1.

Table 1. ADC sampling frequency level setting in frequency domain

f_1 /Hz （Signal to be measured）	f /Hz (Sampling Frequency）	Resolution Δf /Hz
[10,500）	1024	1
[500,1000）	2048	2
[1000,2000）	4096	4
[2000,4000）	8192	8
[4000,5000）	10240	10
[5000,10000）	20480	20
[10000,20000）	40960	40
[20000,40000）	81920	80
[40000,50000）	102400	100
[50000,150000]	819200	800

Obtained from Table 1,the spectrum minimum resolution of our design is 1Hz, signal bandwidth is 150KHz.

5.2. RFFT Algorithm module

This design uses the original library file CCS, sets the sampling points to 1024,Specific steps of using FFT library[6] as follows:

(a)512-point plural sequence is Combined by the 1024-point real sequence, then the reverse sequence operations of the plural sequence is completed.

(b)512-point complex sequence is treated with window (hanning), then the 512-point plural sequence are calculated by FFT .

(c)Splitting and reduction, the result of 1024-point real sequence calculation is obtained by radix-2 FFT .

(d)the amplitude spectrum of frequency spectrum is obtained by squared the real and imaginary of real sequence that processed with FFT and then prescribing.

FFT library includes CFFT32 module, it provides 128,512,1024 points FFT calculation module, while defined all the used variables and functions to the CFFT32 module, which make the interface of FFT simple, and facilitate to call the FFT[7].Module structure of the CFFT32 is:

```
typedef  struct {
    long *ipcbptr;
    long *tfptr;
    int size;
    int nrstage;
    long *magptr;
    long *winptr;
    long peakmag;
    int peakfrq;
```

```
    int ratio;
    void (*init)(void *);
    void (*izero)(void *);
    void (*calc)(void *);
    void (*mag)(void *);
    void (*win)(void *);
    }CFFT32;
```

FFT module initialization procedure is:

```
Void  FFT_config(void)
{
   fft.ipcbptr=ipcb;
   fft.magptr=ipcb;          //Result is stored in the same area
   fft.init(&fft);
}
```

FFT calculation module program as follows:

```
void Compute_FFT(void)
{
   RFFT32_brev(ipcb,ipcb,N);//Bit reverse
   fft.calc(&fft);//RFFT calculate
   fft.split(&fft);//Splitting and reduction
   fft.mag(&fft);
}
```

The format of calculated signal amplitude is Q30 data, it is the true magnitude of the signal that the calculated data divided by 2 to the 30th power and converted to a decimal value, while the real signal frequency also got by processing the signal frequency further. We can obtained the true frequency of the signal by calculated according to the following formula.

$$f_{real} = n \times \Delta f = n \times f_{sample} \Big/ N \tag{9}$$

Where n is the number on the spectrum line , f_{sample} is the sampling frequency , N is the number of sample .

6. System Testing

To test the performance of the measurement system, we need take the steps as follows:

Firstly, according to the table 1,sampling the test signal in all range of the Frequency bands by ADC. Secondly, processing the sampled data by RFFT algorithm. Finally, tabulating the test results. Figure 6 is a field test pattern of the system, Table 2 is the specific test results.

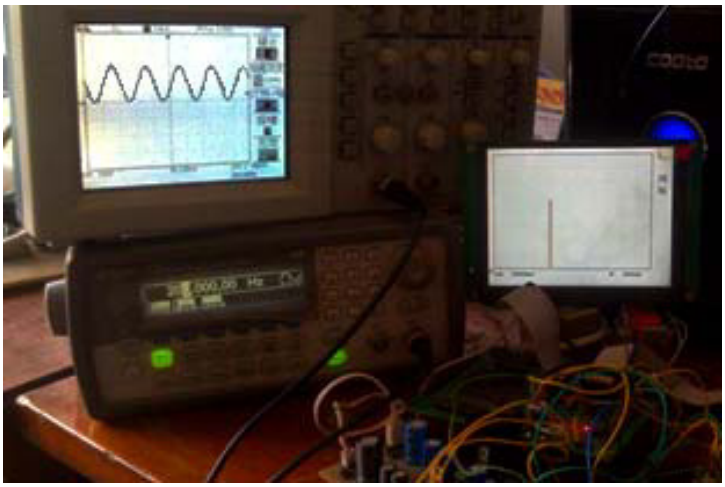

Fig. 6. Field test plots of the test system

Table 2. measurement of the test signal amplitude over the bandwidth

/Hz（Frequency of test signal ）	/V（Inputs of test signal ）	/V（Measurements of test Signal ）	/dB (error amount)
[10,500）	1	About 0.980	-0.175
[500,1000）	1	About 0.980	-0.175
[1000,2000）	1	About 0.980	-0.175
[2000,4000）	1	About 0.980	-0.175
[4000,5000）	1	About 0.980	-0.175
[5000,10000）	1	About 0.980	-0.175
[10000,20000）	1	Range 0.990~0.960	-0.087~-0.355
[20000,40000）	1	Range 0.980~0.960	-0.175~-0.355
[40000,50000）	1	Range 0.990~0.920	-0.087~-0.724
[50000,150000]	1	Range 0.940~0.925	-0.537~-0.677

From the test results of Table 2 we know that , the calculated signal amplitude of the design is relatively stable in the frequency range of 10Hz ~ 150KHz, the maximum error is -0.724dB. The flat of the design is better in the entire bandwidth range , the error is bigger when the measuring signal amplitude between 40KHz to 150KHz, and the fluctuation is more obvious . From test signal spectrum , we can see some frequency spectrum leakage of the signal .Since the design uses a reasonable set of sampling points and frequency, we can sampling the general signal periodically in theory and avoid leakage phenomenon as far as possible. After a data analysis of the test frequency in the range 40KHz ~ 150KHz, we find the error of test signal amplitude mostly comes from the systematic errors of the design.

7. Conclusions

Use the method of signal distortion measurement which proposed in this paper, design and develop the signal distortion measurement system with optimized FFT algorithm, the results show that by field test, this method is a feasible one for measuring. To some extent, it is achieved remarkable results on the inhibition of the spectrum leakage phenomenon, and improved the accuracy of measurement. At the same time, the signal distortion measuring instrument which use the proposed method has the advantages like easy to make, low cost and easy to carry, solve the inconvenience status of field test in engineering applications. This method has a good practical application prospects.

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References

[1] Wu Xiaochun. The algorithm and Application of the real sequence FFT[J] : Automation & Instrumentation, 2010,151(5):81-82.Reference to a book:
[2] Design and realization of real FFT based on DSP[J]:Journal of Dynamics and Control,2005,6,3(2),50-53.
[3] LiuCui, XiongWenjun, ZhengWenxu. Frequency Counter for Complex Frequency Signal based On TMS320F2812 [D]:(TI Contest Papers).Hefei: Hefei University of Technology，2010.
[4] High Performance AUDIO OPERATIONAL AMPLIFIER(OPA2134).
[5]SINGLE-SUPPLY, RAIL-TO-RAIL，OPERATIONAL AMPLIFIERS(OPA340)
[6] Wuhan Zhongxian Technology CO.,TFT Serial of Bus Color LCD user manual.
[7] Yin Yong, Ou Guangjun, Guan Rongfeng.DSP integrated development environment CCS Guide[M].Beijing: Beijing Aerospace University Press,2003.
[8] Cheng Peiqing. Digital signal processing tutorial[M].Beijing: Tsinghua University Press,2007.
[9] Sun Liming.TMS320F2812 principle and C language program development[M].Beijing: Tsinghua University Press,2008,12.
[10] TMS320F2808, TMS320F2806, TMS320F2801,Digital Signal Processors//www.ti.com.