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A Space Vector Pulse Width Modulation Approach for DC Link Voltage Balancing in Diode-Clamped Multilevel Inverter

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Abstract

This paper presents a generalised SVPWM technique –named *Nearest Three Vector and Selected Three Vector* – (NSTV) to control DC-link imbalances in the three-level NPC-MLI, which is one of the main drawbacks. The proposed scheme is a result of the blend of the techniques Nearest Three Vector (NTV) and Selected Three Vector (STV). This scheme can maintain DC-link voltage within a specified tolerance value with any modulation index or a wide range of load variation. The results of the proposed scheme exhibits DC-link voltage variation within 0.25% which well below the acceptable limit. The scheme guarantees to achieve voltage balancing without any additional control. The benefits of the proposed solution over existing schemes are verified through the MATLAB simulation and tested for the proto type MLI designed with the novel SVPWM implemented in FPGA- SPARTEN III.

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1. Introduction

Multilevel inverters (MLI) were proposed by Nabae.A (Nabae.*A. et.al*, 1981). MLI offers a set of features that are well suited for HVDC transmission, reactive power compensating devices, power conditioning and so on (Marcelo *et.al,* 2012; Saeedifard.M .*et .al,*2009; S.Busquets-Monge *et .al,* 2004;). Multilevel inverters have been classified as Diode clamped inverter, Capacitor Clamped inverter, Cascaded MLI and Hybrid type inverter (Rodriguez, J.S *et .al,* 2010). NPC-MLI in Fig.1 suffers from the DC-link imbalance problem due to the dc link capacitors; magnitude of this problem increases with the increase in number of levels. The DC-link imbalance degrades the operation of the inverter by increasing the voltage stress on the semiconductor devices, introducing harmonics and distorting the output voltage.

The neutral point balance can be achieved by using an algorithm to switch the inverter with proper switching states such that the DC-link balancing is achieved. Josep Pou *et .al* have used stationary feed forward SVPWM for D.C-link balancing, in which the duty cycle calculations involved are more complex. A new modulation approach for complete control of DC-link balancing in 3-level 3-phase NPC VSI has been proposed based on the virtual vector concept, which guarantees the balancing of DC-link voltage for any load over the full modulation range (*Jian-Yong ZHENG et.al,* 2010). However this method has only been implemented using carrier based PWM which involves the calculation of angles and trigonometric ratios. A complete control has been obtained in the 3-level 3-phase NPC inverter (*Amit Kumar Gupta et.al*, 2007). This scheme fully dependants on modulation index and reference vector angle.

In this paper, a novel SVPWM *Nearest Three Vector and Selected Three Vector* (NSTV) strategy is proposed. The crux of the scheme is ingenious usage of Nearest Three Vector (NTV) and the Selected Three Vector (STV) to bring the DC-link voltage fluctuations below the tolerated value. The presented solution is capable of eliminating the low frequency dc-link capacitor voltage oscillations and guarantees balancing of dc-link voltage in 3-level NPC-MLI over the full range of modulation (Modulation index > 0.5). The improvement in npf through proposed SVPWM is much pronounced for higher modulation range than the lower. The scheme is simulated and conceptual feasibility is thoroughly understood using MATLAB software. Later the strategy is coded, synthesized and downloaded in FPGA- SPARTEN III.

2. Traditional Space Vector PWM Strategy

The SVPWM treats sinusoidal voltage as constant amplitude vector rotating at constant frequency with reference voltage vector V^*, defined by $V^*=|V^*|*e^{jwt}$, rotates around the centre of the space vector (SVM) diagram at an angular frequency $\omega=2\pi f_{sys}$ (e.g.f_{sys}=50 Hz).The 3-phase 3-level space vector diagram illustrated in Fig.2. The rotating reference vector V^* lies in any of the sector inside that 4 sub-triangles are available. The three vectors of the corresponding triangle can be used to synthesise the sampled reference voltage vector.

$$V *\delta S_1 + V* \delta S_2 + V* \delta M_1 = V* \qquad (1)$$

$$\delta_{S1} + \delta_{S2} + \delta_{M1} = 1 \qquad (2)$$

The algorithm for multi-level SVM is to be implemented by the following steps: Location of the sector and the triangle inside which the tip of the reference vector lies; Selection of the adjacent switching vectors; Calculation of the duty cycles of the switching vectors; Calculation and application of the switching pattern.

3. Influence of switching vector for DC-link imbalance

3.1DC-link capacitor balancing problem with respect to phase current

While using large, zero vectors the phase currents become zero and hence the balance could be obtained.

DC-link imbalance is mainly due to medium vectors, because the phase currents are not zero in those vectors. Due to the existing phase currents, capacitor balance cannot be achieved. The capacitor can be balanced by proper utilization of the short, zero and large vectors without medium vectors (du Toit Mouton.H *et .al,* 2002).

3.2 DC-link capacitor balancing problem with respect to modulation index

For the linear modulation region, there are three modes; (i) ($0 \leq m < 0.5$) in this, the active vectors are the short vectors and the balance is achieved undoubtedly, (ii) ($0.5 \leq m < 0.8$) the active vectors are medium and short, where balancing becomes poor, (iii) in higher modulation ($0.8 \leq m < 0.907$), the participation of the medium vector is maximum and it can compensate the short vector as the DC-link capacitor imbalance is high (S.Busquets-Monge *et .al,* 2004;). At higher modulation, the reference vector lies in Δ_1, Δ_2 and Δ_3 and results in imbalance. The Fig.3 shows that npf against various triangles of sector1.
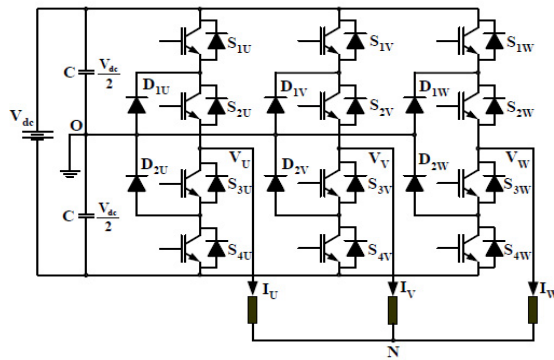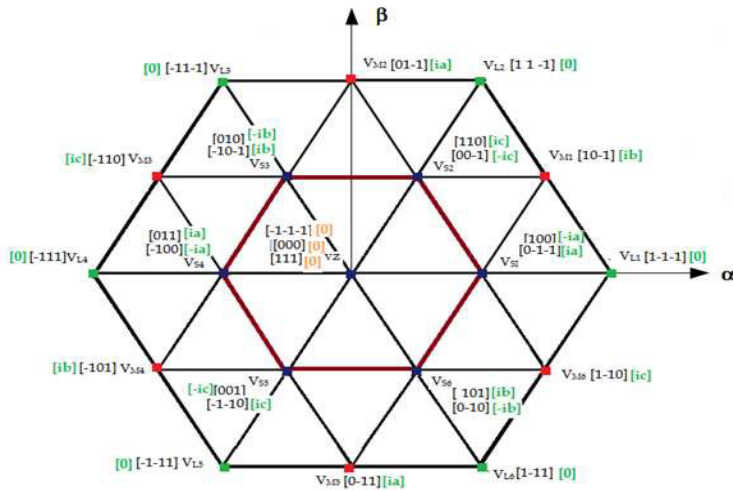

Fig.1 Circuit diagram for 3-level NPC-MLI

Fig.2 Space Vector Diagram of NPC-MLI

4. Problem identification

The major problem in the NPC-MLI is DC-link balancing. The DC-link balancing can be defined as

$$Percentage\ of\ DC\text{-}link\ imbalance = \left\{ \left(V_{dc\text{-}link}/\ n\text{-}1 - V_{c2} \right) / V_{dc\text{-}link}/\ n\text{-}1 \right\} *100\ \% \tag{3}$$

4.1 Nearest three vector (NTV) scheme

When the reference V* lies in the Δ_2, it can be synthesized by using the nearest vectors $V_M, V_{SI,}$ and V_{S2}, which is termed as NTV scheme. Similarly the reference V^* can lies in any of the triangles Δ_2-Δ_4 and it is synthesized by using the corresponding nearest vectors. The triangle where the reference vector is located can be identified by Δ_j by the general implementation of the SVM scheme. Once the triangle identification was done then that particular triangle is treated as sector of a virtual 2-level inverter and the suitable vertex of the triangle can be taken as the zero vector. The tip of the reference vector with respect to shifted vector is represented as (Vα, Vβ). The duty ratios are

$$\delta_{VS1} = V_\alpha - V_\beta/\sqrt{3} \tag{4}$$
$$\delta_{VS2} = 2 - 2V_\alpha \tag{5}$$
$$\delta_{VL2} = 1 - \delta_{VS1} - \delta_{VS2} \tag{6}$$
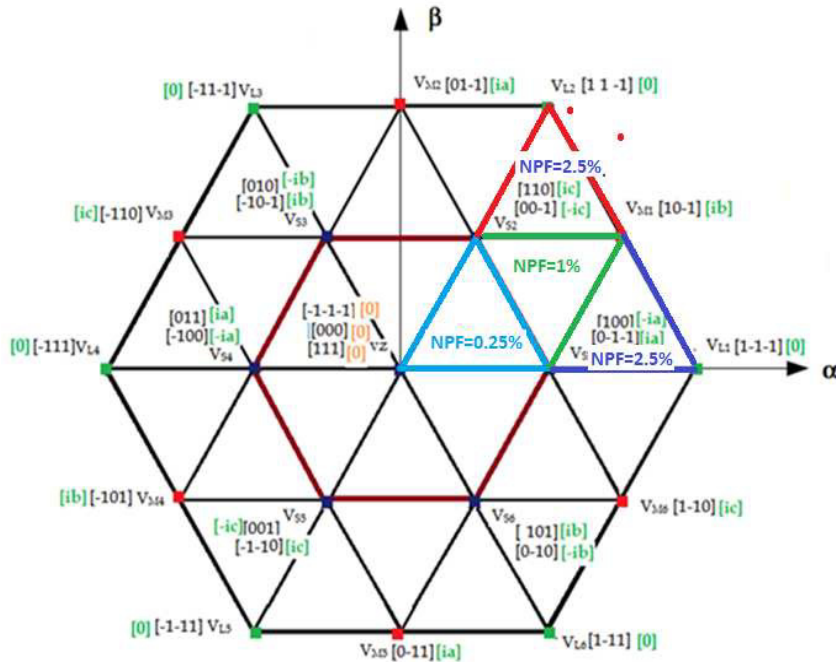

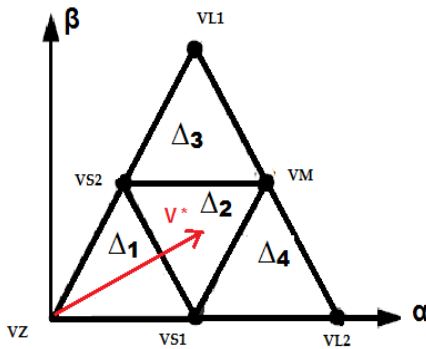Fig.3 Phase currents according to 3 level SVPWM
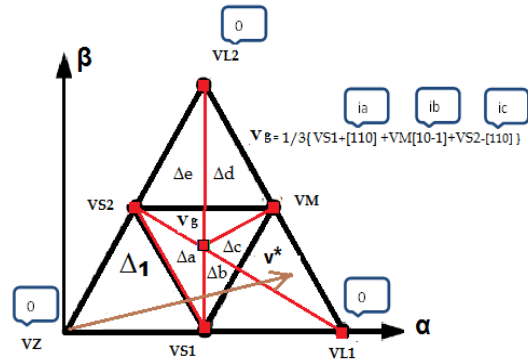
Fig.4 Sector 1 for NTV scheme   Fig.5 Sector 1 for STV scheme

The equations (4)-(6) can be applicable for any triangle. When the control lies within the Δ_2, the vectors V_{SI} V_{MI} and V_{S2} are switched with redundant states.The states(110),(10-1),(100),(00-1), (10-1),(0-1-1) are used with the duty ratios δ_{S1+}, δ_{S2-}, δ_{M1}, δ_{S2+} and δ_{S1-}. Here, $\delta_{S1+} + \delta_{S1-} = \delta_{S1}$ & $\delta_{S2+} + \delta_{S2-} = \delta_{S2}$. So, by controlling duty cycles δ_{S1} & δ_{S2}, the npf can be controlled (*Amit Kumar Gupta et.al, 2007;J.H.seo*)

4.2 Selected three vector (STV) scheme

Once modulation index goes beyond 0.5, then because of the medium vector arrival the capacitor gets imbalanced. So as to reduce the influence of the medium vector contribution in SVM for each sector the ground vector(V_g), is introduced. The 'V_g' lies at an equal distance from V_{s2}, V_{s1} and V_M. V_g can be defined as the mean of the contribution of the vectors V_{s1}, V_{s2} and V_m and Eq. (7) is in accordance. V_g will never induce the D.C-link imbalance as it causes almost zero phase current. To find STV, consider sector1. Now by joining V_{L2} and V_{S1}, V_{L1} and V_{S2}, and V_g and V_M, 5-new triangles are created and named as $\Delta_a(V_{S1}\ V_{S2}\ V_g)$, $\Delta_b(V_{S1}$ $V_{L1}\ V_{S2})$, $\Delta_c(V_{S1}\ V_{LI}\ V_{L2})$, $\Delta_d(V_{S2}V_{L1}V_{L2})$, and $\Delta_e(V_{L2}\ V_{SI}\ V_{S2})$ as evident in Fig.5. Here only the short and large vectors are utilized, the medium vectors are neglected to reduce DC-link imbalance .

$$V_g = 1/3(\ V_{SI+}\ (110)\ +V_M\ (10\text{-}1)+V_{SI-}\ (110)) \qquad (7)$$

Table.1 Proposed selected vector SVPWM scheme for 3 level NPC-MLI with their corresponding currents

Sector	Region	Short vectors	Large vectors
1	$\Delta_b(V_{S1}\ V_{L1}\ V_{S2})$	[100](-i_a)-[0-1-1] (i_a)-[110](i_c)-[00-1] (- i_c)	[1-1-1](0)
1	$\Delta_c(V_{S1}\ V_{L1}\ V_{L2})$	[100](-i_a)-[0-1-1] (i_a)	[1-1-1](0)-[11-1](0)
1	$\Delta_d(V_{S2}\ V_{L1}\ V_{L2})$	[110](i_c)-[00-1] (- i_c)	[1-1-1](0)-[11-1](0)
1	$\Delta_e(V_{S1}\ V_{S2}\ V_{L2})$	[100](-i_a)-[0-1-1] (i_a)-[110](i_c)-[00-1] (- i_c)	[11-1](0)

Triangle determination & duty cycle calculations:
There are two standard techniques used to determine the triangle in which the reference point V^* lies, Case (i) The reference V* makes an angle less than 30° with the α- plane, if the tip of the reference V* lies within the triangles Δ_b or Δ_c.Then the reference point is divided in the ratio 2:1. The V* is $V_\alpha + \sqrt{3}V_\beta \leq 2$ then the point lies in Δ_b. On the other hand if the reference point is $V_\alpha + \sqrt{3}V_\beta < 2$ then V* lies in the Δ_c. Case (ii) The reference V* makes an angle greater than 30° with the α- plane, if the tip of the reference point is within the triangles Δ_e or Δ_d, then similar to the case.1 the triangle can be identified. For example the reference point lies in the Δ_b, if both the inequalities $\alpha \leq 30°$ and $V_\alpha + \sqrt{3}V_\beta \leq 2$ are satisfied. Based on the region duty cycle is calculated

5. Simulation result

The performance of the proposed SVM have been simulated by MATLAB 11.b for 12 switch NPC-MLI with 200V DC-link, two 100µF capacitor, 5kHZ switching frequency fed 1 HP squirrel cage 3-phase induction motor open loop v/f control drive.Fig.6 (a) shows the phase voltage for NTV scheme. The Fig.6 (b) shows the voltage imbalance using the NTV scheme at modulation index 0.9; the capacitor voltage V_{c2} is about 91.9V. Hence using Eq.(3), the npf value of 2% is obtained. Fig.6 (c) shows the phase voltage for proposed NSTV scheme. In Fig.6(d) give voltage across the capacitor using proposed NSTV scheme for the modulation index 0.9, which results the npf values as 0.2% .Here the proposed NSTV scheme limits the DC-link imbalance value to 0.2%, which is well below the IEEE standard of 1% (Nomura s et .al, 2005)
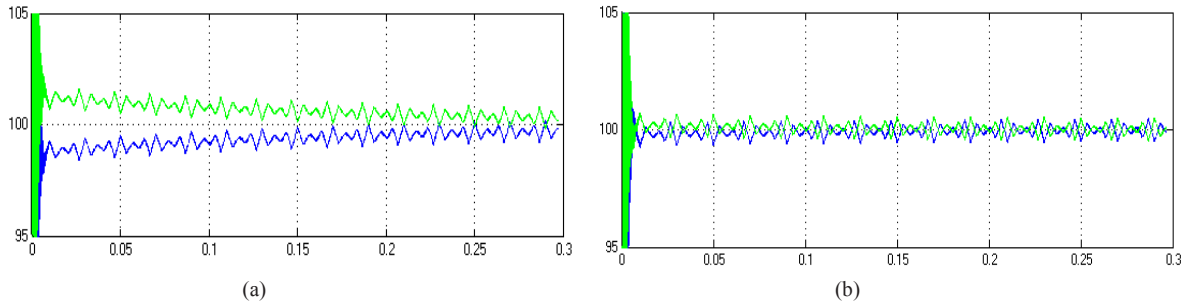

(a)　　　　　　　　　　　　　　　　　　　　(b)

Fig.6 Simulation result in Matlab 11.b for 3-level inverter with SVM based NTV scheme with Modulation Index = 0.907, f = 50Hz, C_1= C_2= 100µF (a) DC link capacitor voltages V_{c1} &V_{c2} for NVT –SVM Scheme , npf 2 %(b) DC link capacitor voltages V_{c1} &V_{c2} for Proposed NSVT –SVM scheme

6. Experimental result

The proposed algorithm is programmed in Verilog Hardware Descriptive Language (VHDL) code and synthesized in minimum computational load using SPARTAN –III - 3AN –XC3S400 FPGA family board.
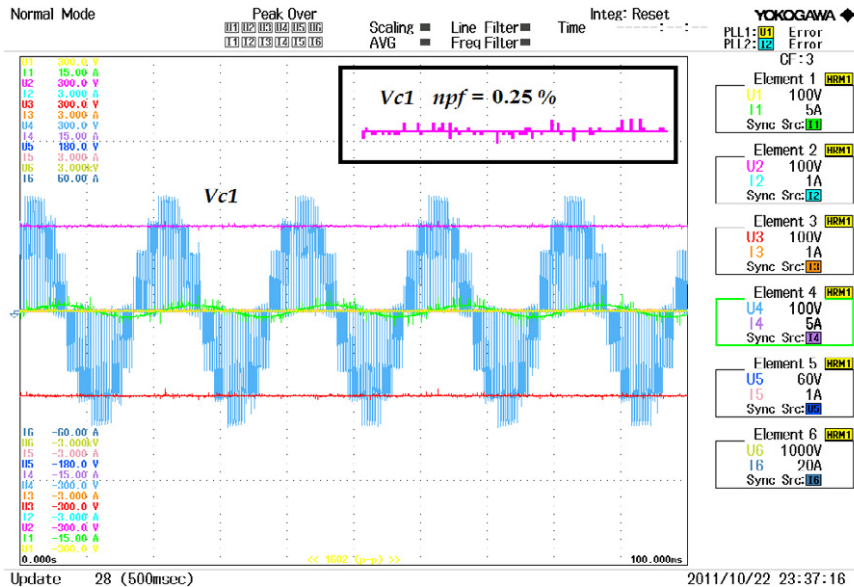
(a)

The SVM modulator duty-ratio information is calculated and pulse is generated through FPGA. The NTV and STV switching sequences are mapped by using the 2D- look up table. The algorithm is tested experimentally on a 3-level NPC laboratory prototype inverter with 200V DC-link, two 100μF capacitor, 5kHZ switching frequency fed 1 HP squirrel cage 3 phase induction motor open loop v/f control drive. The corroborating experimental results are captured using 6 channels YOKOGAWA digital signal oscilloscope (DSO). Fig.7(a)and Fig.7(b) shows the output voltage of the inverter, npf (0.25 %) and THD for the proposed NSTV scheme. Note this Experimental npf value is little differs from simulation platform result for the same system parameters; because of real capacitors will not have the same discharging in nature
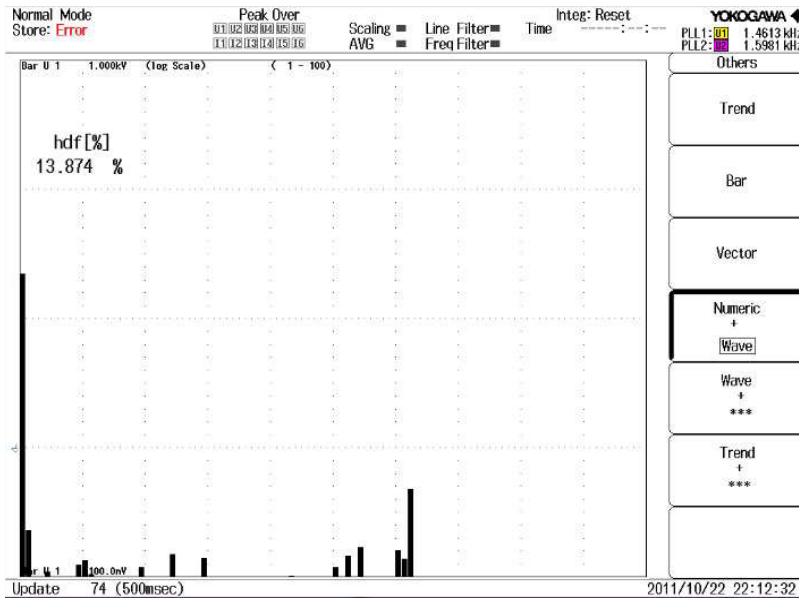

Fig. 7(a). Experimental results for i [15 A/div], V_{c1} and V_{c2} [100 V/div], output voltage v [150 V/div], and V = 200V, m = 0.907, f = 50Hz, $C_1 = C_2 = 100$μF 7(b) THD spectrum for proposed NTV-SV PWM, f = 5 kHz

7. Discussion

Fig.8 depicts the percentage npf verus modulation index for different schemes.For the modulation index (0<m≤0.5),the NTV scheme is medalist in reducing the npf problem. If the modulation index is beyond 0.5, due to the participation of medium vector the npf increases and hence the NTV scheme is not preferable.Therefore for the modulation index (m≥0.5), the STV scheme is used to limit the npf.
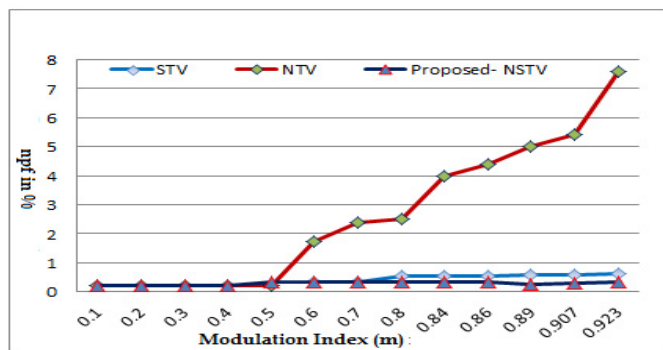
Fig.8 Percentage npf versus Modulation index comparison

8. Conclusion

A novel SVPWM modulation approach for control the DC-link voltage in the 3-phase 3-level NPC VSI is presented. The proposed NSTV scheme maintains the DC-link imbalance within a specified tolerance value. The balancing of the DC-link voltage is achieved irrespective of load condition and over the full range of inverter output voltage. Thus, the proposed NSTV scheme limits the DC-link imbalance value to 0.25%, which is well below the IEEE standard requirement of 1% (Nomura S *et .al,* 2005). The scheme significantly reduces the size of the dc-link capacitors.

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