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Design and Implementation of SORIGA-optimized Powers-of-two FIR Filter on FPGA

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Abstract

With the introduction of sophisticated algorithms, the field of signal processing has experienced enormous diversification of late. In addition to this, design of hardware efficient digital systems has grown sufficient interest amongst the researchers in recent past. In this article, an attempt has been made to realize hardware friendly powers-of-two FIR filter by using an evolutionary computation, called Self-organizing Random Immigrants Genetic Algorithm (SORIGA). In connection to this, this work makes one comparative study amongst various multiplier-less FIR filters in terms of hardware complexity when implemented on an FPGA chip. Finally, supremacy of the proposed design has firmly been established by comparing its hardware cost with many of the state-of-the-art powers-of-two FIR filters.

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1. Introduction

Implementation of a general purpose multiplier in an FIR or IIR structure by means of Very Large Scale

Integration (VLSI) technique is becoming a very complicated and costlier task to be performed. This problem may be solved by considering multiplication operation as repeated addition and hence substituting the filter coefficients as sequence of shifts and additions. These multiplier-less filters are less power hungry and require less hardware blocks for its implementation [1-2]. In connection to this, SPT representation of filter coefficients is very much popular where the effect of multiplier is substituted by means of adders and delay elements only [3-8].

Several algorithms have been proposed so far in the literature where each of which deals with the powers-of-two design of FIR filter. These include traditional techniques like mixed integer linear programming [9], polynomial time algorithm [10], discrete semi-infinite linear programming [11], branch & bound technique [12] and so on. Recently, the domain of circuit and system design has been noticeably influenced by means of a variety of intelligent optimization techniques of current interest like Genetic Algorithm (GA) [13], Orthogonal Genetic Algorithm (OGA) [14], and Differential Evolution (DE) [15-16] and so on.

In this communication, we have employed Self-organizing Random Immigrants Genetic Algorithm (SORIGA) for the design of multiplier-less low-pass FIR filters. Designed filter has been implemented on real time hardware and the requirement of resulting hardware blocks like digital gates, latches, buffers and so on has been calculated using XILINX Design Suite 12.3 software.

2. Design Strategy

2.1. Theoretical background of multiplier-less FIR filter

System function $H(z)$ and the corresponding transfer function $H(e^{j\omega})$ of any causal FIR filter of length L with impulse response $h(k)$ can simply be written in accordance with the following equations [1-2]:

$$H(z) = \sum_{k=0}^{L-1} h(k)z^{-k} \quad (1)$$

$$H(e^{j\omega}) = \sum_{k=0}^{L-1} h(k)e^{-j\omega k} \quad (2)$$

Filters, in which multiplication operation is carried out by means of shifting and addition, will be characterized by its impulse response as outlined below [2]:

$$h(k) = \sum_{m=0}^{\Delta-1} b_{mk} \cdot 2^{-m} \quad \forall k = 0, 1, 2, \dots, L-1 \quad (3)$$

For binary representation scheme, b_{mk} may assume a value from the set $\mathbb{B} = \{0, 1\}$ and Δ signifies the precision of an individual coefficient and formally known as word length of the filter coefficient. Response of such a filter due to an excitation $x(n)$ is given by

$$y(n) = \sum_{k=0}^{L-1} h(k) \cdot x(n-k) \quad \forall n \quad (4)$$

In order to compute the output of this filter at any instant n ; at most L multiplications and $(L-1)$ additions are required. Substituting (3) into (4), we get

$$y(n) = \sum_{k=0}^{L-1} \sum_{m=0}^{\Delta-1} b_{mk} \cdot 2^{-m} \cdot x(n-k) \quad (5)$$

The parameter b_{mk} does not put any overheads as far as the computational or hardware complexity is concerned since, for every k and m , it keeps the term $2^{-m} \cdot x(n - k)$ intact or make it zero depending upon its assignment over the binary space. The term 2^{-m} , when multiplied with $x(n - k)$, causes the multiplier to get shifted right by m bits. For an input word length of W , allowable maximum word length of the product $2^{-m} \cdot x(n - k)$ thus becomes $(W + \Delta)$. As a matter of fact, resulting complexity from the architecture of full-adder is proportionately related to $(W + \Delta)$ in accordance with equation (5).

2.2. Design of powers-of-two FIR filter using SORIGA

SORIGA [17-18] has been judiciously employed in this work for the synthesis of FIR tap coefficients which are encoded in the form of sum of signed powers-of-two. In connection to this, any arbitrary coefficient $h(k)$ may be represented by means of a binary row vector as shown below:

$$h(k) = [b_{0,k} \ b_{1,k} \ b_{2,k} \ b_{3,k} \ b_{4,k} \ \dots \ b_{(\Delta-1),k}] \ \forall k = 0, 1, 2, \dots, L - 1 \quad (6)$$

In order to synthesize linear phase low-pass FIR filter, tap coefficients are chosen to be symmetric around its central coefficient. Proposed scheme has accumulated all such $\lfloor L/2 \rfloor \cdot \Delta$ which has been regarded as a single chromosome \mathcal{B} in the process of evolutionary computation. Being a population-based algorithm, our design strategy generates \mathbb{P} such chromosomes randomly of length \mathcal{L} which form the pool of potential solution. Based upon the fitness of individual chromosome, subsequent genetic operations like selection, cross-over and mutation are carried out subsequently in accordance with the steps of SORIGA. This has been symbolically outlined as follows:

$$\mathcal{B}^S = \mathfrak{S}\{\cup_{i=1}^{\mathbb{P}} \mathcal{B}_i\} \quad (7)$$

$$\mathcal{B}^C = \mathfrak{C}\{\cup_{i=1}^{\mathbb{P}_C} \mathcal{B}_i^S\} \quad (8)$$

$$\mathcal{B}^M = \mathfrak{M}\{\mathcal{B}_i^C\} \ \forall i = 1, 2, 3, \dots, \mathbb{P}_M \quad (9)$$

Where, the operations of selection, cross-over and mutation are symbolized by \mathfrak{S} , \mathfrak{C} and \mathfrak{M} respectively. Parameter \mathbb{P}_C and \mathbb{P}_M identify the total number of chromosomes allowed to take part in the operation of cross-over and mutation respectively.

Selection of competent chromosomes from the pool of \mathbb{P} such members is executed on the basis of their individual fitness which is considered to be the degree of proximity with the ideal response. Proposed algorithm calculates this fitness as an inverse of the maximum difference between the designed and ideal frequency response of the low-pass filter and makes an attempt to minimize this difference to a significant extent. In this connection, maximum difference over the entire frequency band of interest has been regarded as the cost function of the individual chromosome.

3. Results and Analysis

This section demonstrates the outcome of the proposed algorithm analytically. Since the design incorporates evolutionary algorithm, convergence characteristics of our proposition has been depicted in Fig. 1 below which exhibits the variation of averaged cost function with the number of iterations for three different values of cross-over probability. Size of population has been considered as 100 in the entire analysis.

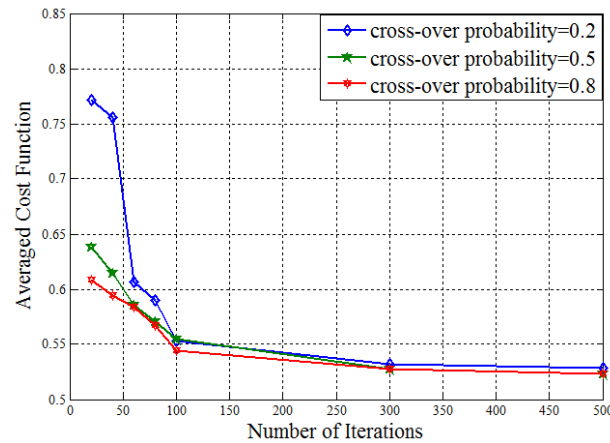


Fig. 1: Convergence characteristics of the proposed scheme

In order to establish the supremacy of the proposed design, frequency response of SORIGA-optimized multiplier-less low-pass FIR filter of order 35 has been compared with few such state-of-the-art filters in Fig. 2 below.

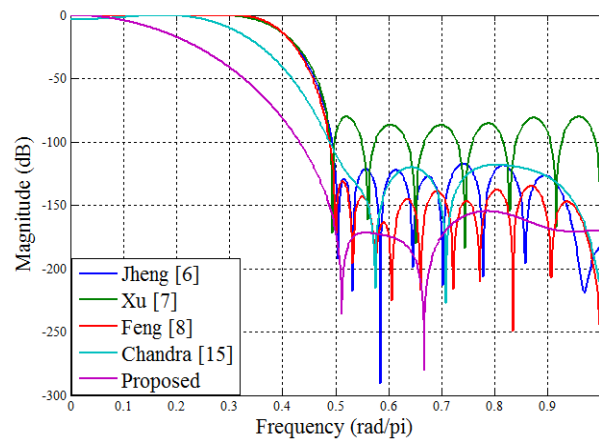


Fig. 2: Comparison in terms of frequency response amongst various multiplier-less low-pass FIR filters

It can be well apprehended from the above comparison that the proposed filter yields more attenuation in transition and stop-band region of frequency characteristics. As for example, at a frequency of 0.65 rad/pi, SORIGA-optimized filter produces an attenuation of about 193.9 dB while the filters designed in [6], [7], [8] and [15] yields approximately 151.6 dB, 180.3 dB, 157.1 dB and 120.6 dB attenuation respectively.

Subsequent part of this section elaborately describes the requirement of different hardware blocks used to realize the powers-of-two filter on an FPGA chip. Quite a few recent algorithms, nurturing the concept of multiplier-less FIR filter design, have also been considered into our analysis and the resulting hardware elements have been listed in Table 1 below. Since the filters designed by means of different algorithms are of

different length; required number of hardware blocks per unit length of the filter has also been included for fair comparison. Word length of input signal has been taken as 8 in the entire analysis.

Table 1 Comparison in terms of hardware elements amongst different multiplier-less FIR filters

Algorithms	Name of the hardware block									
	2-input OR		2-input AND		2-input XOR		Flip flop		I/O buffer	
	Total	Per unit length	Total	Per unit length	Total	Per unit length	Total	Per unit length	Total	Per unit length
Samueli [3]	672	26.88	763	30.52	672	26.88	184	7.36	125	5
Chen [4]	1012	36.143	1134	40.5	1012	36.143	240	8.571	151	5.393
Yao [5]	1395	49.821	465	16.607	1355	48.393	216	7.714	145	5.179
Jheng [6]	1016	35.034	508	17.517	1016	35.034	232	8	153	5.276
Xu [7]	580	20.714	290	10.357	580	20.714	119	4.25	93	3.321
Feng [8]	871	25.618	1163	34.206	1356	39.882	285	8.382	138	4.059
Chandra[15]	530	18.276	531	18.31	352	12.138	65	2.241	128	4.414
Proposed	425	11.806	487	13.528	378	10.5	184	5.111	139	3.861

It can be unambiguously observed from Table 1 that the proposed architecture outperforms most of the state-of-the-art multiplier-less FIR filters by a large margin in terms of the hardware blocks. However, performance of the proposed SORIGA-optimized filter is slightly inferior to that of [7] in terms of 2-input AND, flip-flop and I/O buffer counts. Architecture of the proposed filter as obtained using XILINX Design Suite 12.3 has been depicted in Fig. 3 below.

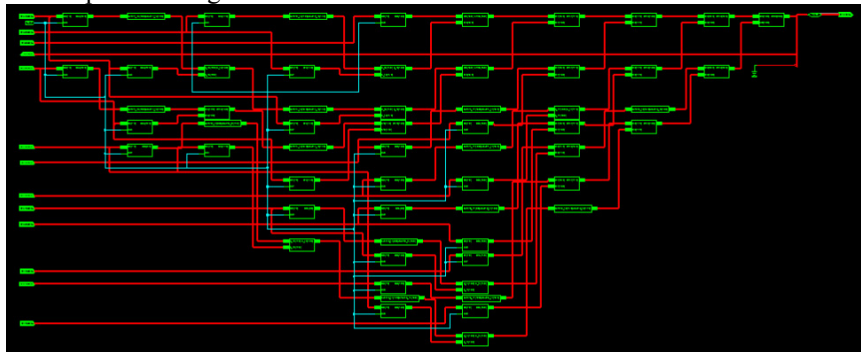


Fig. 3: RTL schematic of the proposed multiplier-less FIR filter realized on FPGA

4. Conclusion

This article deals with design of a multiplier-less low-pass FIR filter has been carried out by means of a recently proposed evolutionary optimization algorithm, called Self-organizing Random Immigrants Genetic Algorithm (SORIGA). Effectiveness of the optimization technique has been evaluated in terms of its convergence speed. Moreover, the supremacy of the proposed design has been established in terms of frequency response of the filter. Furthermore, tap coefficients of the designed filter have been encoded as sums of powers-of-two and implemented on a real time hardware chip using XILINX Design Suite 12.3. It

has been observed that the proposed architecture is superior to other existing design methodologies as far as hardware complexity of the design is concerned. Performance of the solution may further be improved by proper modification of the fitness function of the optimization process as a future scope of this work.

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