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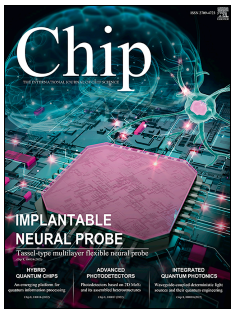

Impedancemetry of multiplexed quantum devices using an on-chip cryogenic CMOS active inductor

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Graphical Abstract

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Highlights

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- Integrated CMOS circuit operating at 4.2 K for the measurement of quantum capacitance at aF-level.
- Novel method of impedancemetry for a resonant circuit with an active inductance connected to a gated quantum device, suitable for the readout of charge and spin qubits.
- Application to individually addressed on-chip nanometric transistors revealing signatures of confined electronic states.
- Advantages with respect to the well-established reflectometry method given by the very-low footprint of the circuit and by the tuning capabilities of the active inductance with respect to frequency and quality factor of the resonator.

Impedancemetry of multiplexed quantum devices using an on-chip cryogenic CMOS active inductor

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Abstract

In the pursuit for scalable quantum processors, significant effort is being devoted to the development of cryogenic classical hardware for the control and readout of a growing number of qubits. In this manuscript, we present a novel approach called impedancemetry that is suitable for measuring the quantum capacitance of semiconductor qubits connected to a resonant LC-circuit. The impedancemetry circuit exploits the integration of a CMOS-based active inductor in the resonator with tunable resonance frequency and quality factor, enabling optimization of readout sensitivity for quantum devices. The realized cryogenic circuit allows fast impedance detection with a measured capacitance resolution down to 10 aF and an input-referred noise of 3.7 aF/$\sqrt{\text{Hz}}$. At 4.2 K, the power consumption of the active inductor amounts to 120 µW, with an additional dissipation for on-chip current excitation (0.15 µW) and voltage amplification (2.9 mW) of the impedance measurement. Compared to commonly used schemes based on dispersive RF reflectometry which require mm-scale passive inductors, the circuit has a notably reduced footprint (50 µm × 60 µm), facilitating its integration in a scalable quantum-classical architecture. The impedancemetry method has been applied at 4.2 K to the detection of quantum effects in the gate capacitance of on-chip nanometric CMOS transistors that are individually addressed via multiplexing.

Keywords: Impedancemetry, Qubit read-out, Cryogenic circuit, Active inductor, CMOS

Introduction

An ingenious use of the laws of quantum mechanics has led to a new computing paradigm, generally known as quantum computing, that promises exponential speed-up in the solution of certain types of problems[1, 2, 3]. Using a prototypical quantum processor with 53 operational superconducting quantum bits (qubits), a ground-

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breaking experiment was recently able to perform a first experiment towards quantum supremacy[4], triggering more extensive research on such a goal[5]. Practical implementations of quantum computing, however, are expected to require much larger numbers of physical qubits[6].

Solid-state implementations seem to offer the best scalability prospects. While superconducting qubits are currently the leading platform, semiconductor CMOS spin qubits are emerging as a serious contender owing to the possibility to leverage the integration capabilities of silicon technology[7]. Very recently, promising developments of spin-qubits in Si/Ge heterostructures have reached a quantum processor of up to 6 qubits [8, 9]. For both superconducting and semiconducting qubits, the quantum processor functions at very low temperature, typically below 0.1 K, but it has recently been shown that silicon qubits can be operated even above 1 K with limited loss of fidelity[10, 11].

In the quest to scale-up to larger numbers of qubits, the use of classical cryogenic electronics positioned as close as possible to the qubits is widely considered a necessity[12, 13]. Various transistor building blocks have been demonstrated at low temperatures to proof their feasibility. These include (de)multiplexers[14, 15], analog-to-digital and digital-to-analog converters[16, 17, 18, 19], low-noise amplifiers[20, 21], RF oscillators[22, 23], and transimpedance amplifiers[24, 25]. More elaborated circuits involving RF Arbitrary Wave Generators have been developed for high-fidelity qubit control, operating at $\sim$4 K for reasons of cooling power [26, 27, 28, 29, 30]. CMOS-based cryogenic controllers operating at $\sim$ 4 K were reported enabling high-fidelity operations on Si electron-spin qubits[31] and on superconducting qubits[32]. In an even more complete approach of the controller, qubit-readout components have been added to the cryogenic circuit[33, 34]. In a random-access strategy with microwave multiplexing of qubits [35, 36], these cryogenic controllers can significantly reduce the number of electrical lines running through the host cryostat, thereby limiting the associated heat load.

Measuring the qubit state involves detecting small capacitance variations in the impedance of an LC tank circuit coupled to the qubit, which is commonly done through RF reflectometry. The inductive element of this tank circuit is typically made up of a surface-mount inductor or a microfabricated superconducting coil. Even for this second case, the corresponding footprint is relatively large ($\sim$mm^2) compared to the qubit size ($\sim$100 nm) and hence hardly compatible with large-scale qubit integration.

In this work, we propose to use an alternative readout technique called impedancemetry for measuring the impedance of the LC tank at resonance, which in our case is around 200 MHz. Unlike the reflectometry method based on traveling wave analysis where 50 Ω impedance matching plays a crucial role in achieving optimal sensitivity, the proposed impedancemetry method relies on the direct impedance measurement of a resonant circuit containing the capacitance to be measured through the locally applied currents and detected voltages. As an essential difference with reflectometry, the sensitivity of impedancemetry depends much less on the 50 Ω matching criterion for the measured value of the impedance of the resonant circuit.

To minimize the surface of the cryogenic readout circuit, we used a CMOS-based active inductor in the LC resonator. The reduced footprint of the CMOS inductor allows for scalability and enables adjustments of the characteristic frequency and quality

factor of the resonator, which is crucial for optimizing measurement sensitivity in terms of signal-to-noise ratio (SNR). Besides the performance of the active inductor in terms of noise, also the power consumption forms an important issue in the evaluation of the proposed cryogenic CMOS inductor. The circuit is completed with an RF current source exciting the LC tank containing the capacitor of the Device Under Test (DUT) and an amplifier to read the voltage response of the resonator. We characterized the circuit sensitivity and tunability at 4.2 K with an addressable capacitor bank demonstrating its capability to measure capacitances as low as 10 aF. Finally, the proposed approach has enabled in-situ impedancemetry measurements of the capacitance of individually addressed gate-coupled transistors. The observed oscillatory signals in the gate capacitance demonstrate the capability to measure quantum phenomena with an on-chip resonator composed of active inductance and nanometric transistor.

Impedancemetry

Capacitive spectroscopy of gate-controlled quantum-dot devices as shown in Fig. 1 allows the detection of electronic quantum states within the structure, including the firstly occupied electron states. For enhanced detection sensitivity at high speed, the gate capacitance of the device under test (DUT), represented as a single-electron transistor in Fig. 1b, is connected to an inductance to form an LC resonator. In a gate-coupled read-out scheme of the quantum state, the response of the tank at cryogenic temperature excited near resonance frequency f_r is probed and analysed at room temperature, usually with homodyne I-Q detection. The phase change $\Delta\phi$ of the tank response becomes an image of the change in DUT capacitance $\Delta C \ll C_p$ (see Fig. 1a) through the relation $\Delta\phi = Q\Delta C/C_p$ around f_r with Q the resonator quality factor and C_p the parallel (parasitic) capacitance.

Fig. 1b shows a schematic comparison of qubit resonance experiments between reflectometry and the newly proposed method of impedancemetry. The commonly used reflectometry uses voltages to excite and probe the resonator via the scattering[37] or transmission[38] of the propagating waves. To isolate the incoming and outgoing signals, directional couplers or circulators are used.

The impedancemetry approach for qubit detection uses currents to excite the resonator and measures the impedance without the requirement of bulky RF elements. The incoming signal V_{in} at the resonant frequency f_r, generated at room temperature, is converted in a current $I_{in} = G_m V_{in}$ with a voltage-controlled current source of transimpedance G_m at the base temperature. The input current I_{in} creates a voltage $V_{out} = Z_r I_{in}$ through the tank impedance Z_r that carries the information about the DUT capacitance. V_{out} is conveyed to a low-power unity-gain amplifier (follower) which should be placed as close as possible to the DUT to reduce parasitic capacitance C_{par}. As usually done, the main amplification is placed at a higher temperature (typically 4.2 K) to benefit from higher cooling power. Note that, compared to the schematic layout of Fig. 1b with the DUT at sub-Kelvin temperatures, the resonator and DUT of the realized circuit are all on-chip, together with current excitation and amplification stage for the impedancemetry measurements performed at 4.2 K.

Impedancemetry has the advantage over reflectometry that the 50 Ω impedance matching plays no role in the optimization of the resonant circuit depending on the in-

ductor and the parallel (parasitic) capacitors. However, the cryogenic circuitry required by impedancemetry generates extra noise compared to reflectometry, which needs to be minimized. The impedance of the resonator naturally filters out-of-resonance components (see Fig. 1a) such as low-frequency flicker noise from electronics. In the perspective of quantum computing involving a qubit matrix, V_{in} could contain a comb of excitation frequencies to excite a set of frequency-selective resonators.

In the Supplementary Material I a comparison is made between reflectometry and impedancemetry with respect to the scaling with the number of qubits for a $N \times N$ array. The footprint of the reflectometry circuit is dominated by the directional coupler occupying approximately 1 cm^2 (for frequencies below a few GHz) which in the transmission variant of reflectometry would be replaced by the doubled footprint of the in- and output connectors (0.1 cm^2). The passive micro-Henry inductance, which is about 1 mm^2 (below a few GHz), dominates the footprint of the impedancemetry circuit.

The connection fan-out of a qubit matrix, originating from objects of different scale, increases the average interconnection length and thus lowers the detection sensitivity with important parasitic capacitance. The applied high magnetic field ($\sim 1\,T$) required to separate spin states via the Zeeman effect prevents an effective use of ferrite materials for reducing the inductance size.

The chosen implementation of an active inductance consisting of transistors and capacitors enables an inductance density as high as a few mH/mm^2 which is 3 to 4 orders of magnitude higher than passive inductances. In addition, active inductances couple only capacitively to each other, allowing for an even denser layout in large-scale implementations. On the contrary, passive inductances couple magnetically over a longer range which can be more challenging to deal with compared to capacitive interactions. In the following, the realized active inductance will be treated in relation to sensitive capacitance detection while considering the important issues of dissipation and noise.

Active inductance

The active inductance behavior is realized by transforming a capacitor C_L into an inductance $L = C_L/G_{m,1}G_{m,2}$ via two transistor devices of transimpedance $G_{m,1}$ and $G_{m,2}$ forming a gyrator[39]. The non-ideal finite conductance and parasitic capacitance of the transistors set the resonant frequency f_r and quality factor Q. More advanced active inductance architectures incorporate a negative resistor in parallel to the inductance in order to improve Q up to a few hundred with independent tuning of the inductance value L and the quality factor Q[39, 40].

Fine calibration of the tunable inductance value using a capacitor bank leads to a precise definition of the resonant frequency value, ideal for optimal frequency-multiplexing of large qubit matrices. The tunability of the Q-factor enables different modes of read-out. High-Q gives a precise measurement of quantum capacitance to calibrate qubit matrices. Lower-Q is more suitable for fast read-out during quantum computation.

Integrated circuit design

The impedancemetry experiment was integrated on a single chip with multiplexed quantum devices using the Fully-Depleted Silicon-On-Insulator (FD-SOI) 28nm CMOS technology. The FD-SOI technology is well suited for high-speed cryogenic applications[41] with lower variability than bulk technologies[42], less sensitivity to carrier freeze-out, and threshold-voltage tuning via the back-gate[43]. The integration of classical circuitry with small-enough transistors that exhibit quantum properties is a plus to validate efficiently new circuit architectures[22, 25, 44]

The realized integrated circuit contains the current source, the active inductance with addressable capacitor banks for tunability, the multiplexed DUTs, and the amplification stage (Fig. 2a, b). During design, we focused on bringing down the footprint and power consumption of the active inductance being the main original component of our circuit. The current generation and voltage-signal amplification were added on-chip to facilitate testing the concept of impedancemetry at 4.2 K. In the absence of high-frequency models of FD-SOI transistors at cryogenic temperatures, we designed the integrated circuit with accurate room-temperature models supplied by the foundry[45]. The evolution of transistor characteristics towards the lowest temperatures was extrapolated from the temperature variation in foundry models but also from acquired 4.2 K data of single transistors[42, 43]. The chosen implementation for the general design of the complete impedancemetry chip can be found in the Supplementary Material II.

The active inductance follows a known NMOS-based Karsilayan-Schaumann architecture[46, 47]. The gyrator is made of a single-ended negative transconductance $-G_{m,1}$ and a differential transconductance stage $G_{m,2}$ coupled to a tunable capacitance C_L leading to a tunable inductance $L(C_L) = C_L/G_{m,1}G_{m,2}$. An added metal-oxide-metal (MOM) capacitor C_p of 136 fF parallel to L controls the resonant frequency $f_r = 1/2\pi\sqrt{L(C_L)C_p}$. No dependence in temperature is expected for MOM capacitors[48]. Adding C_p makes the measuring circuit less sensitive to a change in DUT-capacitance with the increased tank capacitance but avoids the influence of unknown parasitic circuit capacitances . Hence, the resonant frequency f_r is set by C_p, C_L, and $G_{m,i=1,2}$. C_L is implemented with one main metal-oxide-metal (MOM) capacitor of 362 fF in parallel with two digitally-controlled binary-weighted MOM capacitors of 68 and 136 fF (see Supplementary Material II).

Adding a capacitance C_R at the foot of the differential transconductance stage allows to introduce a negative resistance in series with the active inductance, leading to higher Q-factor with an increased effective parallel resistance $R(C_R, C_L)$. The Q-factor of the active inductance defined as $Q = R(C_L, C_R)\sqrt{L(C_L)/C_p}$ depends on C_L and C_R. By tuning C_L, then C_R, L and Q can be adjusted to any desired value apart from possible instabilities. To tune the Q factor, we choose to cover a wide range of C_R values in steps of 23 fF by selecting 4 binary-weighted MOM capacitors of 23, 46, 92, and 184 fF.

The voltage-controlled current source exciting the resonator is made of a current mirror combined to an RC bias tee. The bias tee superimposes DC signals from the diode transistor to set the DC operating point of the current source and AC signals from the excitation input V_{in} to generate the AC current I_{in}. The RC filter of the bias tee consists of R_{bt} (unsilicided polysilicon resistor of 10 MΩ) and C_{bt} (MOM capacitor

of 406 fF) to reach a characteristic frequency of 39 kHz. As no large signals V_{in} are required, the current source operates in subthreshold regime with a bias current of only 0.1 µA to minimize its conductance for a negligible impact on the resonator and obtain a desirable low transconductance for nA-current excitation.

To investigate the active inductance circuit with different DUTs, we added an addressable bank of 6 capacitors (Supplementary Material II). Three MOM capacitors of 2, 4, and 8 fF have the purpose of calibrating the active inductance on known values. Three additional MOSFETs (M0, M1, M2) of width 80 nm and length 28, 60, and 120 nm are used as test-bench for the investigation of quantum properties. The source and drain voltage of the quantum MOSFETs are grounded when unselected and polarized at V_{bias} when selected. The differential transconductance stage of the active inductance copies the DC common-mode voltage V_{cm} to the DUT gate potential, such that the DC gate voltage $V_{gs} = V_{cm} - V_{bias}$ can be varied via V_{bias} (see Fig. 2).

Once excited by I_{in}, the tank voltage is amplified, then sent through a unit-gain buffer for detection at room temperature via meter-long cable. The amplifier is a common-source N-type single-stage and the 1:1 buffer is a common-drain N-type single stage (see Fig. 2a).

The specifications of the circuit at room temperature with respect to inductance values, resonance frequencies, Q-factors, power consumption, and amplifier characteristics have been extracted from simulations using foundry models (see Supplementary Material III for more details). The emulated inductance L ranges from 5.3 to 8.4 µH to reach a resonance frequency f_r from 128 to 165 MHz. The settings of tuning C_L and C_R allow to cover a wide range of quality factors Q from 7 to 300, along with the occurrence of negative Q values that lead to instabilities. The estimated power consumption of the resonator is 85 µW, which could be shared among a number of qubits in a frequency-multiplexed array depending on the allowed frequency spacing within the bandwidth.

From the foundry models at room temperature, we get for the current generating transistor a transconductance G_m of 3.4 nA/mV with a bandwidth of 3.5 GHz (see Supplementary Material III). The first amplifier stage has a gain A of 15 dB and a bandwidth of 1.8 GHz for a power consumption of 150 µW. The next buffer stage in the amplification reaches a bandwidth of 92 MHz for a cable capacitance of 50 pF and a power consumption of 2.4 mW. The net amplification at 165 MHz becomes 8 dB.

Transistor noise translates into transconductance noise for the transistors forming the gyrator-like inductance circuit which generates perturbing variations of the active inductance. A varying L modulates f_r and generates phase noise in V_{out}. The phase noise spectrum of V_{out} around the carrier frequency f_r extracted from room-temperature steady-state simulations (SST) exhibits a $1/f$-flicker component (see Supplementary Material III) on time-scales larger than 10 ms, resulting from a noisy L. For a typical Q of 81 with sufficiently fast measurements at frequencies above 100 Hz to avoid $1/f$ noise, this translates into a phase noise of $0.002\,^\circ/\sqrt{\text{Hz}}$ leading to an input-referred noise of $3.2\,\text{aF}/\sqrt{\text{Hz}}$. This estimated noise in measured capacitance can be compared with the lower and upper range (roughly from 10 aF to 1 fF) of the quantum capacitance in a semiconductor qubit, which would require a noise level of 0.003 to 0.3 $\text{aF}/\sqrt{\text{Hz}}$ for 99 % read-out fidelity (or SNR = 22) in 1 µs (see Eqs. 17-19 in [49]). While the noise of the designed impedancemetry circuit may be too large for fast single-shot

qubit-state detection with high fidelity, the noise performance could be improved in the future through optimization of the active inductor architecture and by taking advantage of forthcoming compact transistor models at cryogenic temperatures.

Voltage excitation and homodyne detection are performed at room temperature with an all-digital lock-in amplifier (Fig. 2c). Different configurations for single (I) and double (II a,b) demodulation are further described in the following section when needed.

Impedancemetry circuit characterization

Without the assistance of low-temperature models, the operating point of the circuit had to be determined experimentally starting from room-temperature settings of bias voltages and currents. The increase in threshold voltage of NMOS (resp. PMOS) transistors at 4.2 K is compensated by applying a back-gate voltage of 1.2 V (resp. -2 V). The optimal cryogenic common-mode voltage $V_{cm} = 0.48$ V was obtained while monitoring the tank impedance via repeated frequency sweeps until a typical resonance behavior up to 200 MHz emerges for the lowest values of C_L and C_R. The gain of the low-temperature amplification stage at f_r is optimized with respect to the current bias of amplifier and buffer (see Supplementary Material IV for a detailed low-temperature characterization of the amplifiers). The main results of the impedancemetry with respect to tunability and detection sensitivity are shown in Figure 3.

The amplitude and phase of V_{out} using single homodyne detection (I) without any connected DUT are shown in Fig. 3a for the 4 C_L values from 362 to 566 fF and two C_R values chosen between 0 and 322 fF depending on C_L. V_{out} at maximal amplitude was kept equal to 1.8 mV by adjusting V_{in} to avoid non-linearities coming from non-linear MOSFETs behavior. The resonance frequency f_r varies by 5 % from 189 to 199 MHz by tuning C_L. The quality factors Q extracted from a linear fit of the phase around f_r are shown in Fig. 3b. The Q values range from 80 to 250, and can be tuned by a factor > 2 for every C_L by adjusting C_R. These data demonstrate that Q can be tuned almost independently of the resonance frequency with a frequency variation of less than 0.22 % across the entire C_R range (see Fig. 3b).

For the minimum value of C_L with the highest resonance frequency, we calibrate the capacitance sensitivity of the circuit for each Q by switching on and off the DUT MOM capacitors C_m=2, 3, and 8 fF and using double homodyne detection (II a) (see Fig. 3c). The capacitance sensitivity α is extracted from a least-square linear fit of the phase change $\Delta\phi = QC_m/C_p \equiv \alpha C_m$ for a given Q as shown in Fig. 3d. The sensitivity α increases linearly with Q from 0.76 to 1.9 °/fF. From the linear fit in Figure 3d, we obtain $C_p = 137$ fF, in good agreement with the designed value (136 fF). In usual circuits without an additional input capacitance[46], the parasitic capacitance of the MOSFETs determines the resonance frequency. In future design with accurate cryogenic compact models, this capacitance can be reduced significantly leading to higher resonance frequency and improved sensitivity, along with larger Q.

From C_p and f_r, we are now able to deduce the inductance value L. By adjusting C_L, L varies from 2.42 to 5.18 µH. For a total footprint of 60×50 µm, the active inductance density of 1.73 mH/mm^2 is five orders of magnitude higher than previously used passive inductors (55 nH/mm^2)[37] and three orders of magnitude higher than superconducting inductors (1.6 µH/mm^2)[50].

From the bias-current settings at cryogenic temperatures, a reliable estimate of the power consumption of the impedancemetry circuit can be given, at low temperatures amounting to 123 µW for the active inductance, 0.15 µW for the input-current source, and 2.9 mW for the output amplification. These values can be reasonably compared with the circuit simulation at room temperature mentioned previously.

Capacitance resolution

We will now examine the capacitance resolution of the set-up, in deriving the input-referred noise in $\mathrm{aF}/\sqrt{\mathrm{Hz}}$ from the signal-to-noise ratio (SNR) as a function of the integration time t_{int}.

To accomplish this, we generate a capacitance change by continuously connecting and disconnecting the DUT MOM capacitor $C_m = 2\,\mathrm{fF}$ at a rate of 1 kHz. Using the demodulation method (I), the square-wave of the phase ϕ at f_r with a rise time given by the integration time is used to extract the signal power P_{sig} and noise power P_{noise} by separating the corresponding frequency components in the power spectrum (see Supplementary Material IV for the used method of analysis). The resulting SNR$= P_{sig}/P_{noise}$ is used to extract the capacitance resolution given by the equivalent $C_m(SNR = 1) = C_m/SNR$ shown in Fig. 4 as a function of t_{int} from 100 ns to 100 µs. A capacitance of 1 fF can be detected with an integration time of 1 µs with $SNR = 1$. The capacitance resolution follows a square-root law with t_{int} from which we extract the equivalent input-referred noise of $3.7\,\mathrm{aF}/\sqrt{\mathrm{Hz}}$, close to the previously mentioned noise extracted from room-temperature simulations. The obtained noise amplitude is two orders of magnitude higher than the best reported sensitivity using an ultra-low noise SQUID amplifier ($0.07\,\mathrm{aF}/\sqrt{\mathrm{Hz}}$)[51]. However, removing the SQUID amplifier and only measuring with the remaining standard 4 K semiconductor amplifier increases the noise to $1.6\,\mathrm{aF}/\sqrt{\mathrm{Hz}}$[51], which lies in the same order of magnitude as the obtained noise for our approach.

A correlated noise of the type of a two-level fluctuator appears on longer time scales which originates probably from the $1/f$ flicker noise of the transistors, preventing measurements at times longer than 1 ms using detection method (I). To remove the phase noise originating from the fluctuating L, we add a second demodulation (IIa) at the capacitance switching frequency of 1 kHz. The 1 kHz square-wave ϕ from (I) with an integration time of 100 µs is demodulated by method (IIa) at 1 kHz to obtain its amplitude $|\phi|$. The capacitance resolution as a function of the second integration time for the 1 kHz demodulation is extracted by taking the ratio of the average and the standard deviation of the $|\phi|$ signal and is shown in Fig. 4. With an integration time of 1 s, the experimentally observed resolution becomes as low as 10 aF.

Quantum capacitance measurements

With the calibrated impedancemetry circuit, we are able to detect the gate quantum capacitance C_{gg} of the multiplexed tiny MOSFETs (M0, M1, M2 in Figure 2a) similar to the ones used to implement spin qubits with CMOS technology[7]. Measurements will be presented for M2 with a gate length of 120 nm and a gate width of 80 nm. The

device M1 with length 60 nm and width 80 nm shows similar behavior (see Supplementary Material V). The device M0 with length 28 nm and width 80 nm did not reveal any distinct oscillatory structure above the noise level as observed in the other two devices.

The total gate capacitance C_{gg} of such devices corresponds to the sum of the capacitance to drain, source, back-gate, and MOSFET channel of which the gate to channel capacitance depends highly on the gate-source voltage V_{gs} controlled by the DC component of V_{bias} via $V_{gs} = V_{cm} - V_{bias}$ (see Fig. 2a). As C_{gg} of a nanometric device (few aF) is extremely small compared to $C_p = 136\,\mathrm{fF}$, we do not expect to have sufficient SNR for small capacitance variations at reasonable integration times. Better sensitivity can be obtained by modulating V_{gs} (method IIb) to measure after demodulation the first derivative dC_{gg}/dV_{gs} as C_{gg} varies a lot in a small V_{gs} window.

While the resonator impedance is probed at 199 MHz, V_{gs} is modulated at 1 kHz with mV-range excitation on V_{bias} (see Fig. 2b and 2c). The obtained result with a relatively large 25 mV V_{gs} modulation (shown in Fig. 5a) is reminiscent of the typical gate capacitance variation around threshold voltage $V_{th} \simeq 0\,\mathrm{V}$ shown for $V_{bg} = 6\,\mathrm{V}$. C_{gg} (see inset of Fig. 5a) reflects the typical behavior for a FET capacitance from the subthreshold regime $V_{gs} \ll V_{th}$ to the strong inversion regime $V_{gs} \gg V_{th}$. The measured overall change in gate capacitance, approximately 6 aF as shown in the inset of Figure 5a, could be compared with the expected geometric capacitance of 77 aF for M1, using a crude parallel-plate approximation with transistor gate area and 1.1 nm equivalent silicon-oxide thickness for GO1 transistor devices. The circuit in series with the gate capacitance, used to apply the gate voltage (see Figures S5b and c in Supplementary Material II), might play a role to explain the discrepancy between the measured DUT capacitance and the expected value for small values of capacitance.

Upon decreasing the amplitude of the V_{gs} modulation to only 3.1 mV, the observed dC_{gg}/dV_{gs} signal in Fig. 5b reveals a fine structure around V_{th} consisting of successive peak-dip oscillations. Following numerical integration, these features result in a series of peaks in C_{gg}, which we interpret as quantum contributions to the capacitance coming from electrons tunneling in and out of randomly localized quantum states within the transistor channel. Such quantum phenomena have been observed previously in various CMOS devices (see review [52]), including nanometer-sized transistor channels made of the same FD-SOI 28nm technology[43].

To further identify these quantum states, we acquire dC_{gg}/dV_{gs} for different back-gate voltage V_{bg} from 2 to 6 V as shown in Fig. 5c. As V_{bg} increases, all observed features shift to lower V_{gs} with a slope close to the ratio $\beta = C_{g-ch}/C_{bg-ch}$ of gate-channel capacitance C_{g-ch} over the backgate-channel capacitance C_{bg-ch} alike the V_{th}-shift with back-gate for similar FET devices[43]. For $V_{bg} > 4\,\mathrm{V}$, all features have a coupling ratio of 10 except for one with a lower coupling 8.6 attributed to an impurity closer to the back-gate interface. No anomalous impurity structure is detected in the smaller 60×80 nm device (see Supplementary Material V). At lower V_{bg}, the coupling increases with V_{gs} from 10 to 14 as the electron-filled inversion layer is brought back to the top-interface. The systematic gate-voltage variation of the oscillatory structures with applied back-gate voltage gives additional evidence that these structures result from the DUT transistor.

While there is still room for improvement in the noise of the active inductor and

the power consumption of the amplifier stages, these measurements demonstrate that the proposed integrated impedancemetry approach can detect the capacitive signatures of structure in the electronic density of states of quantum dots.

Conclusions

We reported an integrated circuit that performs impedancemetry of a resonator coupled to a quantum dot for the measurement of quantum capacitance at cryogenic temperatures. The realized on-chip circuit of the impedancemeter operating at 4.2 K allows the measurement of quantum capacitance with a resolution down to 10 aF (noise level 3.7 $\mathrm{aF}/\sqrt{\mathrm{Hz}}$). Although improvements should be made in the noise performance to be competitive with state-of-the-art reflectometry on quantum devices, the implementation of the active inductance in the resonator allowed the controlled tuning of the resonance frequency and quality factor, which will be of importance for optimal frequency-spectrum crowding in multiplexed read-out schemes. Novel read-out architectures with cryogenic electronics, such as the active inductance with its much smaller footprint compared to passive circuit elements, have the potential to increase scalability and flexibility in the design and exploitation of quantum processors.

The time multiplexing of nanometric quantum devices with on-chip switches can be beneficial in reducing the power consumption per qubit in a scalable multi-qubit architecture. Combined with frequency multiplexing, the dissipated power of about 100 µW for the resonator circuit could be used for the read-out of 100 or more qubits by optimizing the frequency bandwidth and resolution. To improve the impedancemetry method, the amplification stages should be positioned at base temperature, close to the resonator and the connected device. Although the focus of the present design is to prove the principle of integrated active impedancemetry, improvements are needed to measure devices at sub-K temperatures with the limited cooling power of typically 500 µW.

Further work towards lower noise and lower power design with more accurate high-frequency models of transistor characteristics at cryogenic temperatures will improve the final performance. Measuring multiplexed out-of-chip capacitances of quantum devices will be also promising for the systematic screening and testing of many quantum devices with a simpler experimental setup than reflectometry. In the long run, the realization of tailored high-end analog electronics at cryogenic temperatures will improve and accelerate the up-scaling of quantum processors.

Methods

Fabrication details. The impedancemetry chip was designed in a commercial CMOS FD-SOI 28nm technology with low-V_{th} (LVT) thin-oxides (GO1) for both the circuit transistors and the DUT nanotransistors. The chip is wire-bonded onto a QFN48 package directly soldered on a 4-layer PCB with FR4 substrate.

Measurement set-up. The FR4 PCB is placed at the end of a dip-stick enclosed in a metallic container filled with a small amount of helium gas for thermal exchange with a liquid He bath at 4.2 K (see Supplementary Material VI). A PCB-mounted thermometer ensures a precise monitoring of the PCB temperature. High-frequency lines

of V_{in} and V_{out} are routed on the PCB from the chip package to the SMA coaxial connectors via top-layer 50Ω-matched co-planar waveguide with ground plane and via fencing. Supply lines are decoupled from environmental noise with PCB-mounted capacitors (0.1, 1, 10 µF) and conveyed to room temperature with copper wiring. All other DC lines are conveyed to room-temperature with $50-130\,\Omega$ constantan wiring. At room temperature, electronic apparatus comprises a multi-channel low-noise 21-bit digital-to-analog converter, and a 600 MHz lock-in amplifier.

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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Competing interests

The authors declare a granted patent US-Patent 11387828, dated July 12, 2022.

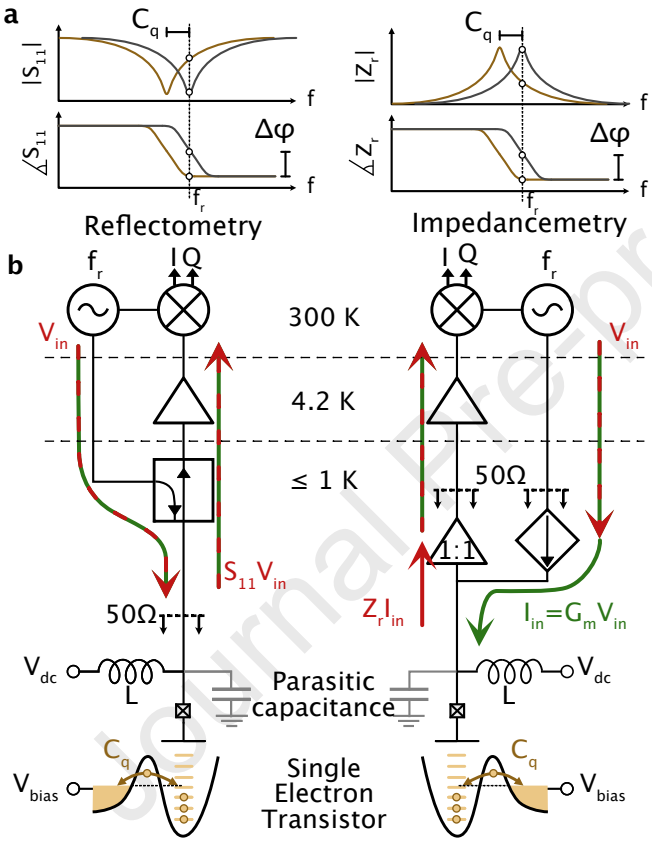

Figure 1: Integration of measuring circuitry for read-out of quantum capacitance. **a,** Schematic signals of amplitude and phase for the complex scattering coefficient S_{11} and impedance Z_r of a resonant circuit in, respectively, reflectometry and impedancemetry. **b,** Comparison between a typical reflectometry setup (left) and the proposed impedancemetry setup (right) for the measurement of the quantum capacitance C_q of a single-electron transistor embedded in a resonant *LC* circuit. Impedancemetry with the integrated cryogenic electronics for applied current I_{in} and amplified signal $I_{in}Z_r$ leads to a lower footprint of the measurement circuitry by getting rid of bulky directional couplers. Red (respectively green) arrows represent voltages (resp. currents). Red-green arrows emphasize the voltage-current interdependence due to signal propagation in 50 Ω lines.

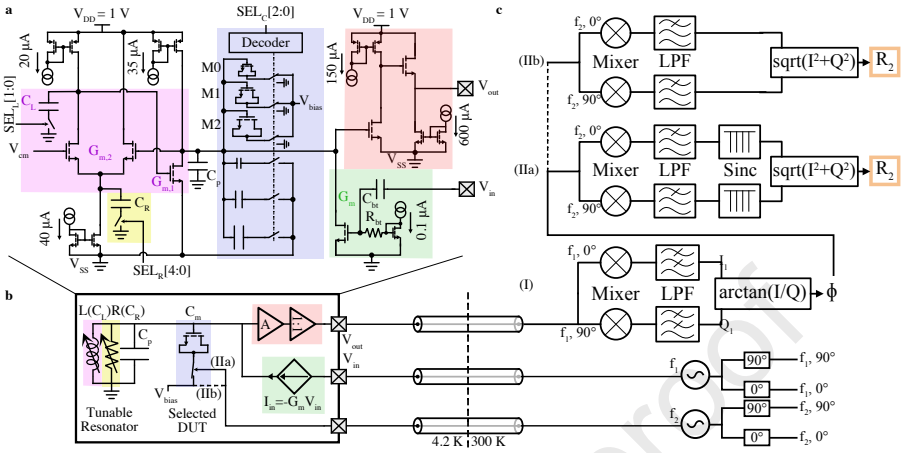

Figure 2: Setup with on-chip electronics. **a,** On-chip circuit implementation of the active inductance (pink), current excitation (green), test capacitor bank (blue), and amplification stage (red). For clarity, the bias MOSFETs operating in DC are drawn of smaller size than MOSFETs in the high-frequency signal chain. **b,** Simplified view of the on-chip resonant circuit placed at 4.2 K with tunable resonator, DUT, current excitation, and voltage amplification, linked to room-temperature phase-sensitive electronics via meter-long cables. **c,** Room-temperature homodyne detection with single (I) and double (II) demodulation of the circuit output V_{out} and generation of voltage excitation V_{in} at modulation frequencies f_1 (150-200 MHz) and f_2 (1 kHz).

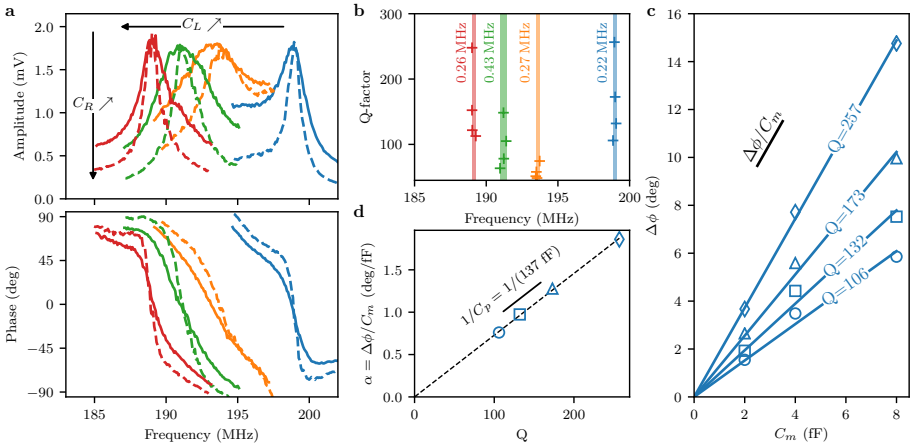

Figure 3: Characterization of the resonant circuit at 4.2 K for capacitance detection. **a,** Amplitude and phase of the demodulated circuit output V_{out} for several active inductance settings. The resonance frequency shifts to lower frequency as the inductance value increases with increasing C_L (different colors). The continuous line (low-Q) and dashed line (high-Q) show the signals for different values of C_R. **b,** Data points for the resonance frequency f_r when the extracted Q is tuned with C_R. The colored bars of width given by the written maximal deviation indicate the low dispersion of f_r for fixed C_L when varying Q with C_R. **c,** Measured phase shift for MOM capacitor C_m of 2, 4, and 8 fF in several Q-factor settings. The capacitance sensitivity $\Delta\phi/C_m$ of the circuit is extracted from the slope with a least square fit at given Q. **d,** Capacitance sensitivity extracted from **c** as a function of the Q factor. A least square linear fit of $\Delta\phi/C_m(Q)$ allows to extract the capacitance C_p parallel with the active inductance.

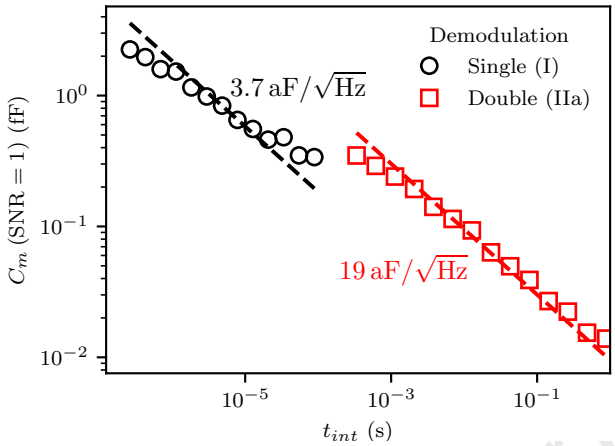

Figure 4: Capacitance resolution of the measurement set-up at 4.2 K. Extrapolated capacitance C_m at signal-to-noise ratio equal to 1 for single (I) (black circles) and double (IIa) (red squares) homodyne detection of the capacitance measurement as a function of the integration time t_{int}. Dashed lines are least-square fits $C_m = a\, t_{int}^{-1/2}$ with $a = \sqrt{0.25}\, S_c$ and S_c (indicated values) the equivalent noise spectral density in aF/$\sqrt{\text{Hz}}$ of the capacitance measurement.

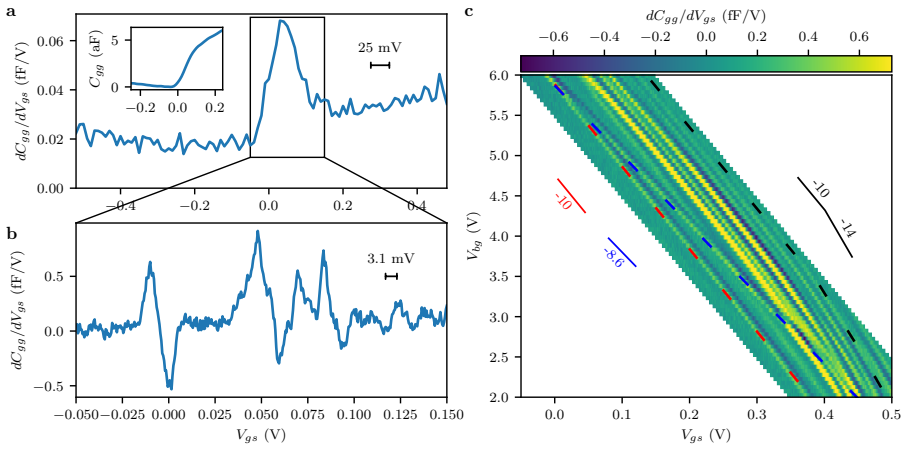

Figure 5: Quantum capacitance measurement of an integrated MOSFET with channel length 120 nm and width 80 nm at 4.2 K. **a,** Measurement of the first derivative of the gate capacitance C_{gg} with respect to V_{gs} by applying a gate-source AC excitation of 25 mV. The inset shows the capacitance $C_{gg}(V_{gs})$ variation of approximately 6 aF near threshold gate-voltage computed from the integrated signal of the derivative, to be compared with the geometric gate capacitance for this MOSFET (see text). **b,** Expanded view of dC_{gg}/dV_{gs} around the off-on transition of the MOSFET measured with a smaller excitation of 3.1 mV. The resolved features are signatures of quantized electronic states in the measured capacitance of the MOSFET channel. **c,** Evolution of dC_{gg}/dV_{gs} with the back-gate voltage V_{bg} and the gate-source voltage V_{gs}. The indicated slopes $\beta = dV_{bg}/dV_{gs} \simeq C_{g-ch}/C_{bg-ch}$ represent the relative coupling strength of the detected quantized states with respect to back- and front-gate.

Declaration of interests

☐ The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

☒The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

The authors declare a granted patent US-Patent 11387828, dated July 12, 2022.