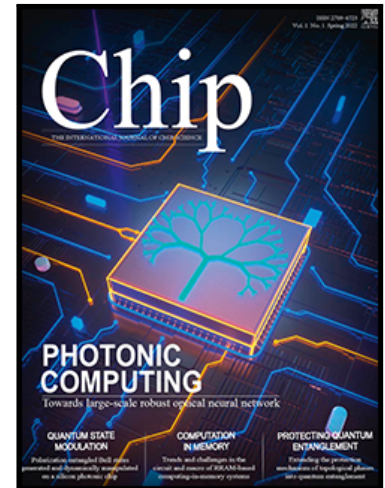


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Cryo-CMOS modeling and a 600 MHz cryogenic clock generator for quantum computing applications

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ABSTRACT

The development of large-scale quantum computing has boosted an urgent desire for the advancement of cryogenic CMOS (cryo-CMOS), which is a promising scalable solution for the control and read-out interface of quantum bits. In this paper, 180 nm CMOS transistors are characterized and modeled down to 4 K, and the impact of low-temperature transistor performance variations on circuit design is also analyzed. Based on the proposed cryogenic model, we present a 180 nm CMOS-based 450-850 MHz clock generator operating at 4 K for quantum computing applications. At 600 MHz output frequency, it achieves <4.8 ps RMS jitter with 30 mW power consumption (with test buffer), corresponding to a -211.6 dB jitter-power FOM, which is suitable for providing a stable clock signal for the control and readout electronics of scalable quantum computers.

Keywords: Cryogenic CMOS, Characterization, Modeling, Clock generator, Quantum computing

INTRODUCTION

Over the past decade, quantum computers have garnered significant attention due to their unparalleled computing capabilities in solving specific problems that are intractable for classical computers, such as prime factorization, quantum medical analysis, etc¹⁻³. Quantum bits (qubits) are operated in an ultra-low temperature environment provided by a dilution refrigerator, typically in the range of a few tens of millikelvin, and manipulated using microwave-driven controlled evolutions and flipping operations. To accurately read out and control the quantum processor, a classical control interface is typically employed, which is implemented today with commercial instruments operating at room temperature (300 K) and connected to the qubits via coaxial cables. However, as the number of qubits grows towards thousands and millions, the corresponding increasing number of long cables introduces challenges, including heat leakage and time delays, which significantly impact the temperature stability inside the dilution refrigerator and complicate the measurement process. Practical quantum computing applications require stable manipulation and readout of millions of qubits, demanding scalability in quantum computing systems. To overcome this bottleneck, a cryogenic electronic interface that operates in

close proximity to the quantum processor is proposed⁴⁻⁶. This readout and control interface is placed in the 1-4 K temperature zone of the refrigerator, which reduces the temperature leakage, minimizes the path of high-frequency signals, and mitigates the complex interconnection challenges between the cryogenic qubits and room temperature instruments. Therefore, research on low-temperature electronics and IC for quantum computing applications has been an active research field over the past few years³⁻²⁰.

Although a cryogenic analog-to-digital converter (ADC) for RF readout of large-scale spin quantum bits has been presented^{7,15}, its clock signal is currently sourced from an oscillator at room temperature, which increases the complexity and limits the scalability of system interconnection. Therefore, as shown in Fig. 1, a local cryogenic clock generator is required to generate clock signals for the components (such as ADC, DAC, etc.) in the qubit control/readout circuits. Firstly, the electrical characteristics of cryogenic CMOS (cryo-CMOS) devices deviate significantly from those at room temperature.

Commercial models of CMOS devices are typically designed for an applicable temperature range of -40 °C to 125 °C²¹⁻²³.

Therefore, it is necessary to conduct characterization and modeling of cryo-CMOS devices to address the availability of the compact model. Cryogenic circuit architectures also need adjustment to accommodate the characteristics of cryo-CMOS devices for reliable operation at such low temperatures.

In this article, we characterize SMIC 180 nm CMOS transistors at temperatures ranging from 300 to 4 K. Based on the commercial BSIM3v3 model, we develop a cryo-CMOS model available for 4 K simulations to aid in the design of cryogenic circuits. This model incorporates the correction of low-temperature effect and parameter optimization using a machine learning (ML) approach. On this basis, this work demonstrates a cryo-CMOS clock generator, which is optimized for 4 K operation. The clock generator exhibits an output frequency range of 450-850 MHz. At 600 MHz output frequency, it achieves -95.53 dBc/Hz with 10 kHz offset and -102.73 dBc/Hz with 1 MHz offset phase noise, <4.8 ps RMS jitter, and -39.32 dBc reference spur with 30 mW power consumption (with test buffer), corresponding to a jitter-power FOM of -211.6 dB at 4 K.

This article is organized as follows. In Section II, we provide a description of cryogenic device characterization and the developed 4 K CMOS model for circuit design. Section III elaborates on the clock generator architecture and cryogenic circuit design considerations. The measurement results of the clock generator at 300 K and 4 K are presented in Section IV, and finally, we conclude this article in Section V.

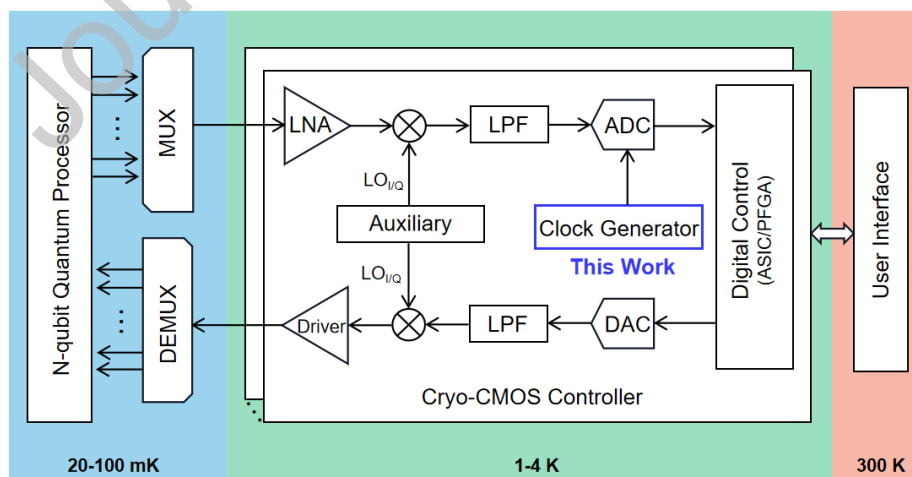


Fig. 1 | Simplified block diagram of the cryo-CMOS controller for the control and readout of qubits⁴⁻⁵.

CRYOGNEIC DEVICE CHARACTERIZATION AND MODELING

Cryo-CMOS Characterization The low-temperature behavior of devices deviates from that at 300 K, leading to a necessary re-characterization and modeling process. As shown in Fig. 2, we characterized the electrical properties of the 180 nm CMOS technology in a wide temperature range from 300 K to 4 K. Due to the relaxation of the Boltzmann thermodynamic limit ($k_B T/q$), the subthreshold swing (SS) becomes steeper as the temperature decreases [Fig. 2a and 2c], which means that the switching speed of the devices becomes faster at low temperatures. Due to the weakening of lattice scattering, the mobility is optimized and then the drain current (I_{DS}) and the transconductance (G_m) are improved, as shown in Fig. 2a and 2b. The low-temperature mobility is mainly determined by surface roughness scattering, thus the mobility reduction due to the vertical field at large V_{GS} bias is more significant at low temperatures, even leading to negative G_m behavior at $V_{GS} = 1.8$ V in Fig. 2b. Fig. 2d shows the output characteristics in 10 $\mu\text{m}/180$ nm NMOS at different temperatures. As expected, the on-state current (I_{ON}) increases gradually as the temperature decreases, especially between 77 K and 300 K. It is worth noting that, at 4 K when $V_{DS} > 1.4$ V, I_{DS} exhibits a significant unsaturated characteristic, resulting in a significant reduction in transistor output impedance. This phenomenon is caused by the “kink effect”²⁴⁻²⁵ and will be discussed in the next subsection. Therefore, it is necessary to avoid transistor bias within this range ($V_{DS} > 1.4$ V) in circuits that are sensitive to output impedance, such as amplifiers or current sources. The saturation region transfer characteristics and the extracted threshold voltage (V_{TH}) are shown in Fig. 2e and 2f. The gate-induced drain leakage (GIDL) effect and the off-state (I_{OFF}) current are significantly optimized at low temperatures [Fig. 2e]. At low temperatures, the larger band gap elongates the band-to-band tunneling (BTBT) distance and thus reduces the GIDL current²³. It means that the on-off ratio is improved and the static power consumption in the digital circuit is greatly reduced. V_{TH} is extracted at the threshold current $I_{TH} = 1.0 \times 10^{-9}$ W/L (A). Compared with room temperature, V_{TH} increases by ~ 300 mV at 4 K in both 10 $\mu\text{m}/10$ μm and 10 $\mu\text{m}/180$ nm transistors, which can be attributed to the bandgap (E_g) widening and the scaling of the Fermi-Dirac function²⁶⁻²⁸. The intrinsic carrier concentration n_i is extremely small at low temperatures and thus leads to a large inversion threshold $2\phi_F = 2k_B T/q \ln(N_a/n_i)$, where N_a is the substrate doping concentration. Therefore, a higher supply voltage is required to overcome the increased V_{TH} at low temperatures but results in additional power consumption. To overcome the trade-off of power consumption and frequency, low- V_{TH} devices, adjusting V_{TH} by substrate bias, and back-gated silicon-on-insulator technologies are favorable choices for cryo-CMOS circuits design.

To guide the cryo-CMOS circuits design, the low-field mobility of NMOS and PMOS (μ_n and μ_p) is estimated at $V_{DS} = 50$ mV by the Y-function (the $I_D/\sqrt{G_m}$ method)²⁹⁻³⁰. The extracted results are shown in Table 1. At room temperature, the ratio of μ_n to μ_p is about 3.7:1, but it becomes 5.9:1 at 4 K. In digital circuits, to ensure that the rising time of the output signal is consistent with the falling time, the size of PMOS must be much larger than that of NMOS to obtain sufficient pull-up capability. Therefore, the digital standard cell libraries need to be redesigned. Different from μ_n , μ_p at 77 K is slightly larger than that at 4 K. To adjust the V_{TH} of PMOS, a light boron implant was performed in the channel, leading to the formation of buried channels. Due to the freeze-out of the implant, the peak mobility of the buried channel is around 80 K³¹⁻³², thus μ_p at 77 K is slightly larger than 4 K. In addition, the G_m - V_{GS} curve changes more dramatically at low temperatures [Fig. 2b]. This phenomenon may deteriorate the linearity of circuits, such as amplifiers, and thus aggravate the total harmonic distortion (THD). In addition, the mismatch of the current factor (β) and V_{TH} deteriorates as well at cryogenic temperatures³³, leading to an additional challenge. Based on the above analysis, it is necessary to establish a cryo-CMOS model to assist low-temperature circuit design.

Table 1 | Mobility of 10 $\mu\text{m}/180\text{ nm}$ MOSFETs at 300 K, 77 K, and 4 K.

Temperature (K)	300 K	77 K	4 K
$\mu_n (\text{cm}^2/\text{V}\cdot\text{s})$	145.9	993.3	1066.5
$\mu_p (\text{cm}^2/\text{V}\cdot\text{s})$	113.3	182.8	181.5
μ_n/μ_p	3.7	5.4	5.9

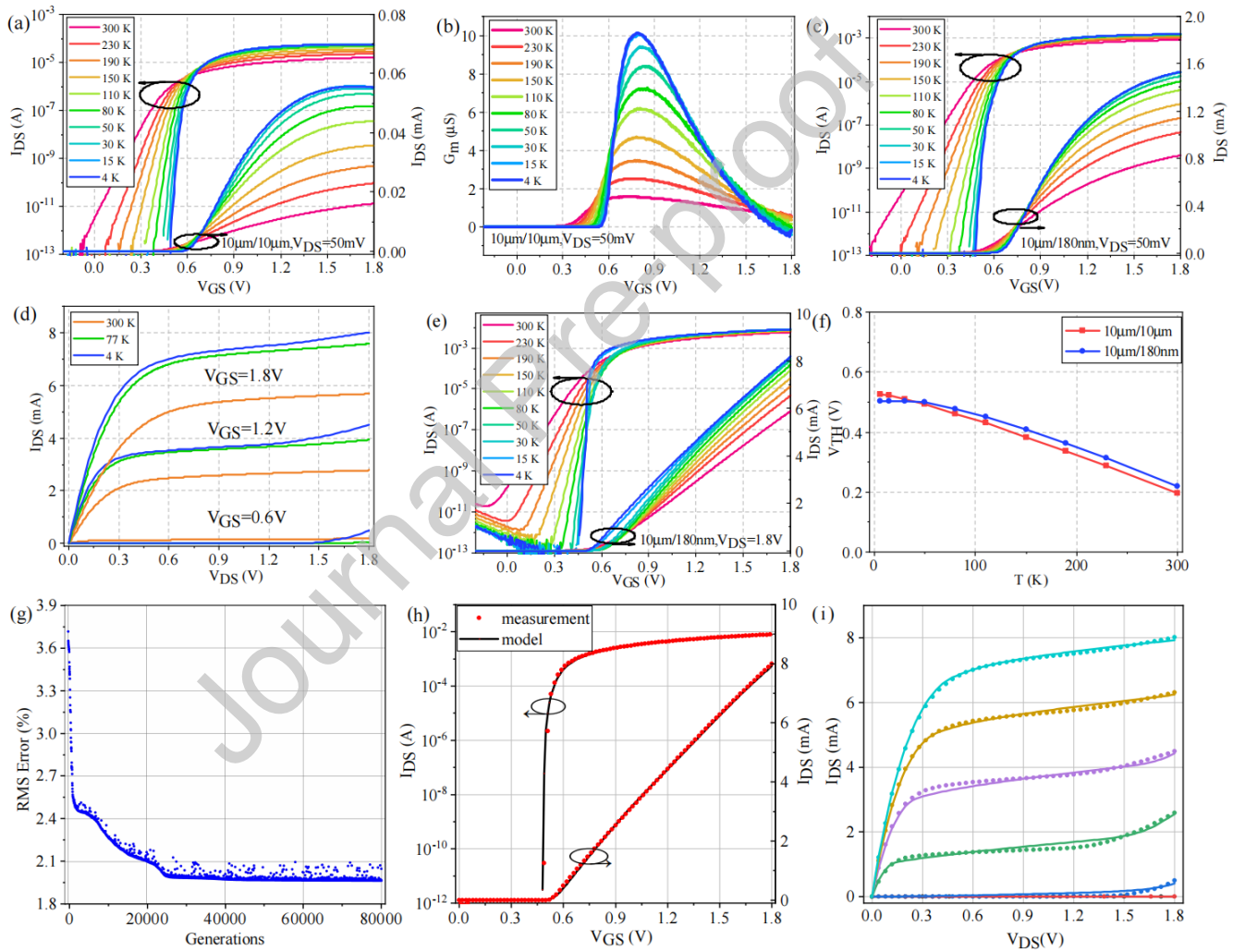


Fig. 2 | Cryo-CMOS characterization and modeling. **a**, I_{DS} - V_{GS} curves and **b**, The transconductance of 10 $\mu\text{m}/10\text{ }\mu\text{m}$ NMOS with $V_{DS} = 50\text{ mV}$. **c**, Linear region transfer characteristics, **d**, output characteristics, and **e**, saturation region transfer characteristics of 10 $\mu\text{m}/180\text{ nm}$ NMOS. **f**, V_{TH} versus temperature in 10 $\mu\text{m}/10\text{ }\mu\text{m}$ and 10 $\mu\text{m}/180\text{ nm}$ NMOS. **g**, RMS error versus optimization generations an example Cryo-CMOS parameter optimization process. After kink correction and ML-assisted parameter optimization, the measurement (symbol) and model calculation results (solid line) of the **h**, saturation region transfer characteristic and **i**, the output characteristic at 4 K.

ML-Assisted Parameter Optimization and Modeling As reported²⁵, the standard compact model is able to cover cryogenic operation without significant modifications (e.g. BSIM²¹, EKV²², PSP³⁴). The low-temperature CMOS characteristics are described by updating the parameters of the standard commercial model. The E_g widening-induced V_{TH} shift can be described by adjusting the V_{TH} -related parameters, the weakening of lattice scattering can be described by adjusting the mobility-related parameters, and mobility reduction due to the vertical field is already included in the original BSIM model. Besides, although most commercial models are based on the Boltzmann statistics, the Poisson-Boltzmann equation is still effective even down to deep-cryogenic temperatures²⁷. To obtain more accurate cryogenic model parameters, we developed a machine learning-assisted parameter optimization program. A modified evolutionary strategy (MES) is proposed to optimize the default parameters of the BSIM3v3 model²¹ and the (1+1) evolutionary strategy³⁵ is employed in the MES. The mutation is the foremost step in MES and the equations of the mutation operation are presented below:

$$\begin{cases} i = \text{radnom.randit}(0, n) \\ j = \text{radnom.randit}(-100, 100) \\ \text{Gene}_i(\text{child}) = \text{Gene}_i(\text{parent}) \times (1 + j/1000) \end{cases}$$

where $\text{Gene}_i(\text{child})$ is the value of $(i+1)^{\text{th}}$ parameter of the child generation and $\text{Gene}_i(\text{parent})$ is the value of $(i+1)^{\text{th}}$ parameter of the parent generation. The child parameters' vector is written into the model equations after the mutation operation to calculate the simulation value. The *RMS error* and the *fitness* are defined as:

$$\begin{cases} \text{RMS Error} = \sqrt{1/N \times \sum_{i=1}^n \left(\frac{I_{\text{measi}} - I_{\text{calci}}}{I_{\text{measimax}}} \right)^2} \times 100 \\ \text{fitness} = \frac{1}{m} \times \sum_m \text{RMS Error} \end{cases}$$

where N is the number of data points, I_{measi} , I_{calci} , and I_{measimax} represent the measurement data, calculation results, and the maximum measurement value, respectively. The *fitness* is the average *RMS error* of different electrical characteristics in CMOS transistors. According to the *fitness* value, the program selects the better parameters' vector from the child and parent as the parent of the next generation until the optimization process is completed. An example optimization process is shown in Fig. 3a: the *RMS error* decreases monotonically until convergence during the parameter optimization process. To ensure the rationality of the parameters, the model parameters are corrected, adjusted, and ML-assisted optimization multiple times during the modeling process.

Besides, the non-ideal effects need to be additionally corrected. The kink effect can be effectively avoided in processes below 160 nm node³⁶, but it is an additional challenge for 180 nm cryo-CMOS modeling [Fig. 2d]. The physical explanation of the kink effect dates back three decades^{24,37-39}. At low temperatures, the substrate is so resistive that it is at floating potential due to the carrier freeze-out. The holes produced by impact ionization flow to the freeze-out substrate and accumulate, raising the floating substrate potential. Hence V_{TH} reduces and I_{DS} increases, i.e., resulting in the kink effect³⁸⁻³⁹. Following the above physical mechanism, the revised threshold voltage (V_{TH_kink}) can be expressed as:

$$V_{TH_kink} = V_{FB} + 2\Phi_F + \gamma\sqrt{2\Phi_F - V_{bulk}}$$

where Φ_F is the Fermi potential, γ is the substrate bias effect coefficient. V_{bulk} is the potential of the freeze-out substrate and can be calculated by $V_{bulk} = I_{sub} \times R_{bulk}$, where I_{sub} represents the substrate current and R_{bulk} is the substrate resistance related to I_{sub} ²⁵. The modified V_{TH_kink} is written into the original model and then the corrected I_{DS} is calculated. As shown in Fig. 3b and 3c, the simulation results of the model and the measurement results are well-fitted in the subthreshold, the saturation, and the kink region. However, the accuracy of the proposed model is limited. This parameter-fitted model is not a low-temperature physics-based compact model and many of the low-temperature effects (e.g. incomplete ionization^{26,40-41},

quantum transport⁴², source-to-drain tunneling⁴³⁻⁴⁴, etc.) have not been taken into account. Besides, the Monte-Carlo parameters, parasitic capacitors, self-heating effect⁴⁵, mismatch parameters³³, and small-signal model⁴⁶ of cryo-MOSFETs also need further study and modeling. These works will be carried out in our next stage of cryo-CMOS modeling research.

CRYO-CMOS CLOCK GENERATOR

Based on the above research, we present a 180 nm process cryogenic clock generator for the control and readout electronics of qubits. In order to meet the stringent requirements of a comprehensive index, a charge pump phase-locked loop architecture is adopted for the clock generator in this design, as shown in Fig. 3a. Additionally, the off-chip loop filter is used since the performance of our on-chip passive devices at low temperatures cannot be accurately predicted. The division ratio of the divider can be adjusted between 16 and 31 using a 4-bit digital signal. Due to freeze-out in the base at 4 K, the severe degradation of the bipolar junction transistor (BJT) characteristics precludes the design of a bandgap reference or low dropout regulator (LDO) to provide circuit bias provision. However, as the operating temperature for this design is fixed at 4 K, the absence of the bandgap reference will not have a significant impact. Besides, the clock generator prioritizes parameters such as frequency tuning range and chip area over-achieving high phase noise performance. Consequently, a ring oscillator-type voltage-controlled oscillator (VCO) is adopted instead of the inductor-capacitor (LC) oscillator type in this design.

Double-Edge Receiving Ring Oscillator The use of ring oscillators in clock generator design is widespread due to the absence of inductors and capacitors. Current-starved ring oscillators are particularly popular due to their simple structure, lower transistor count per unit, and low intrinsic noise. However, their single-ended circuit design makes them vulnerable to substrate or power supply noise. To mitigate this issue, differential ring oscillators have become the more popular choice for VCO designs as they provide superior phase noise performance. It consists of a set of differential pairs, a pair of PMOS load transistors, and a positive feedback load section. Frequency control is accomplished by adjusting the strength of positive feedback, which affects the delay of each stage. The traditional differential ring oscillators only use NMOS transistors to receive the previous stage's signal. However, at cryogenic temperatures, the V_{TH} increases by ~300 mV, which has a negative effect on the turn-on time of the transistors. To address this issue, the cryogenic clock generator utilizes a double-edge receiving ring oscillator structure, as shown in Fig. 3b.

Unlike the conventional structure, the PMOS transistors in the delay unit, i.e. M7 and M8 [Fig. 3c], can receive signals from the stage before the previous module through an additional transmission path (the green path). As a result, the waiting time for PMOS transistors to turn on is significantly reduced during an oscillation cycle, enabling faster signal reversal and increased output frequency without significant power consumption⁴⁷⁻⁴⁸. Additionally, according to phase noise analysis theory⁴⁹⁻⁵⁰, the reduction in rise time results in better VCO phase noise performance by reducing the injection noise of the PMOS transistors. With the utilization of the additional transmission path, the double-edge receiving ring oscillator is able to achieve a frequency range of 370 MHz to 870 MHz, which is nearly double the frequency range of the conventional single-edge receiving oscillator that only ranges from about 133 MHz to 468 MHz, as shown in Fig. 3d.

Charge Pump Fig. 3e shows the detailed structure of the charge pump, which adopts the drain switch structure with current steering switches⁵¹. To suppress the in-band noise of the PLL, the charge pump current is set to 50 μ A. The good DC current matching performance of the charge pump at 4 K is shown in Fig. 3f, with only 2.1 % maximum DC mismatch when the output voltage is between 0.2 V and 1.6 V.

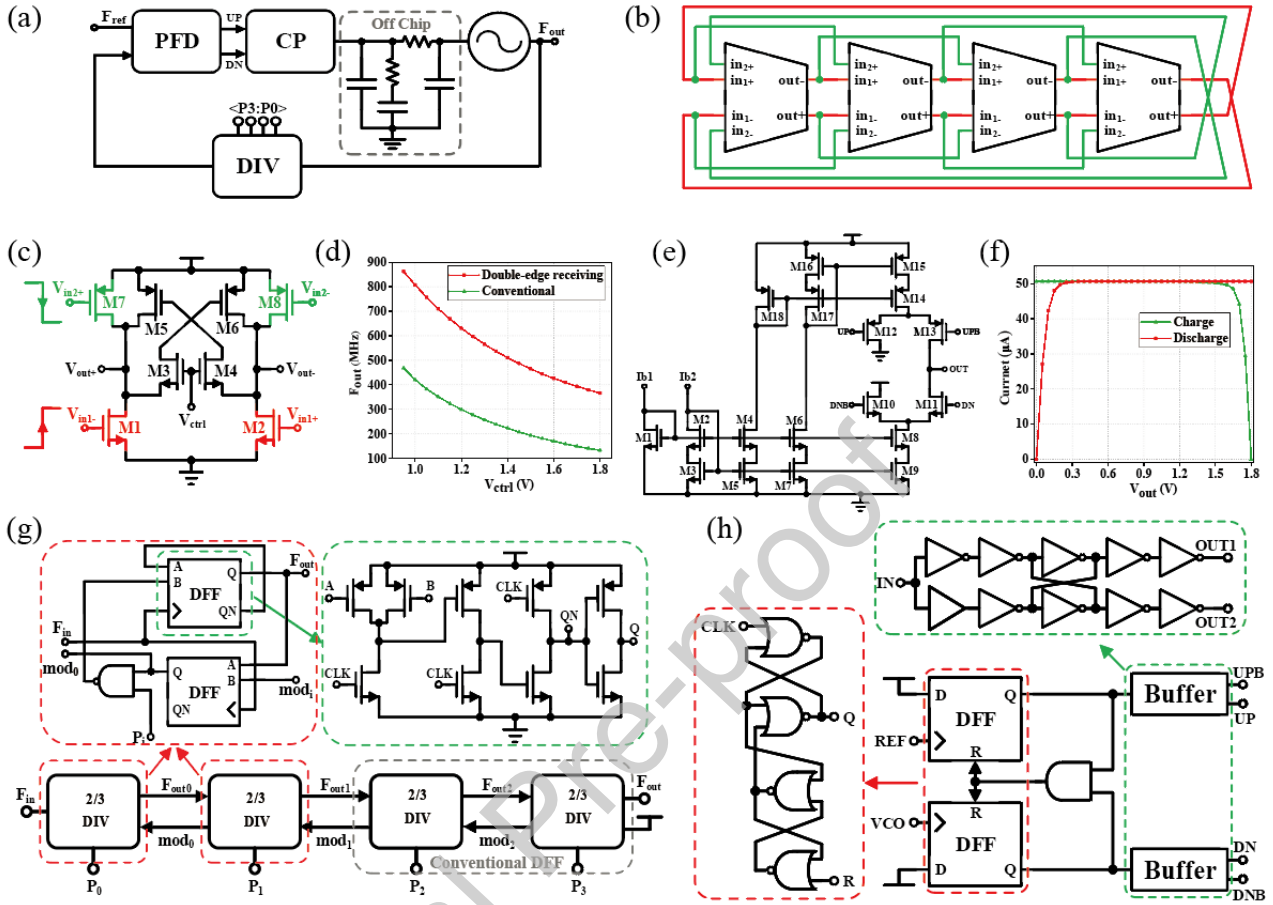


Fig. 3 | Design details of cryo-CMOS clock generator circuit. | **a**, The circuit structure of the cryogenic clock generator. **b**, The circuit structure of the double-edge receiving ring oscillator. **c**, The schematic diagram of the internal module circuit. **d**, Oscillation frequency comparison between the double-edge receiving ring oscillator and the conventional differential ring oscillator. **e**, The circuit structure of the charge pump. **f**, Charging/discharging current versus output voltage. **g**, The circuit structure of the multi-mode frequency divider. **h**, The circuit structure of the phase-frequency detector.

Multi-mode Frequency Divider As shown in Fig. 3g, the multi-mode frequency divider comprises four 2/3 dual-mode frequency dividers, which can enable integer frequency division between 16 and 31. The frequency of the divider is mainly determined by the D flip-flop (DFF). As the maximum output frequency of the VCO approaches 900 MHz, with the possibility of even higher measured frequencies, the first two stages of the dual-modulus prescaler are designed with the true single-phase clock (TSPC) DFF. Incorporating the TSPC-DFF in the design decreases the number of MOS transistor stacks from power to ground, resulting in reduced signal transmission delay and a substantial improvement in operating frequency⁵². Additionally, a faster high-speed TSPC (E-TSPC) flip-flop is employed to guarantee adequate design margin, which reduces one MOS transistor stack compared to the traditional TSPC design. Despite an increase in static power consumption, the circuit speed is subsequently improved. Moreover, the high-speed TSPC flip-flop can reduce the number of logic gates in the dual-modulus prescaler by incorporating “AND” logic into its structure.

Phase-Frequency Detector In modern phase-locked loop designs, the commonly used frequency and phase detector is based on D flip-flops. The detailed structure of the phase-frequency detector (PFD) is shown in Fig. 3h. It consists of two D flip-flops, inverters, the transmission gates that make up the buffer stage, and an AND gate in the reset path. The phase frequency detector employed in this design offers a wide phase detection range and features a simple circuit design. The delay of the reset path is 600 ps at 4 K and thus the minimum pulse of PFD can fully turn on the switches in the charge pump to eliminate the dead zone. Besides, to ensure that the digital differential signal with sufficient driving capability matches the charge pump circuit, a buffer circuit composed of transmission gates and inverters is connected after the PFD. The buffer circuit generates four signals, namely UP, UPB, DN, and DNB, which serve as input signals for the current steering charge pump.

MEASUREMENT RESULTS

The cryogenic clock generator was fabricated in a standard 180 nm bulk CMOS process. The micrograph of the clock generator is shown in Fig. 4a and the overall area without pads is $\sim 415 \times 593 \mu\text{m}^2$. Fig. 4b shows the cryogenic measurement setup and the chip was wire-bonded to PCB and placed in a Lakeshore 4 K cryogenic probe station. Besides, COG-(NP0-)type capacitors, dry tantalum capacitors, and thin film resistors are employed on our low-temperature PCB because they perform relatively stable over a wide temperature range⁵³. The chip power was applied and the output signal was detected via the cryogenic probes (Fig. 4c). Low-dropout regulators (LDOs) commonly use a bandgap voltage reference. However, the bandgap reference is unusable because of the failure of BJTs. Therefore, a separate PCB board is used to solder the test LDOs, which is then connected to the chip test board via coaxial cables. The reference clock is provided by the signal generator and the output signal is observed through an oscilloscope. The signal is also fed into a signal analyzer (Keysight N9030B) to obtain the spectrum and phase noise curve.

Before the overall test, it is necessary to perform a separate test on the VCO. At room temperature, the VCO exhibits a frequency coverage range of ~ 230 -575 MHz within the control voltage range of 0.75-1.8 V, and the frequency can exceed 600 MHz when the control voltage is close to 0. When the output frequency is 232 MHz, the phase noise at 1 MHz frequency offset is -116.12 dBc/Hz, and when the output frequency is 612 MHz, the phase noise at 1 MHz frequency offset is -113.82 dBc/Hz. At 4 K, the VCO covers a frequency range of ~ 330 -900 MHz within the control voltage range of 0.75-1.8 V. The phase noise curve of the VCO is shown for two different frequencies: 359 MHz and 881 MHz. At 359 MHz, the phase noise at 1 MHz offset is -104.08 dBc/Hz, and at 881 MHz, it is -105.9 dBc/Hz at 1 MHz offset.

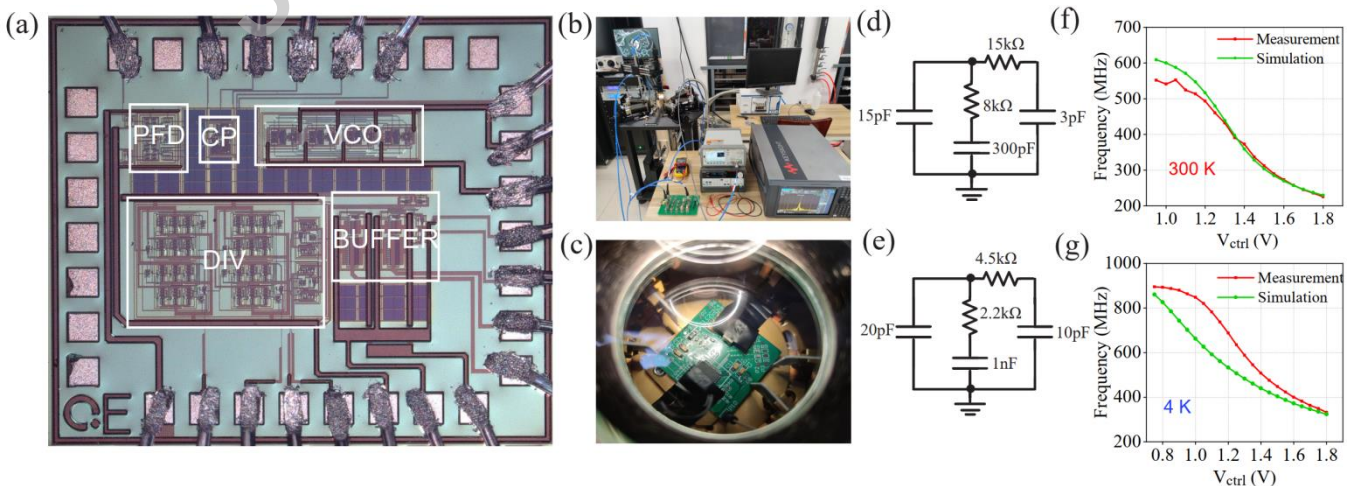


Fig. 4 | Details of measurement. **a**, Chip micrograph. **b**, Cryogenic measurement setup. **c**, Cryogenic PCB in the probe station. Design of loop filter parameters for **d**, room temperature and **e**, 4 K conditions. The measurement and simulation results of the F-V curves of the VCO at **f**, 300 K and **g**, 4 K.

Table 2 | Performance of clock generator with different output frequencies at 300 K

Output Frequency (MHz)	Reference Spur (dBc)	Phase Noise @ 10 kHz (dBc/Hz)	Phase Noise @ 1 MHz (dBc/Hz)
300	-38.84	-94.47	-108.4
400	-35.94	-91.57	-88.19
500	-42.33	-96.17	-105.21
600	-63.16	-89.68	-112.01

Table 3 | Performance of clock generator with different output frequencies at 4 K

Output Frequency (MHz)	Reference Spur (dBc)	Phase Noise @ 10 kHz (dBc/Hz)	Phase Noise @ 1 MHz (dBc/Hz)
450	-38.16	-94.18	-96.53
550	-32.44	-97.09	-103.88
600	-39.32	-95.53	-102.73
650	-32.5	-95.56	-102.37
750	-48.15	-96.41	-109.27
850	-34.61	-74.41	-114.72

The loop filter is a third-order passive structure that uses external resistors and capacitors. According to the frequency-to-voltage (F-V) curve of the VCO, the tuning gain K_{vco} of the VCO at room temperature is ~ 360 MHz/V and ~ 700 MHz/V at 4 K, respectively. Combining with other loop parameters such as the loop bandwidth and charge pump current, the calculated parameters of each component in the loop filter are shown in Fig. 4d and Fig. 4e. The measurement and simulation results of the F-V curves of the VCO are shown in Fig. 4f and Fig. 4g, respectively. At 300 K, the measurement results are in good agreement with the simulation results. At 4 K, although the trend of the F-V curve is consistent, there is a deviation between measurement and simulation results, especially at high frequencies. As we discuss in the modeling section, this deviation can be attributed to the absence of parasitic capacitance correction in our cryo-CMOS model, which is important for high-frequency circuit designs.

The performance measurement results of the clock generator at 300 K and 4 K are listed in Table 2 and Table 3, respectively. When the clock generator is running at the target frequency (600 MHz), the measured spectrum and phase noise of 300 K and 4 K are shown in Fig. 5. The clock generator's 600 MHz output spectrum at room temperature is shown in Fig. 5a, with a reference spur of -63.16 dBc. The phase noise curve is shown in Fig. 5b, with in-band phase noise of -89.68 dBc/Hz @ 10 kHz and out-of-band phase noise of -112.01 dBc/Hz @ 1 MHz. The RMS jitter is calculated to be ~ 9.1 ps (12 kHz-20 MHz) based on the integrated phase noise curve.

The clock generator's 600 MHz output spectrum at 4 K is shown in Fig. 5c, with a reference spur of approximately -39.32 dBc. As shown in Fig. 5d, the phase noise of the clock generator is -95.53 dBc/Hz, -97.07 dBc/Hz, and -102.73 dBc/Hz at 10 kHz, 100 kHz, and 1 MHz frequency offset, respectively. And the RMS jitter is <4.8 ps between 12 kHz and 20 MHz, corresponding to a jitter-power FOM of -211.6 dB. Table 4 shows the detailed performance comparison of the presented PLL. At such a low temperature, i.e. 4 K, the proposed technique still demonstrates good performance, which could potentially be used as a clock generator for ADCs and DACs in the qubit-interfaced cryo-CMOS controllers.

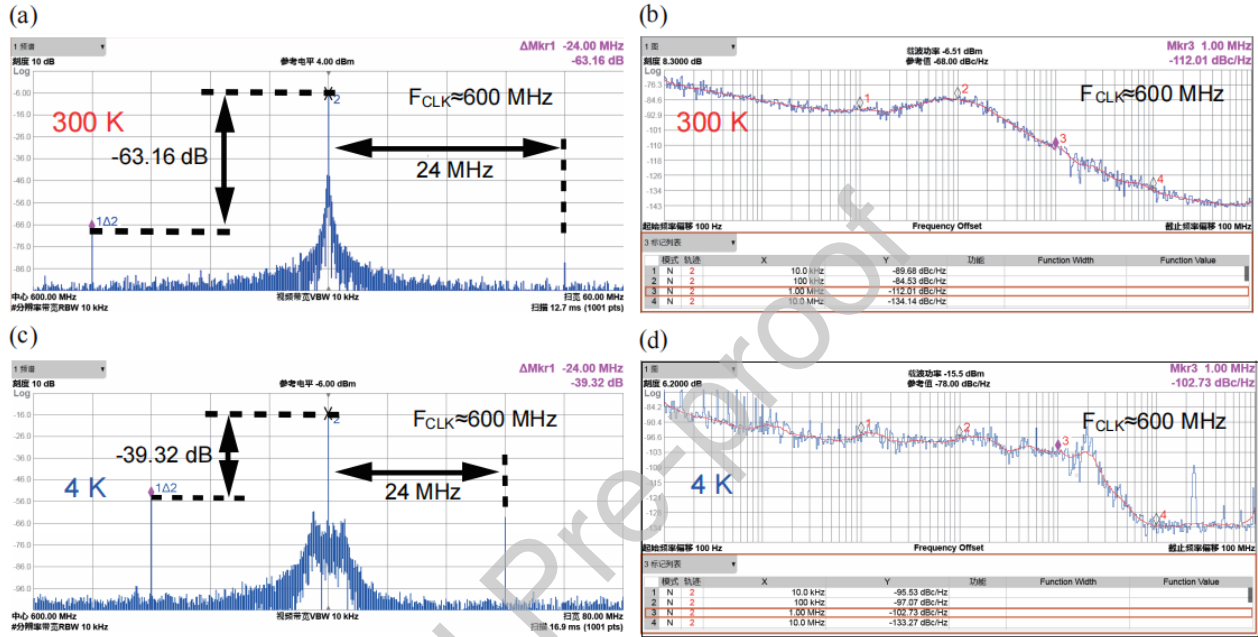


Fig. 5 | Measured spectrum and phase noise of the PLL. **a**, Measured spectrum when the clock generator is running at 600 MHz at 300 K. **b**, Measured phase noise plot when the clock generator is running at 600 MHz at 300 K. **c**, Measured spectrum when the clock generator is running at 600 MHz at 4 K. **d**, Measured phase noise plot when the clock generator is running at 600 MHz at 4 K.

Table 4 | Benchmark with other works.

Specifications	JSSC 2022 ⁵⁴	ASSCC'2019 ⁵⁵	ISSCC 2022 ⁵⁶	ASSCC'2020 ⁵⁷	This work
Temperature (K)	3.5	300	3.5	300	4
Topology	LC+CPPLL	Ring+CPPLL	LC+DPLL	Ring+CPPLL	Ring+CPPLL
Technology (nm)	40	65	40	110	180
Power Supply (V)	N/A	1	1	3.3/1.5	1.8
F_{PLL} (GHz)	12.7	0.432	11.392	1.6125	0.6
FTR (GHz)	10.8-17.3	0.36-0.456	9-13	0.4-1.7	0.45~0.85
Fref (MHz)	50.4	24	356	25	20
PN@1MHz (dBc/Hz)	-115	-98.9	N/A	-100.8	-102.7
RMS jitter (ps)	N/A	N/A	0.274	3.78	4.8
[Int.Bandwidth]	N/A	N/A	[N/A]	[100-40MHz]	[12k-20MHz]

Spur (dBc)	-55.6	-68.9	N/A	NA	-39.32
Area (mm ²)	N/A	0.064	0.068	0.284	0.246
Power consumption (mW)	11.15	1.11	12.5	21.1	30 (with test buffer)
FOM ^a (dB)	N/A	-218.7	-240.3	-215.2	-211.6

$$^a \text{FoM} = 10\lg\left[\left(\frac{I_{\text{RMS}}}{1\text{s}}\right)^2 \cdot \frac{\text{Power}}{1\text{mW}}\right]$$

CONCLUSIONS

This work presents the characterization and modeling of commercial 180 nm CMOS transistors down to 4 K. Based on the proposed model, a 180 nm process clock generator for the control and read-out electronics of qubits is presented. At 300 K with a 600 MHz output frequency, the clock generator achieves a phase noise of -89.68 dBc/Hz at 10 kHz offset, and -102.73 dBc/Hz at 1 MHz offset. At 4 K, the clock generator exhibits an output frequency range of 450-850 MHz. When the output frequency is set to 600 MHz, it achieves a phase noise of -95.53 dBc/Hz at 10 kHz offset, -112.01 dBc/Hz at 1 MHz offset, and <4.8 ps RMS jitter, -39.32 dBc reference spur with 30 mW power consumption (with test buffer), corresponding to a jitter-power FOM of -211.6 dB. With the demonstrated performance, this clock generator contributes to providing a stable local clock signal for AD/DA or digital circuits at cryogenic temperatures in large-scale quantum processors.

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