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Modeling and Simulation of Different System Topologies for DSTATCOM

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Abstract

Power Quality enhancement in a distribution network is achieved by shunt compensation device known as Distribution static compensator (DSTATCOM).In this paper, three different system topologies for Distribution Static Compensators (DSTATCOMs) are modeled and tested using Simulink'SimPowerSystem Toolbox for power system quality studies. Simulation tests on a distribution system, equipped with the unbalanced and non-linear load. With the different system topologies of Distribution Static Compensators (DSTATCOMs) it is observed that power factor can be improved in supply system. The DSTATCOM controls are based on Synchronous Reference Frame control. The modeled DSTATCOM topologies can be used to develop and test different, control strategies and methods for the DSTATCOM. These models can also aid instructors in teaching power quality courses.

Keywords: Distribution Static Compensator (DSTATCOM); Simulink'SimPowerSystemToolbox; Control; Modeling; Simulation; power quality; Synchronous Reference Frame (SRF)

1. Introduction

Distribution static compensator (DSTATCOM) is one of the power custom device that is used for Power Factor Improvement on source side [1]. The DSTATCOM has a Six-leg Voltage-Sourced Converter (VSC) with Insulated Gate Bipolar Transistor (IGBT) as a switching element. Different studies have been performed

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to evaluate the performance or propose control strategies for DSTATCOM to improve its performance [2-10]. Time domain simulations and /or practical experiments have been used to perform these studies.Time domain simulations have been shown to provide accurate prediction of the behaviour of Voltage-Sourced Converter (VSC) based FACTS devices [11]. There are many packages available to model and simulate VSC based FACTS devices such as EMTP, PSCAD, MATLAB/SIMULINK, PSIM. MATLAB/SIMULINK is the most widely used package in engineering sciences since it has many toolboxes that cover all engineering applications [12]. This paper models and simulates three different system topologies for Distribution static compensator (DSTATCOM) using Simulink'SimPowerSystem Toolbox. The DSTATCOM topologies are based on Synchronous Reference Frame (SRF) control [13].

2. System Topologies for DSTATCOM

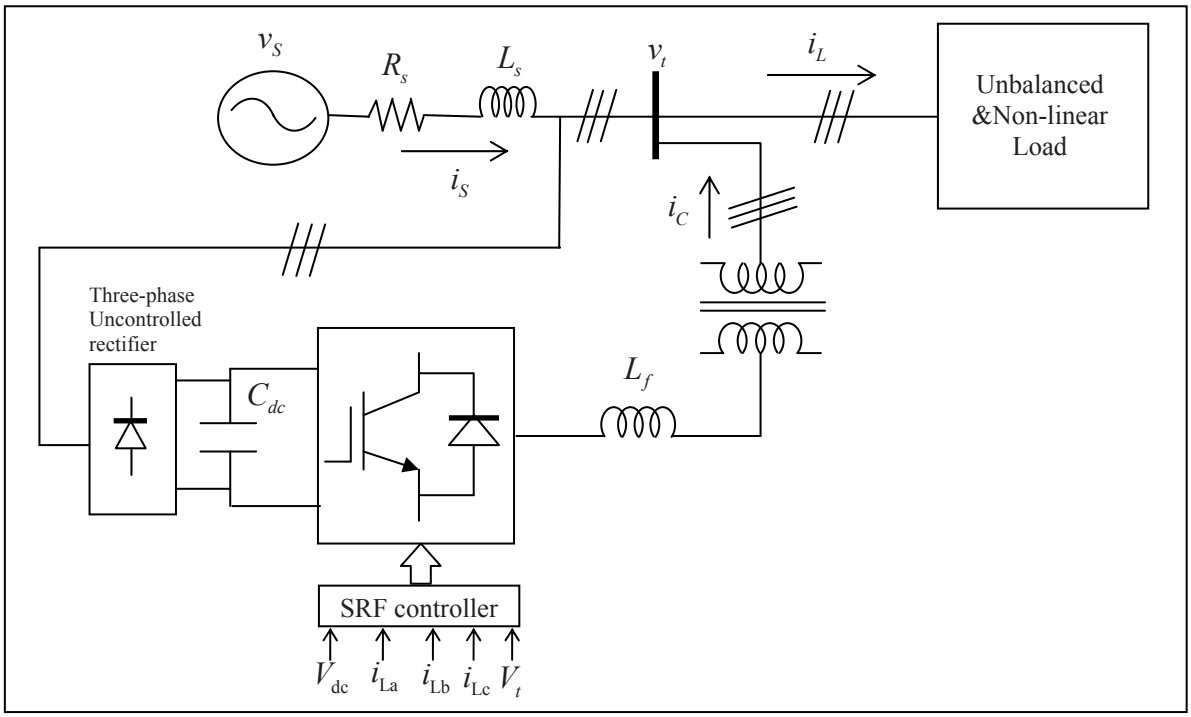
There are different system topologies for the DSTATCOM. Out of which, three are selected and used in this paper. The selected systems are:

1- DSTATCOM with supply side-connected rectifier shown in Fig.1. (System 1)

2- DSTATCOM with load-side-connected rectifier shown in Fig.2. (System 2)

3- DSTATCOM with constant dc voltage shown in Fig.3. (System 3)

The load which has been selected for these topologies are three phase unbalanced R-L load and diode rectifier as a nonlinear load. A step-up transformer for stepping up the voltage has been used in between the STATCOM and distribution system.



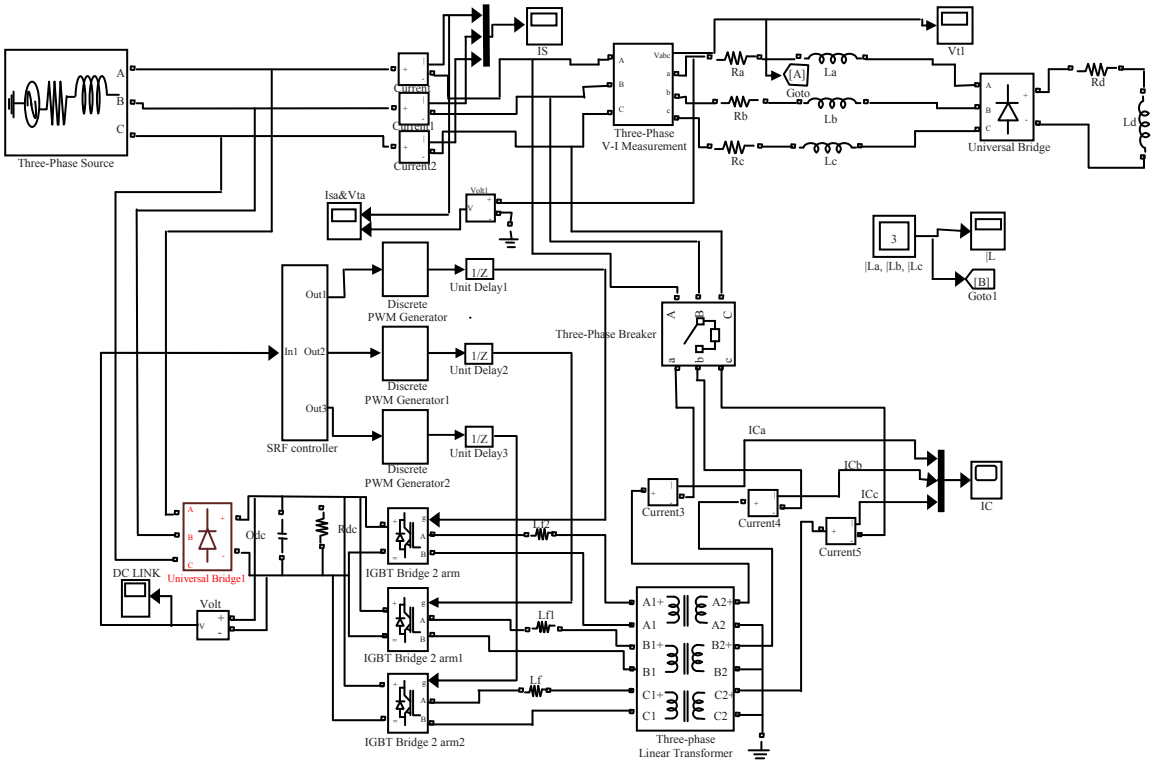


Fig. 1. DSTATCOM with supply side-connected rectifier including Simulink Model

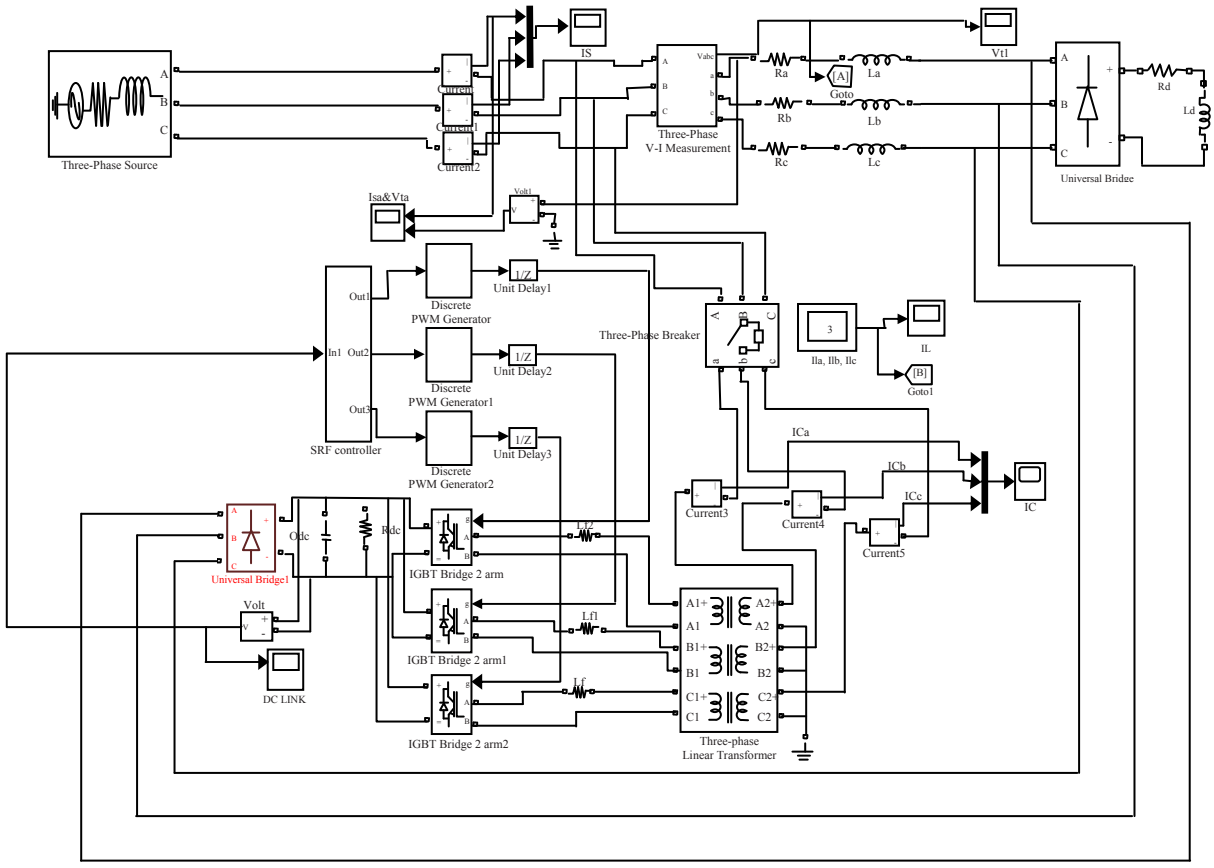
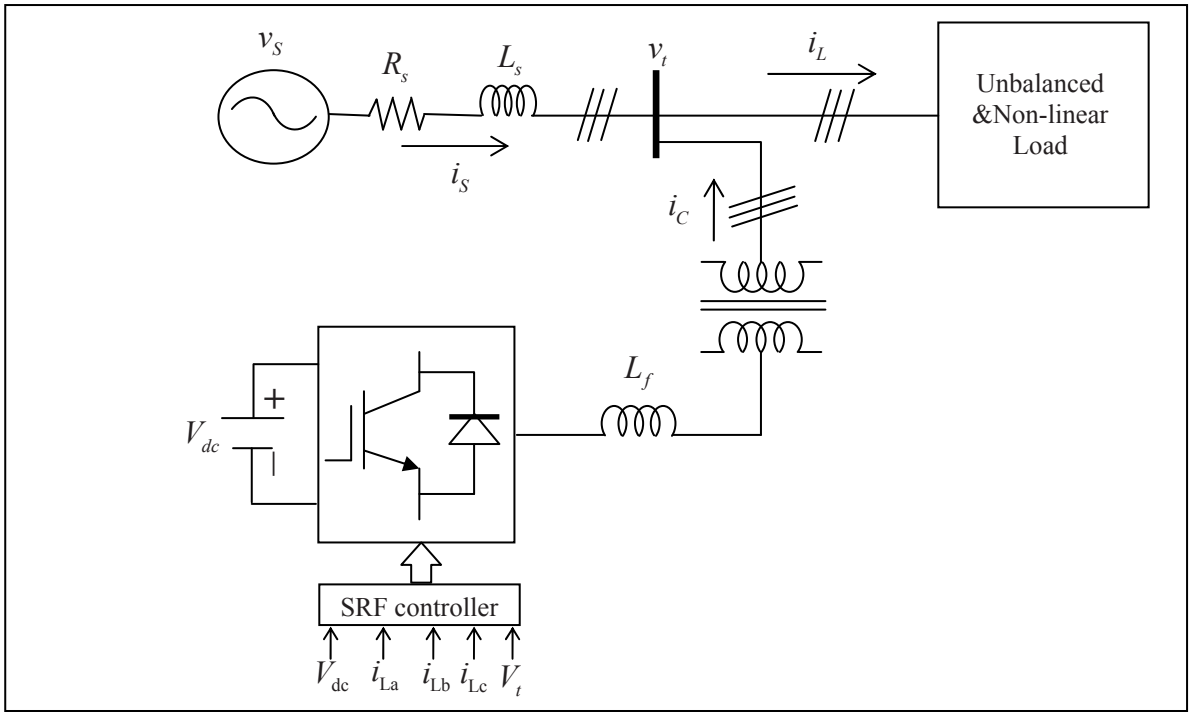


Fig. 2. DSTATCOM with Load side-connected rectifier including Simulink Model


v_S
R_s
L_s
v_t
i_L
Unbalanced
&Non-linear
Load
i_S
i_C
L_f
V_{dc}
+
SRF controller
V_{dc} i_{La} i_{Lb} i_{Lc} V_t

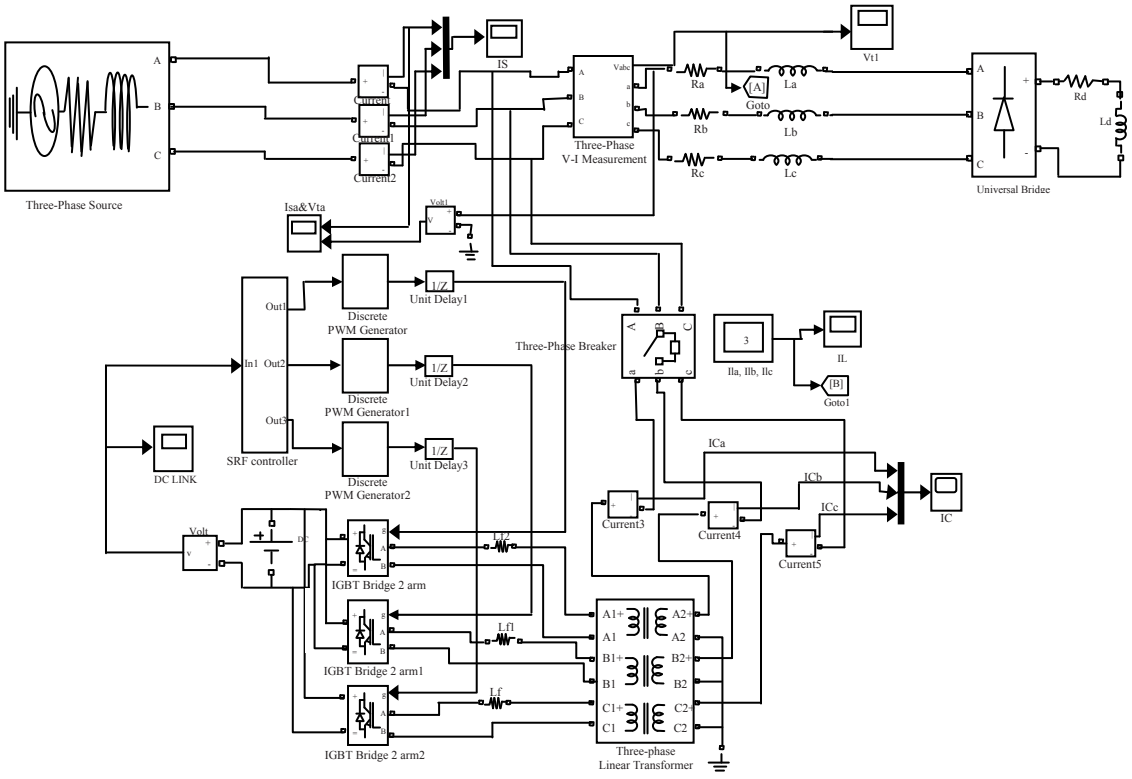


Fig. 3. DSTATCOM with constant DC voltage including Simulink Model

3. Control Scheme

DSTATCOM Topologies are controlled using Synchronous Reference Frame (SRF) theory.

The three phase load current in *a–b–c* frame are converted to the two phase load current in *d–q* frame using the following formulation

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \frac{2}{3} \begin{Bmatrix} \cos \omega t & \cos\left(\omega t - 2\pi/3\right) & \cos\left(\omega t + 2\pi/3\right) \\ \sin \omega t & \sin\left(\omega t - 2\pi/3\right) & \sin\left(\omega t + 2\pi/3\right) \end{Bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} \overline{i_{Ld}} \\ \overline{i_{Lq}} \end{bmatrix} = \begin{bmatrix} G(s) i_{Ld} \\ G(s) i_{Lq} \end{bmatrix} \tag{2}$$

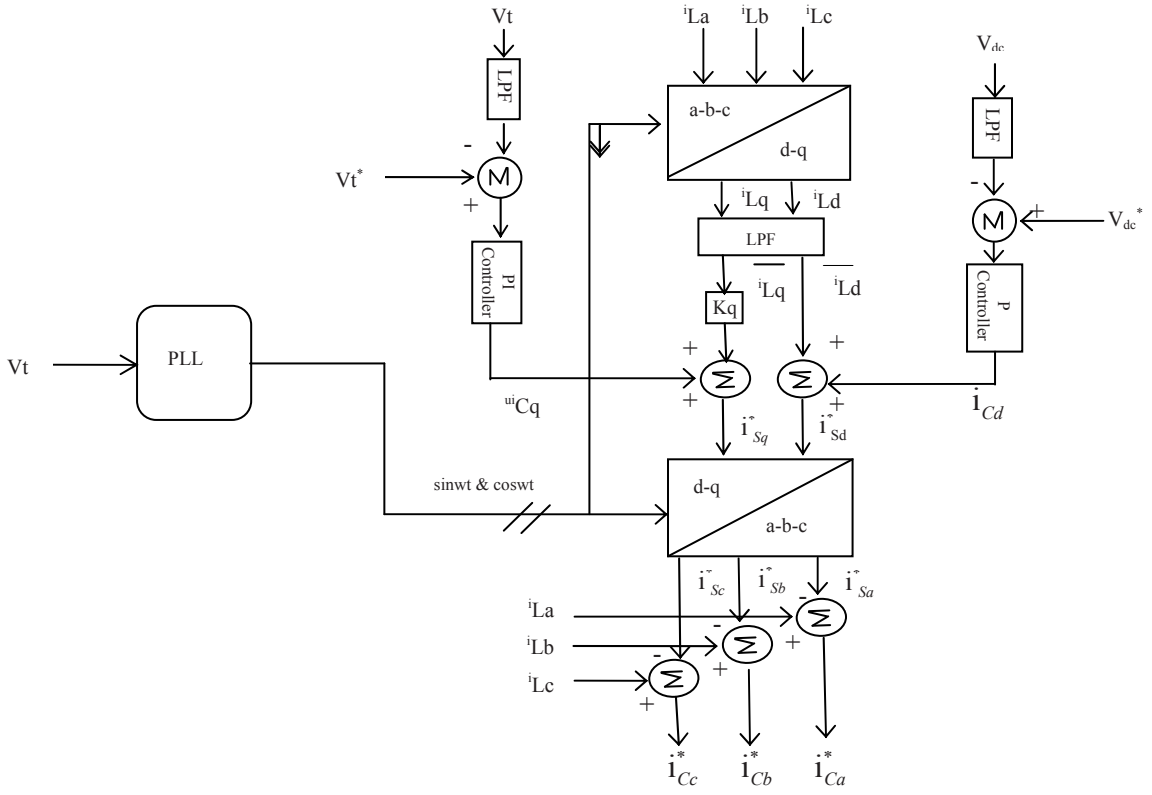


Fig. 4. Block diagram for Synchronous Reference Frame (SRF) Control Scheme

Gain K_q is defined as the ratio of Q_S^* to $\overline{Q_L}$ and its value will be Zero for Power Factor Improvement.

The d-q component of reference source currents are obtained as

$$\begin{aligned} i_{Sd}^* &= \overline{i_{Ld}} + i_{Cd} \\ i_{Sq}^* &= K_q \overline{i_{Lq}} + ui_{Cq} \end{aligned} \tag{3}$$

The d-q component of reference source currents are converted to the three phase a-*b*-*c* frame using the following formulation

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = 2/3 \begin{Bmatrix} \cos\ \omega t & \sin\ \omega t \\ \cos\left(\omega t - 2\pi/3\right) & \sin\left(\omega t - 2\pi/3\right) \\ \cos\left(\omega t + 2\pi/3\right) & \sin\left(\omega t + 2\pi/3\right) \end{Bmatrix} \begin{bmatrix} i^*_{sd} \\ i^*_{sq} \end{bmatrix} \tag{4}$$

The desired compensator currents can be obtained as

$$\begin{aligned} i_{Ca}^* &= i_{La} - i_{Sa}^* \\ i_{Cb}^* &= i_{Lb} - i_{Sb}^* \end{aligned}$$

$$\dot{i}_{Cc}^{*} = \dot{i}_{Lc} - \dot{i}_{Sc}^{*}$$

4. Simulation Results

The three DSTATCOM topologies have been simulated for the power factor improvement mode. The total simulation period is 1.0 s. Based on the simulation results,the following analysis can be prepared:

(1)The simulation results of sysem1 are depicted in Fig. 6. Load current is unbalanced and non-sinusoidal. Compensator current is sinusoidal in nature. The phase angle between source current and Terminal voltage are Zero degree. This ensure Power factor will be unity i.e. Power factor can be improved after the DSTATCOM is switched on. The dc link voltage V_{dc} as shown in Fig continues to increase until the DSTATCOM is switched on and finally reach the steady state value of 500V. It starts settling after 0.2 s. The dc voltage V_{dc} starts to build up on the dc capacitor C_{dc}.

(2)The simulation results of sysem2 are depicted in Fig.7. The waveform of Load current, Compensator current, Source current and Terminal Voltage are same as in Fig.6 but the magnitude of load current is comparatively increased. Power factor can be improved after the DSTATCOM is switched on. The DC link voltage Vdc exponentially increasing with time as shown in Fig. The DC link voltage is not maintained constant but tending towards the value of 250 V.

(3)The simulation results of sysem3 are depicted in Fig.8. The waveform of Load current, Compensator current, Source current and Terminal Voltage are same as in Fig. 6. Power factor can be improved after the DSTATCOM is switched on. The DC link voltage is maintained constant at 500 V before and after the DSTATCOM is switched on. This allows the DSTATCOM to improve Power Factor with almost no interruption in the load current.

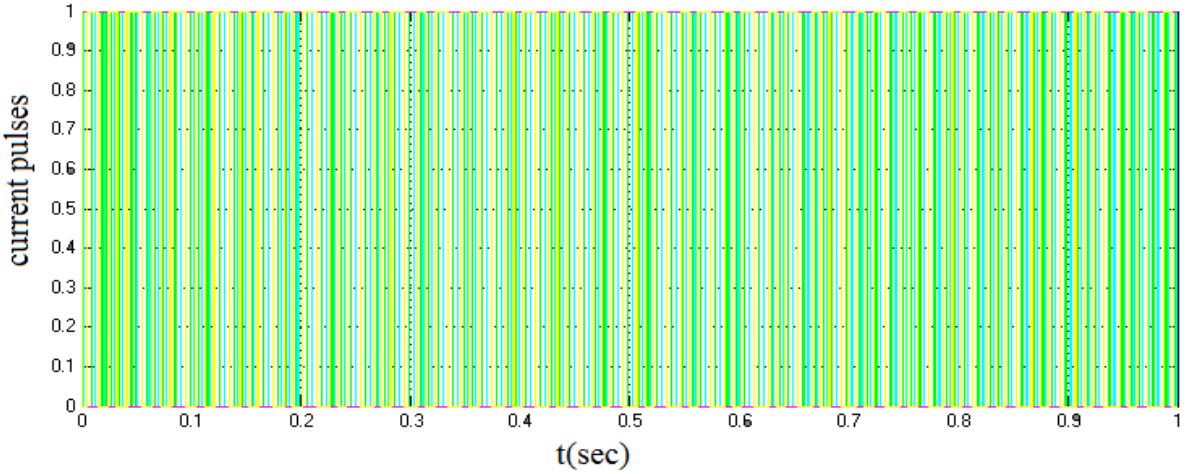
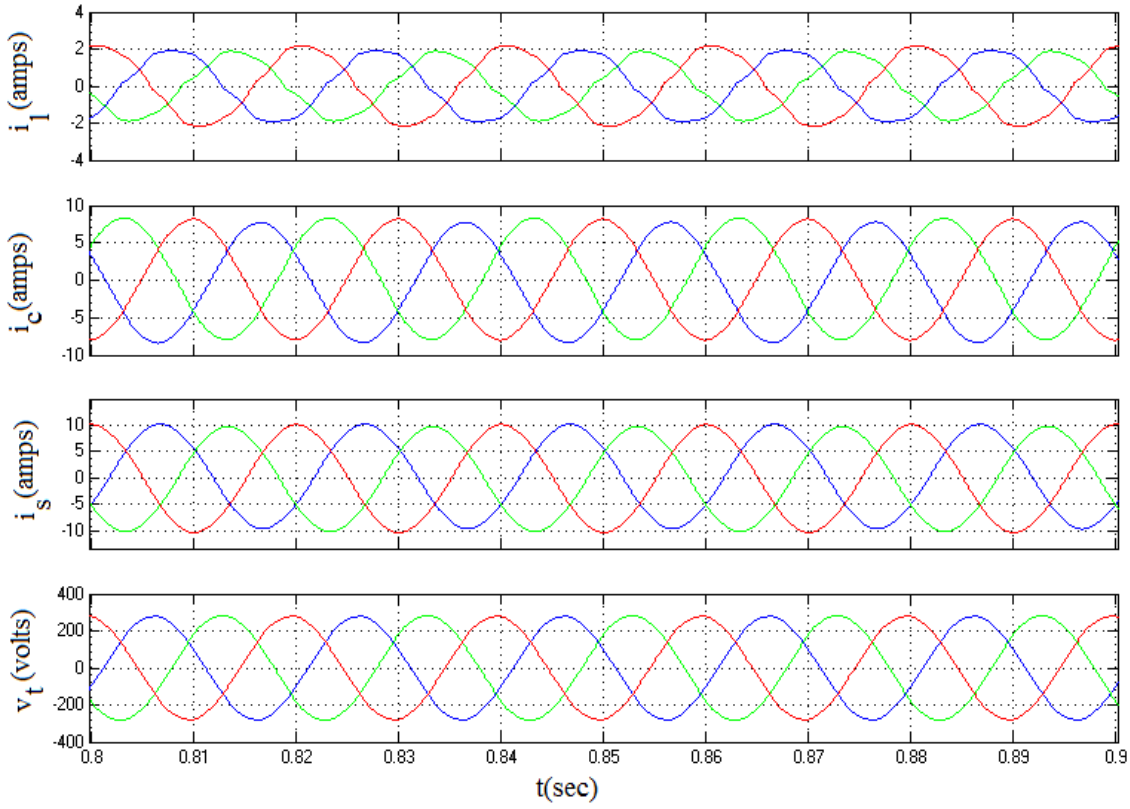


Fig.5. PWM pulses for IGBT



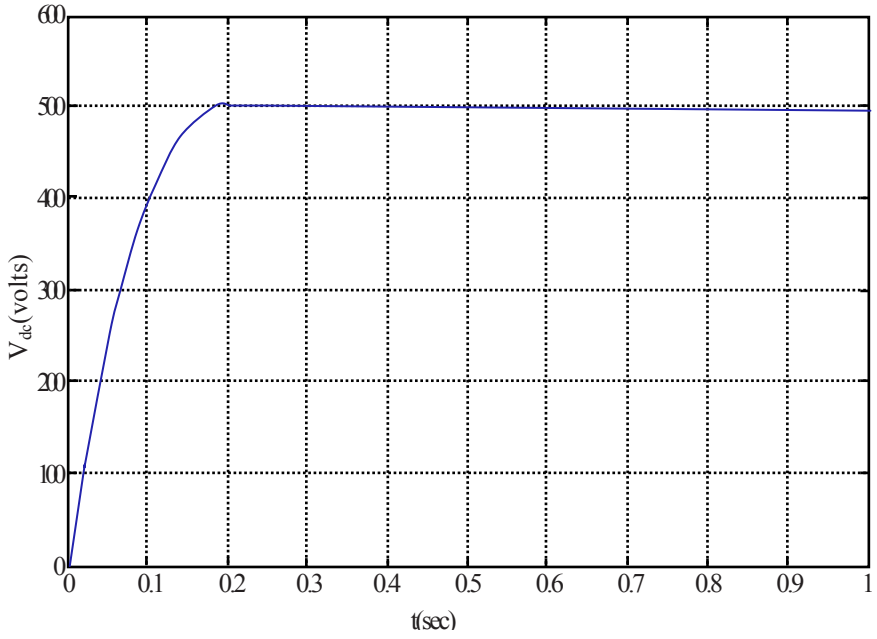
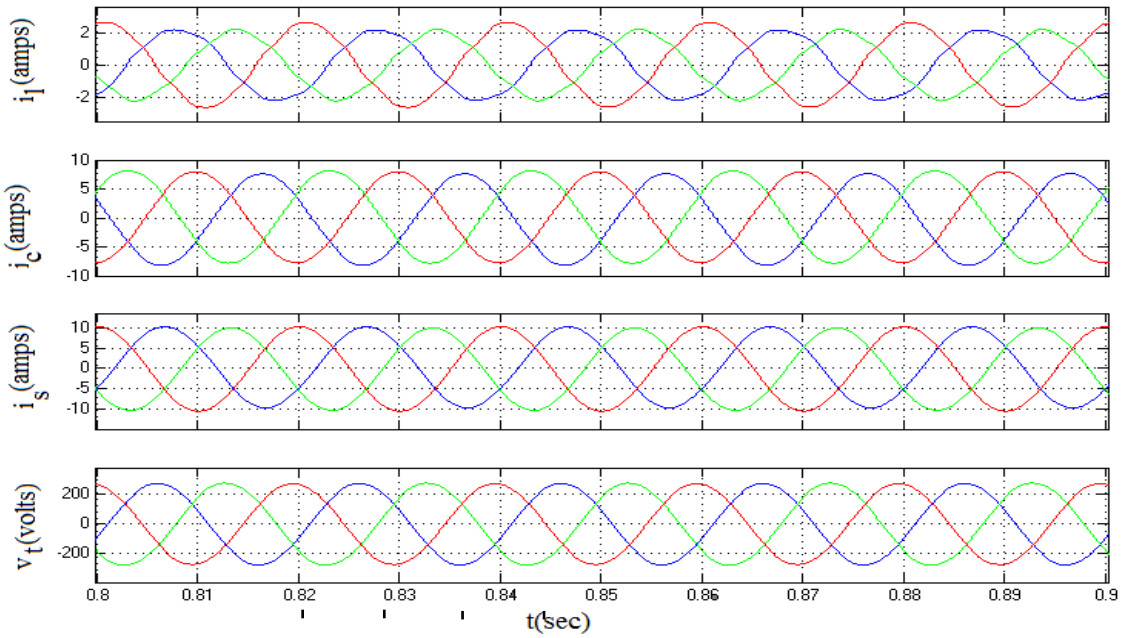


Fig. 6. System response with Power Factor Improvement (system1)



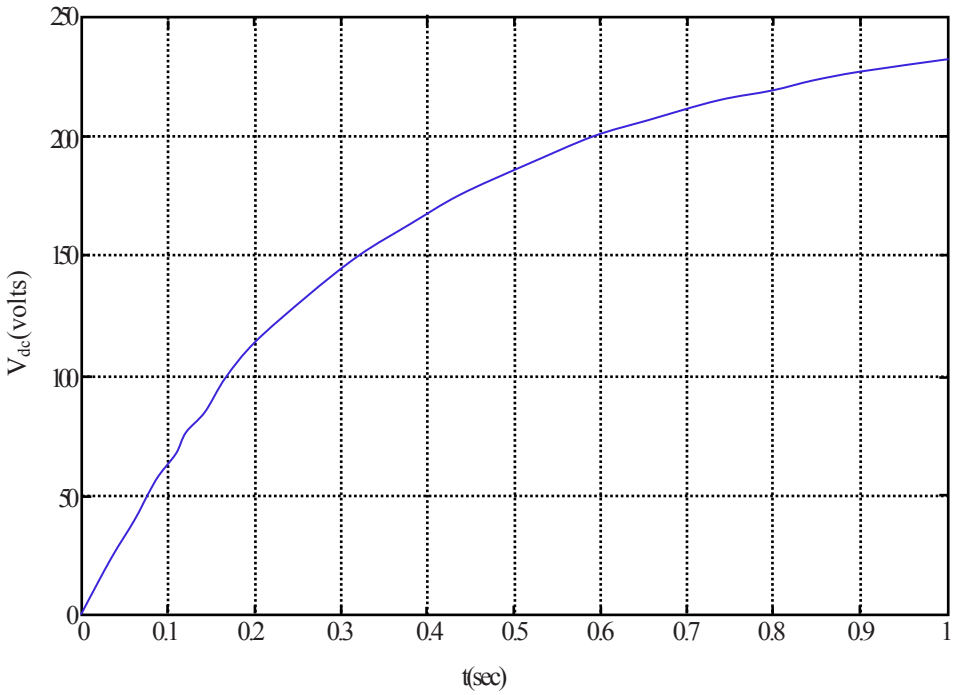
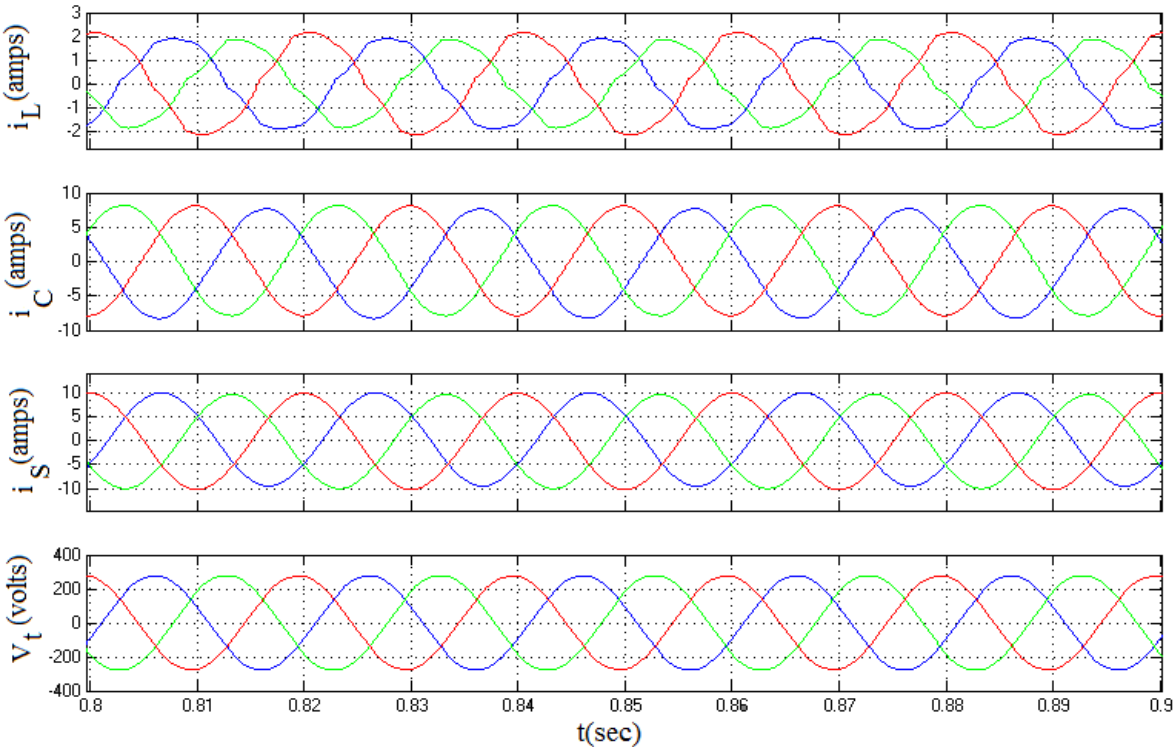


Fig. 7. System response with Power Factor Improvement (system2)



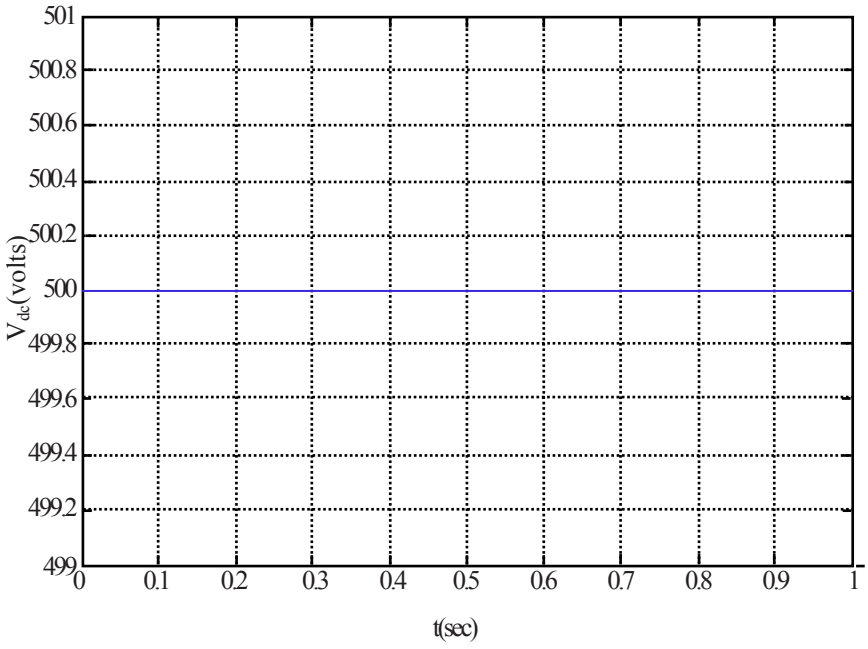


Fig. 8. System response with Power Factor Improvement (system3)

5. Conclusion

This paper has developed models for different system topologies of the Distribution Static Compensator (DSTATCOM) using Simulink'SimPowerSystem Toolbox. The control of the DSTATCOM system topologies is based on Synchronous Reference Frame control. Time domain simulations have been used to verify the operation of these models. These models can be easily modified to:

1- Perform different types of power quality studies in a user friendly simulation environment for teaching and researching.

2- Test control strategies and methods for the DSTATCOM.

3- Develop models for other system topologies of the DSTATCOM, which is not considered is this paper, by modifying the existing modeled topologies.

Acknowledgments

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APPENDIX

AC line voltage: V_{LL}= 415 V, 50 Hz, Source inductance and resistance: Ls= 42 mH, Rs= 1.57 Ω

Unbalanced R-L Load at each phases: Phase a- 45 Ω , 195 mH, Phase b- 70 Ω , 220 mH,

Phase c- 30 Ω , 170 mH

Diode resistance and inductance- 120 Ω , 35 mH

Proportional controller gain: Kp= 0.6 , Proportional gain = -0.2 , Integral gain = -40

DC Voltage : V_{dc} = 400V, DC capacitance: C_{dc} = 3500 μF, DC resistance: R_{dc} = 5500 Ω
Filter inductance: L_f = 5.0 mH, PWM switching frequency: 20 kHz