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AASRI Procedia 7 (2014) 62 – 67

AASRI Procedia

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2013 2nd AASRI Conference on Power and Energy Systems

ZVS Multi-Output Push-Pull QRC Using Analog Controller UC3825 for Low Power Applications

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Abstract

The analysis, design and implementation of a zero voltage switched multi output push-pull topology is presented in this paper. To double the secondary output a voltage doubler circuit is introduced in each secondary winding of the multi output transformer. The voltage doubler introduced also helps in obtaining ZVS in the passive switches at the secondary of the transformer. To further add on the advantage of increased power packing density UC3825 an analog controller is deployed in the hardware prototype to regulate the output voltage against supply and load disturbances

Peer-review under responsibility of Scientific Committee of American Applied Science Research Institute

Keywords: Zero Voltage Switching(ZVS); Voltage Doubler(VD); Quasi resonant converter(QRC); Analog controller

1. Introduction

Hard switched DC-DC converters are nowadays replaced by soft-switched converters. Though they have increased components like resonant inductor (ZCS) and capacitors (ZVS) they offer less voltage/current stress across the switches. Hence the advantage of isolation and less switch stress promote the resonant converters

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Peer-review under responsibility of Scientific Committee of American Applied Science Research Institute
doi:10.1016/j.aasri.2014.05.030

for SMPS applications [1] – [7]. To add-on the advantages mostly high switching frequencies are selected, to reduce the size of the magnetic components [4] – [7]. Thus several new topologies were reported in literature with high frequency soft switching techniques in all types of isolated DC-DC converters [13] – [15]. Out these converters reported in literature push-pull converter is best opted for low voltage application due to features like good transformer utilization factor, isolation, doubled output power when compared with its forward converter counterpart [5] – [7]. Furthermore to reduce the ringing and oscillation in the secondary diodes, voltage doubler circuits were introduced in the secondary for doubling the secondary voltages and for reducing the stress across the diodes [8] – [10]. To this original converter i.e. the primary ZVS push pull converter with secondary voltage doubler, is added an extra secondary winding to obtain a multi output topology. This proposed multi output topology with secondary voltage doubler and primary ZVS technique is designed and simulated in PSIM. The simulation results obtained are compared with the theoretical waveforms of the proposed converters. To obtain a regulated output, a compact controller UC3825 analog controller IC is utilized to regulate the output [11] – [12]. The closed loop hardware implementations details are presented in detail in this paper to validate the proposed topology.

2. Proposed Circuit

2.1 Operation of the Proposed Cirucit

The proposed multi output ZVS push-pull converter is shown in Fig.1. C_{r1}, C_{r2}, C_{r3}, C_{r4}, L_{r1}, L_{r2}, are resonant capacitors and resonant inductors respectively. C_{f1}, C_{f2} and L_{f1}, L_{f2} are the filter components Resonance occurs in both primary and secondary side of the converter i.e., between (L_{r1} & C_{r1}) and (L_{r2} & C_{r2}) in the primary side and between magnetizing inductance of secondary1 & C_{r3} and between magnetizing inductance of secondary 2 & C_{r4} in secondary side. This converter further adds the advantage of increased number of secondary output by adding extra winding in the transformer secondary of the single output converter. The operation of the converter circuit is similar to that of a single output converter and is explained in 6 different modes in [10]. It consists of a multi output pushpull transformer with voltage doubler circuit in each secondary. The output voltage is sensed and fed to an analog controller to obtain the required pulses for the converter through the driver cum opto-coupler circuit.

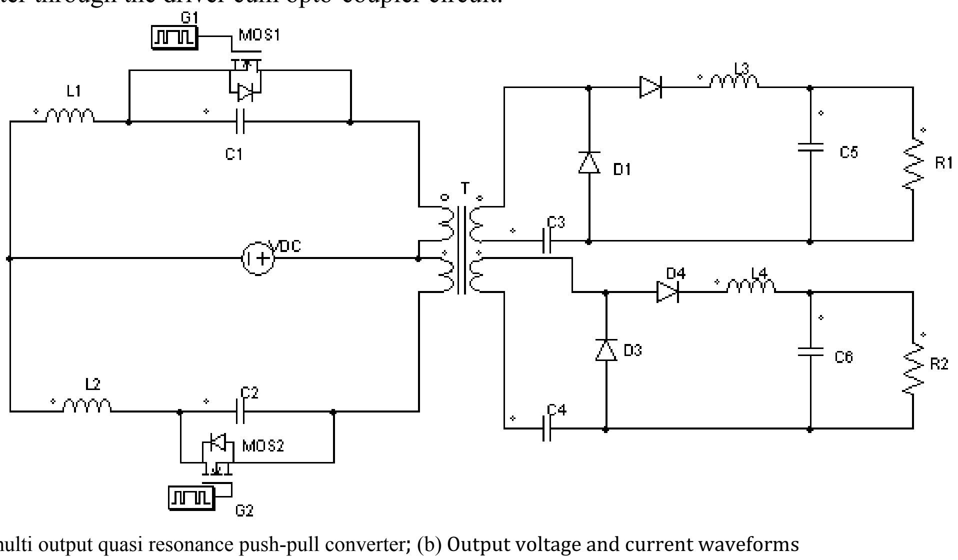


Fig. 1 ZVS multi output quasi resonance push-pull converter; (b) Output voltage and current waveforms

2.2 Specifications and Design

Specifications of the converter are : Switching frequency (f_s) :- 50 kHz, Output power (P_0) :- 3.5 W, Input voltage (V_s) :- 15±15%, Output voltage 1 (V_{01}) : - 5 V, Output current 1 (I_{01}) :- 0.5 A, Output voltage 2 (V_{02}) :- 3.3 V, Output current 2 (I_{02}) :-0.33 A.

The data for a sample design of 3.5W, 50 kHz multi output ZVS push-pull converter are considered as given in specification.

The condition for ZVS is $I_m Z_0 > V_S+V_0 \Rightarrow Z_0= 40$ *(1)*

$$Z_0 = \sqrt{\frac{L_r}{C_r}} \tag{2}$$

Resonant Frequency, $f_0 = 2.5\times f_S = 125$ kHz

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{L_r C_r}} \tag{3}$$

Cut-off frequency, $f_f = 0.1 f_S$ *(4)*

From equations (1) to (4), $C_r = 0.33\mu F$, $L_r = 60\mu H$, $C_f = 220\mu F$ and $L_f = 10\mu H$.

3. Closed Loop Hardware Results

Hardware implementation of closed loop multi-output push-pull converter is carried out with UC 3825 IC with the designed values of components as explained in section 2.2. The hardware implementation results are presented and discussed in detail.

Stability of the system can be improved using a PWM controller along with type 3-error amplifier. The PWM controller IC UC 3825 is selected, for obtaining complementary outputs of same frequency and duty cycle. By adding compensation to the error amplifier, stability can be achieved for the converter. The phase margins of 45^0 to 60^0 are considered secure value for a stable system. An error amplifier value is designed in such a way that total gain cross over frequency crosses at -1 slope at a preferred value. Hence type 3 error amplifiers are selected, which consist of 3 pole and 2 zeros, including one pole at origin. Desired duty cycle and frequency can be obtained by selecting proper resistance (R_t) and capacitor(C_t). The R_t and C_t values are calculated as given below.

$$R_t = \frac{3V}{10mA(1-D_{\max})} = 3.3K\Omega \qquad C_t = \frac{1.6D_{\max}}{R_t f} = 4.36nF$$

3.1 Rated Output Condition

The first and second output voltage and current of (5V, 0.5A) and (3.3V, 0.33A) respectively obtained at rated conditions are as shown in Fig 2(a) and (b). The resonant capacitor voltages with the corresponding gating pulses are as shown in Fig.3 (a) and (b). It is observed from the figure that the peak capacitor voltages of 1 and 2 are 59 and 66V respectively. The hardware pulses produced from the PWM controller IC is fed to an optocoupler for isolation. It is observed from the figure that the duty ratio of the pulses is 46% and frequency is 50 kHz. Peak voltage is found to be 14.4V for the obtained pulses.

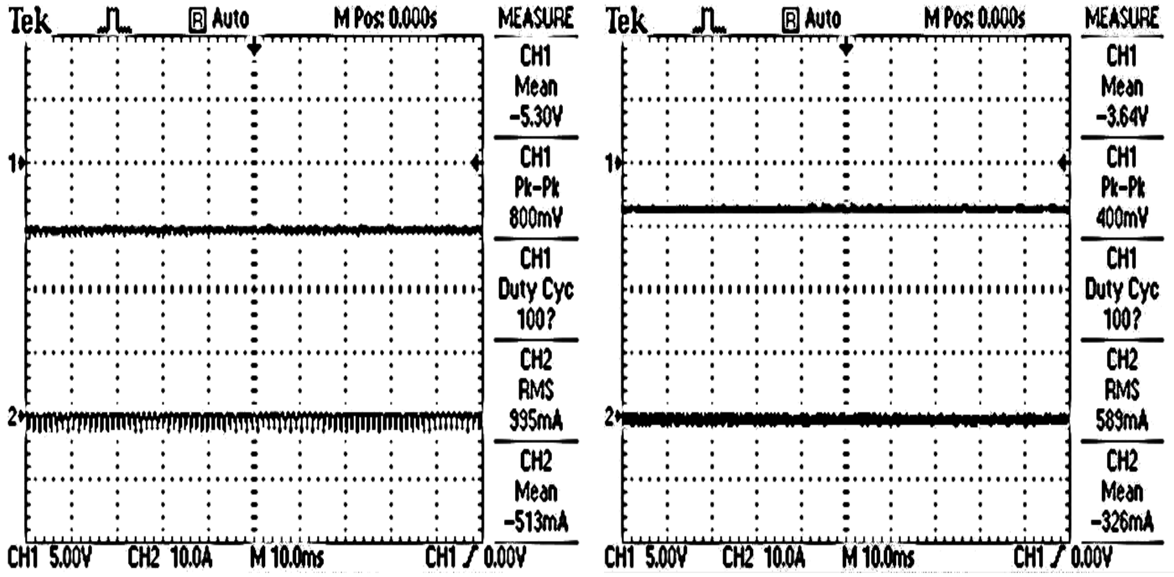


Fig. 2 (a) First Output voltage (V_{01}), current (I_{01}); (b) Second output voltage (V_{02}), current (I_{02}).

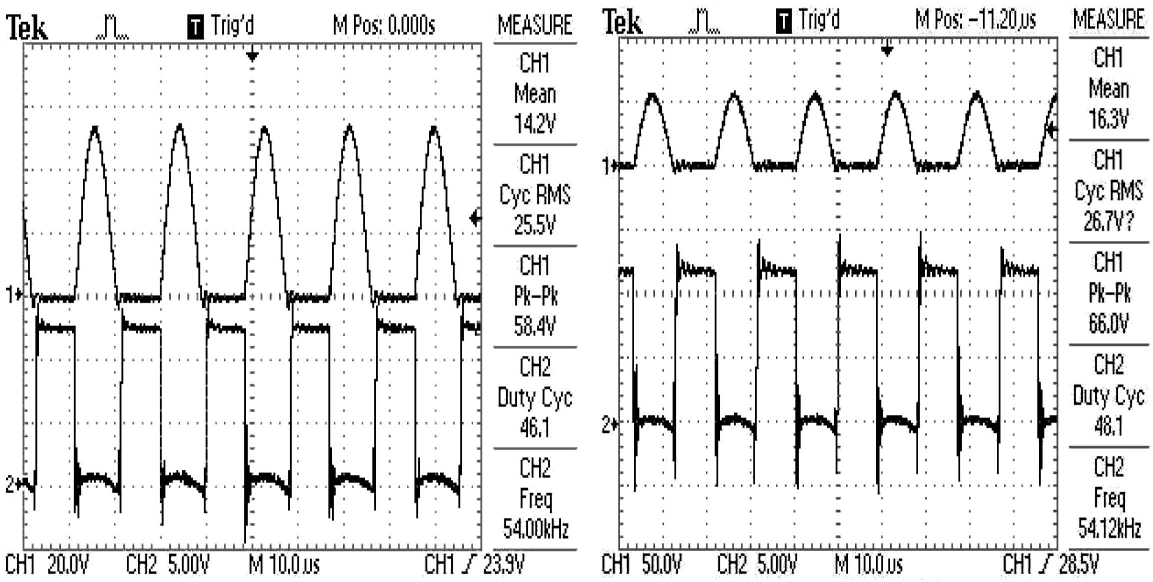


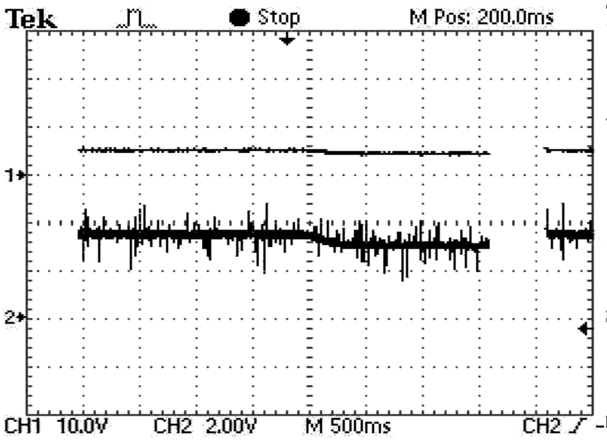
Fig. 3(a) Waveforms of switch 1 pulse, V_{cr1} ; (b) Switch 2 pulse, $V_{cr2.}$

3.2 Line Transients

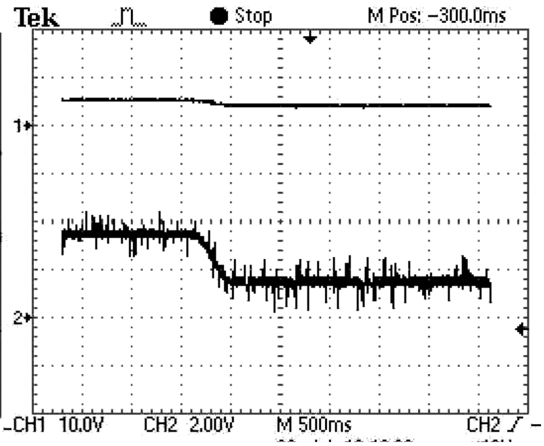
The output voltages corresponding to variation in supply voltage are shown in Fig 4(a). Change in output voltages from 5V to 4.95V and 3.6V to 3.4V are observed for a supply voltage decrease from 15V to 13V in fig.4 (a). For increase in supply voltage from 15V to 17V, it is observed that the voltage1 settles at 5.05V from 5V and correspondingly voltage2 settles at 4V from 3.6V respectively.

3.3 Load Transients

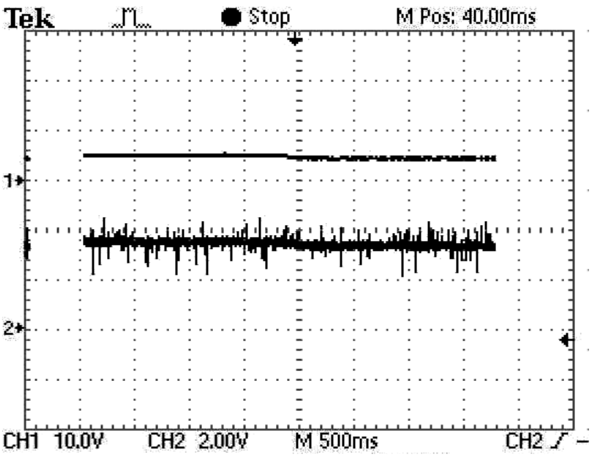
Closed loop implementation response of the proposed multi-output push-pull converter for load transients are presented and discussed in this section. Figure 4(b) shows both the output voltage waveforms for decrease in load resistor2 from 10Ω to 7Ω. For load resistor1 variations also similar waveforms were noted as shown in fig 4(c). By decreasing the load1 from 10Ω to 7Ω, the variations in load voltage1 observed was very small and are also within the specifications considered (i.e) a regulated output voltage is obtained. The output voltages were observed to vary when the load resistance was decreased/increases in the case of open loop implementation, but for closed loop, the outputs are almost constant for load variation as shown in figure 4(b) and (c). From the results it is observed that the output 1 is regulated for all the load changes applied because of the feedback loop provided through the analog controller IC UC3825. A slight variation in second output voltages is observed for its own load changes. Figure 4(d) depicts the hardware prototype developed.



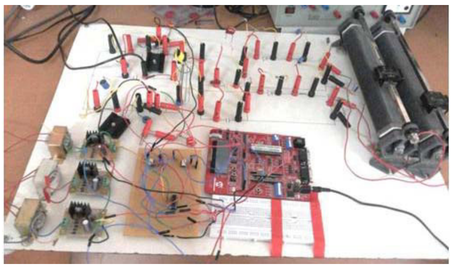
(a)



(b)



(c)



(d)

Fig.4. Output voltages for (a) decrease in supply voltage; (b) decrease in second load resistance; (c) decrease in first load resistance; (d) Hardware Prototype..

4. Conclusion

Design, simulation, analysis and closed loop implementation of a 3.5W primary ZVS multi output pushpull converter for high frequency application with secondary voltage doubler is discussed in this this paper. The following are the list of selection parameters along with their advantages listed: High frequency operation - Reduction in the size of magnetic components used like inductors, transformers and capacitors leading to compactness, Multiple secondary winding – Isolated multi output of different rating, Analog controller UC3825 – Regulated output for load and line variations, Voltage doubler circuit – Doubles the secondary voltages, ZVS in primary circuit – Reduces the switching losses in the primary switches, ZCS in secondary circuit – Reduces oscillation and voltage spike in diodes, which reduces the stress across the diodes.

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