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Error Threshold for Individual Faulty Gates Using Probabilistic Transfer Matrix (PTM)

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Abstract

In the progression from CMOS technology to nanotechnology, being able to assess reliability of nano-based electronic circuits is fast becoming necessary. Due to this phenomenon, several computational-based approaches have been proposed for the reliability assessment of nanotechnology-based circuit systems. In quantifying reliability measure of the desired circuit system, faulty gates are considered as the most active part of the system. To have reliable circuit system, apart from its faulty gates, the size of error, p, in those faulty gates has to be lesser than a threshold, $\varepsilon*$. In other words, for the individual faulty gates to function reliably, the parameter interval of error in those faulty gates has to be $0 \le p < \varepsilon*$, based on their respective gate error thresholds. This hypothesized that reliability of the desired circuit system does not only depend on its faulty gates, but it also depends on the error threshold of those faulty gates above which no reliable computation is possible. Therefore, there is a need to compute the exact error thresholds for individual faulty gates above which no circuit made up using those gates can calculate reliably. This paper shows the employment of Probabilistic Transfer Matrix (PTM) model in deriving the exact error threshold for individual faulty gates. The employed methodology provides simple and powerful analytic method to analyze reliability measure of nanotechnology-based circuit systems.

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1. Introduction

As CMOS technology scales down to nanometric scale, inconsistency in transistor performance will continue to increase, making the transistors less and less reliable.

This occurrence will subsequently affect the performance and downgrade the reliability of the desired circuit system made-up of these transistors [1]. Inconsistencies in the performance of transistors occur due to manufacturing ambiguity in the CMOS production process. Due to this physical-level of characteristics, non-deterministic behaviors will continue to develop in the circuit system which naturally affects the evolving technologies to have restrictions to operate reliably. Therefore, reliability has turn out to be the most important subject in the design entry of circuit systems and thus offer new challengers to circuit designers. Various probabilistic design methodologies have been implemented to assemble reliable circuit systems built out using unreliable devices [2, 3]. Due to the demand of having reliable design, a number of computational methodologies have been also proposed to assess reliability of nanotechnology-based circuits [4-12]. They are Probabilistic Transfer Matrix (PTM) [4-7], Probabilistic Gate Model (PGM) [8-10], Boolean Difference-based Error Calculator (BDEC) [11] and Bayesian Network (BN) [12].

Reliability of a desired circuit system is not only affected by its faulty gates, but it also depends on the size of the error, p, in those faulty gates. In order for the system to be reliable, the size of the error in its faulty gates has to be lesser than a threshold, $\varepsilon*$. The upper-limit of error in those faulty gates is increasingly important subject to be considered in the fault tolerance computation as it provides the exact bounds above which no circuit made up using those faulty gates can compute reliably. For this purpose, we have shown here that apart from computing reliability of the desired circuit system, Probabilistic Transfer Matrix (PTM) has also the ability to compute the fundamental error threshold for individual faulty gates.

Section 2 outlines Probabilistic Transfer Matrix (PTM). Section 3 exhibits the employment of PTM in deriving the exact error threshold for individual faulty gates. Extensive simulation results and discussion are shown in Section 4. The paper is concluded in Section 5.

2. Probabilistic Transfer Matrix (PTM)

A relationship between input and output values for the operation of an integrated nano-based electronic circuit can be characterized by its truth table. Under certain circumstances, an incorrect output value can be generated by its input value. If we can identify how frequent this phenomenon is likely to occur, then we can demonstrate this occurrence using Probabilistic Transfer Matrix (PTM) [4-7]. PTM is represented in matrix form where column and row indicate input and output values respectively. For demonstration purpose, PTM for a two-input AND gate is shown in Eq. 1. The symbol p in Eq. 1 denotes the probability for wrong output value; sometimes we can also refer p as gate error probability. For a logic gate with $p = 0$, its PTM is termed as Ideal Transfer Matrix (ITM), in which the correct output value for that gate to occur, is assigned with a probability of 1. Eq. 2 shows the ITM matrix for AND logic gate.

$$\text{PTM} = \begin{bmatrix} 1-p & 1-p & 1-p & p \\ p & p & p & 1-p \end{bmatrix}$$

(1)

$$\text{ITM} = \begin{bmatrix} 1 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

(2)

Probabilistic Transfer Matrix (PTM) and Ideal Transfer Matrix (ITM) can represent any components from the desired circuit. These components can be divided into three special classes of gates namely standalone wires (uncorrelated), fan-out gates and swap of wires (correlated) as shown in [6].

- Standalone wire has no errors and denoted as 2 x 2 Identity Matrix, I.
- Fan-out gate refers to a gate where its output is associated to more than one input of the next gates. This gate is represented as F_n, where it feeds an output signal to n inputs of the next gates. Fig. 1 shows the F_2 involving NAND gates. Its matrix representation is shown in Eq. 3.
- Swap of wires refers to crossing of wires. Fig. 2, Fig. 3 and Fig. 4 show swap of two-wires with one crossing point, swap of three-wires with one crossing point and swap of three-wires with two crossing points respectively. In respective ways the swap of wires are shown in Eq. 4, Eq. 5 and Eq. 6.
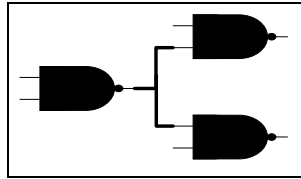

Fig.1. 2-output fan-out NAND gates

$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \qquad (3)$$
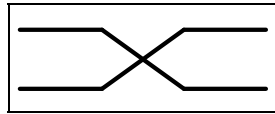

Fig.2. 2-wire swaps [6]

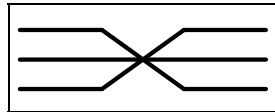$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \qquad (4)$$

Fig.3. 3-wire swaps [6]

$$
\begin{bmatrix}
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\
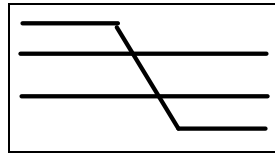0 & 0 & 0 & 0 & 0 & 0 & 0 & 1
\end{bmatrix}
\tag{5}
$$

Fig.4. 3-wire swaps [6]

$$
\begin{bmatrix}
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1
\end{bmatrix}
\tag{6}
$$

There are two different types of connection for components in the desired circuit; either serially or parallelly as shown in Fig. 5. For a serial connection, circuit PTM is obtained as the product of PTM matrices for individual components as shown in Fig. 5(a). For a parallel connection, circuit PTM is obtained as the tensor product of PTM matrices for individual components as shown in Fig. 5(b) [4-7].
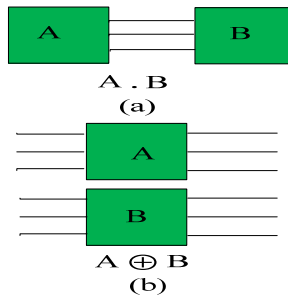
Fig.5. (a) Serial Connection and (b) Parallel Connection

3. System Design

Using the built-in feature of PTM, it can be hypothesized that reliability of the desired circuit system does not only depend on its faulty gates, but also on the error thresholds of those faulty gates above which no reliable computation is possible. For this purpose, PTM is employed to compute the exact error thresholds for individual noisy gates. In this approach, von-Neumann model has been considered. According to the model, the worst scenario in computing circuit reliability is attained when two input signals for a logic gate have same likelihood of being '1' [8].

To determine the exact error threshold for NAND gate, PTM model is applied to a series of NAND gates as shown in Fig. 6. In this series of NAND gates, its order is labelled by index j, j = 1, 2, 3, ….., k, …., where the output signal of gate j converts to an input signal of gate $j + 1$. For any stationary p value, $0 < p \leqslant 0.5$, one randomly chooses an initial value of $X1$ (likelihood of input signal being '1'). The likelihood of output signal being '1' is computed for next stages until a sufficiently large number of stages are analyzed. This process of iteration is continued until the likelihood of output signal being '1' converges to some fixed attractors. The attractors can be in the form of

- a point for that specific p,

- a number of distinct points for that specific p,

- or chaos.

Once fixed attractors are obtained, those fixed attractors are plotted against each value of p as shown in Fig. 7 for NAND gate. By applying the same procedure on a series of other gates, one can obtain similar kind of graph plots as demonstrated in Fig. 8, Fig. 9 and Fig.10 for NOR, XOR and NOT gates respectively.
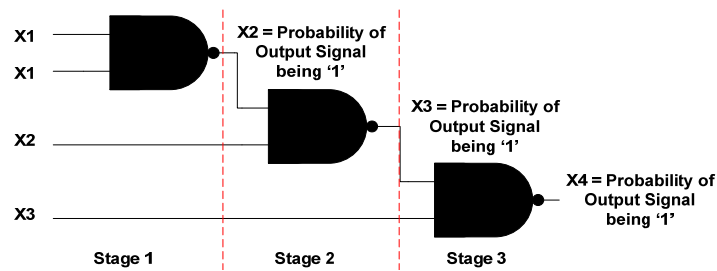
Fig.6. Series of NAND gates
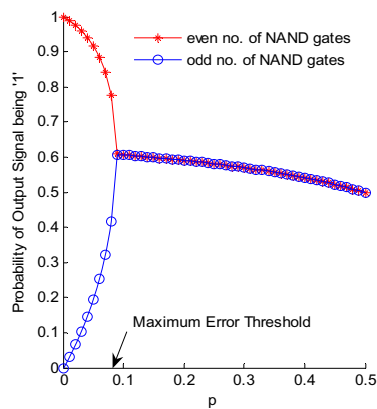
4. Simulation Results and Discussion

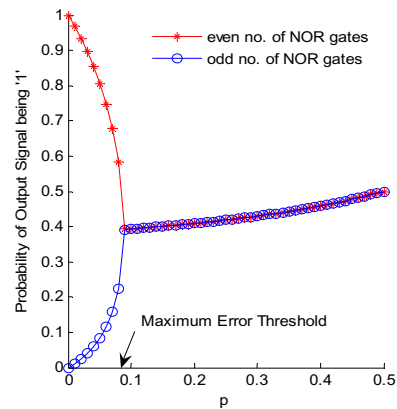Fig.7. Graph Plot for NAND gate

Fig.8. Graph Plot for NOR gate

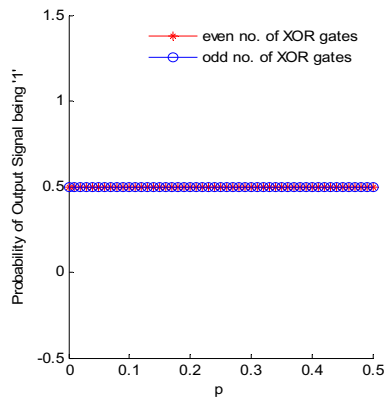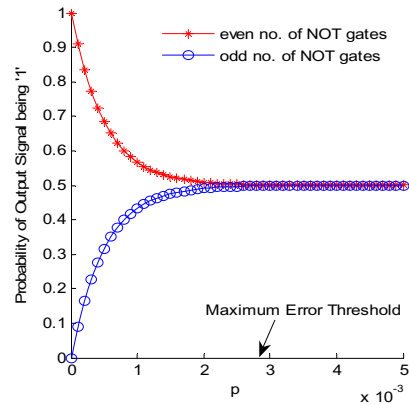

Fig.9. Graph Plot for XOR gate

Fig.10. Graph Plot for NOT gate

From the graph plots, when error in the faulty gate, p < maximum error threshold, then the gates can function reliably based on its even and odd numbers of logic gates. When error in the faulty gate p > maximum error threshold, then the output signal can be explained as neither being '1' nor '0'. From Fig. 7 and Fig. 8, both NAND and NOR faulty gates share the same error threshold which is < 0.1. This phenomenon happened because the NOR gate is a duality of the NAND gate, so their behaviors, illustrated by Fig. 7 and Fig. 8, come out to be complementary to one another. For XOR gate in Fig. 9, its maximum error threshold is 0, or in other words a maximum error threshold never occurs for this gate. For NOR gate in Fig. 10, its maximum error threshold is < 3×10^{-3}. Based on PTM approach, among all the faulty gates, NAND and NOR gates give the highest error threshold, followed by NOT gate and then by XOR gate. This indicates that from all the existing faulty gates, NAND and NOR gates would be preferably used the most in designing a circuit system due to their highest error threshold compare to other faulty gates.

5. Conclusion

Reliability is fast becoming a critical subject in the design entry of nanotechnology-based circuits. Due to this occurrence, various computational-based approaches have been proposed to assess reliability of these circuit systems. Apart from assessing reliability, in this paper we briefly present an analytical approach based on Probabilistic Transfer Matrix (PTM) on how to derive exact error thresholds for general probabilistic computation. Exact error thresholds for faulty gates are significantly important subject to be considered in the designing nano-based circuit systems as it provides the exact bounds above which no reliable calculation is achievable.

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