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Impacts of the Drain-side nWell Adding on ESD Robustness in 0.25-μm LV/HV nMOSTs

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Abstract

An n-channel MOS transistor (nMOST) no matter what low or high voltage processes are often used in I/O pads as ESD protection components. However, the contact spiking is a common caused leakage problems which deeply affect the ESD reliability capability of protection devices. Therefore, in this work, we proposed systematic experiments on the drain side: by adding an n-type Well (nWell) structure in the drain area for 0.25-μm low voltage (LV)/ high voltage (HV) processes. After measurement and analysis, it is found that for this LV process adding the nWell in drain side is bad for the I_{t2} robustness of ESD capability, such as the lowest ESD capability condition (S= 9-μm) as compared with the reference group (none with the nWell) is decreased up to 42%, so in the ESD protection application should be avoided to add this structure; in the same token adding the nWell structure in the drain side of an HV nLDMOS, it was found that can expand an ESD current conduction cross-sectional area, which will not dissipate a lot of heat on the surface of the device led to burn, and then enhancing the ESD capability. Meanwhile, the ESD capability of a DUT with S= 9-μm as compared with the reference group (none with the nWell) is increased up to 8%, so adding an nWell structure in the drain side is good for ESD capability (I_{t2} value) of HV MOS devices.

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Keywords: Contact spiking; electrostatic discharge (ESD); field oxide device (FOD); holding voltage (V_h); lateral-diffused MOS (LDMOS); trigger voltage (V_{t1}); secondary breakdown current (I_{t2})

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1. Introduction

In recent years, with advances and scaling in microelectronic technologies, a large number of silicon technology has been widely used in the daily use of personal computers, laptops, mobile phones, internet, digital cameras, and others applications. Moreover, electrostatic discharge (ESD) events affect the reliability of ICs appeared to be increasingly serious, the reason lies in the integrated circuits are scaled, resulting in a thinner gate oxide layer, the source/drain regions were shallow junction depths and contacts window size got smaller. Therefore, the weighting of integrated circuits suffered by ESD damages is rapidly increased. Therefore, ESD reliability has become increasingly important for ultra deep submicron or nano-scale processes electronic products [1-4].

In the microelectronics failure analysis, especially a contact spiking happened to drain region caused leakage or short circuit, and which does deeply affect the reliability of ESD capability [5-8]. In the design rules of T-Fab 0.6-μm process [9], which records the designer should add an nWell structure below the drain side to enhance the ESD capability of components, but how is it in a 0.25-μm process? This paper will also aim at and evaluate this process as for the low- and high-voltage devices to explore.

2. Contact spiking and layouts of DUTs

2.1 Contact spiking phenomenon

The damage of ESD for integrated circuits was mostly caused by ESD large current with residual heat. The rising time was set to be in the nano second scale, and the voltage can be up to kV during the transient ESD noise of human body model (HBM). The transient power on a small area of drain depleted high-resistance region of an MOSFET is high. The generated heat usually results in aluminum or via-plug material of a contact window spiking, and the fusing part would form alloy with silicon substrate. Then, the p/n junction of semiconductor device disappears, and the electrical junction performance will seem to be short and abnormal. The spiking phenomenon is prone to take place in p/n junction of drain or source side, especially occurs in the drain reverse bias situation. This is due to the resistance of this area be highest and to form high temperature and cause spiking phenomena.

2.2 nWell adding of an LV 5V nMOST in the drain side

All of these test DUTs were fabricated by a T-Fab 0.25-μm low-voltage 5-V process. The multi-finger structure of nMOSTs used in this work, the channel length (L) is kept to be 0.8-μm, channel width of each finger (W_f) is 50-μm, finger numbers M= 4, and the total channel width (W_{tot}) is kept a constancy, 200-μm. As shown in Figs 1(a)~ 1(b), this structure exists an n-type well process below drain contact window to cover whole drain contact-hole region. These DUTs works out to modulate n-well width (S) in the drain side. Starting from the minimum design rule, it gradually increases the value of S until fitted in the design rule for the n-well to drain diffusion region. Therefore, the nWell width (S) changes from 0-μm (Ref. DUT), 3-μm, 5-μm, 7-μm, 9-μm and to 11-μm, respectively. That's the method we used to modulate nWell to observe and testify the proposed structural impacting on nMOST devices.

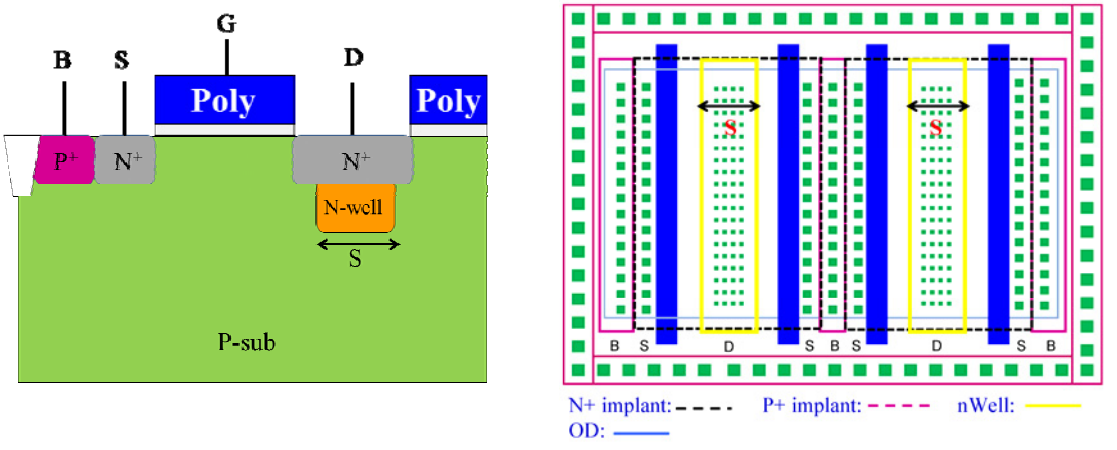


Fig. 1. (a) Cross-sectional view; and (b) layout schematic diagram of an LV nMOST with adding an nWell structure in the drain-side.

2.3 nWell adding of an HV nMOST in the drain side

Here, the entire test DUTs for this experiment was fabricated by a T-Fab 0.25-μm 60-V high voltage process. The channel length is kept to be 2-μm, channel width of a unit finger (W_f) is set to be 100-μm, finger numbers M= 6, and the total channel width (W_{tot}) is kept a constancy, 600-μm. As shown in Figs 2(a)~ 2(b), the 60-V lateral-diffused MOS (LDMOS) with adding an nWell structure beneath the drain-side contacts, so that it can cover the drain contact area. Changing the width (S) of an nWell, the S parameter started from a value of the minimum design rule to the contact hole, and slowly increased the value of S until conform to a minimum design rule of nWell to the drain-side diffusion region will be investigated in this paper. So, the widths (S) of this nWell are 0-μm (Ref. DUT), 3-μm, 4-μm, 5-μm, 6-μm, 7-μm, 8-μm and 9-μm, respectively. Therefore, the width of an nWell grew up slowly to check and verify the influence of this structure on nLDMOS devices.

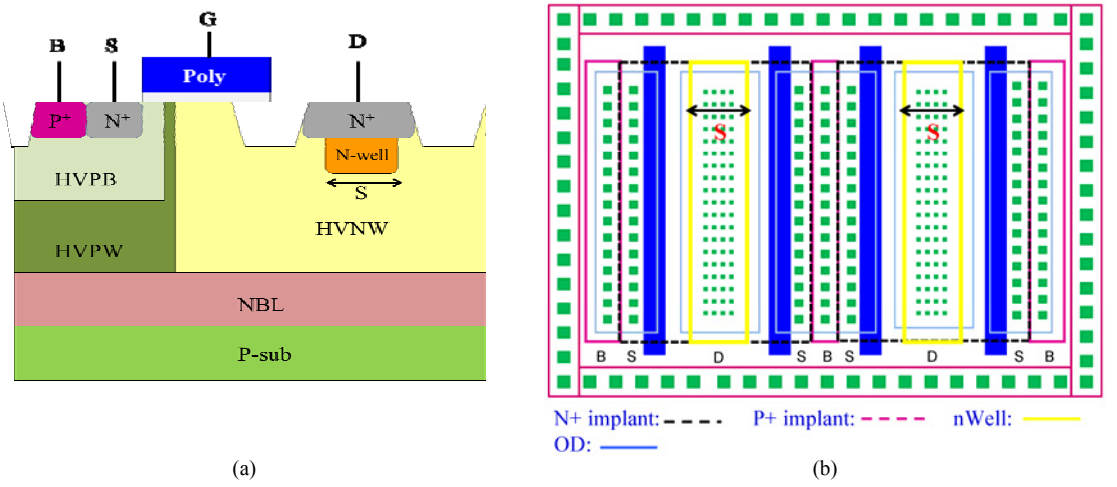


Fig. 2. (a) Cross-sectional view; and (b) layout schematic diagram of an HV nLDMOS with adding an nWell structure in the drain-side.

3. Testing Equipment System

A transmission-line-pulse (TLP) system for experimental testing is controlled by the LabVIEW software. It managed the subsystem electrical machine such as the ESD pulse generator, the high-frequency digital oscilloscope and the digital power electric meter instruments to achieve the automatic measurement. This machine can provide a continuous step-high square wave to device, and short raise time of the continuous square wave can also simulate transient noise of ESD. This HBM-like system has used the short square wave with 100-ns pulse widths and 10-ns rising/falling times to evaluate the voltage and current response of device.

4. Measurement Results and Discussion

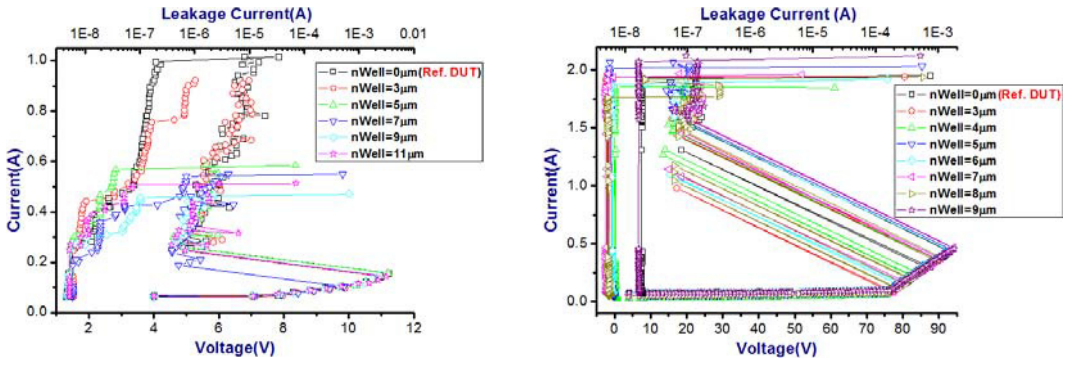
4.1 nWell adding of an LV 5V nMOST in the drain side

Fig. 1 samples had been tested, the TLP data can be obtained and shown in Fig. 3(a) and Table 1. With the increasing of the nWell width (S), the I_{t2} value is slowly decreased, and an nMOS device with S=0 (Ref. DUT) has a maximum I_{t2} value. Nevertheless, from Fig. 4, the influence of an nWell structure on V_h of DUTs is not evident. The V_h value slightly increased only when the width of nWell equals 3~7-μm. Unfortunately, the I_{t2} values from experiment data, the lowest ESD capability condition (S= 9-μm) as compared with the Ref. DUT (none with the nWell) is decreased up to 42% in this LV 5-V 0.25-μm process. Therefore, it should be avoided using an nWell structure in the drain side for an LV process, in which it can't effectively increase the ESD capability by adding an nWell structure in the drain-side. Thus, it is not same as the T-Fab 0.6-μm process described.

4.2 nWell adding of an HV nMOST in the drain side

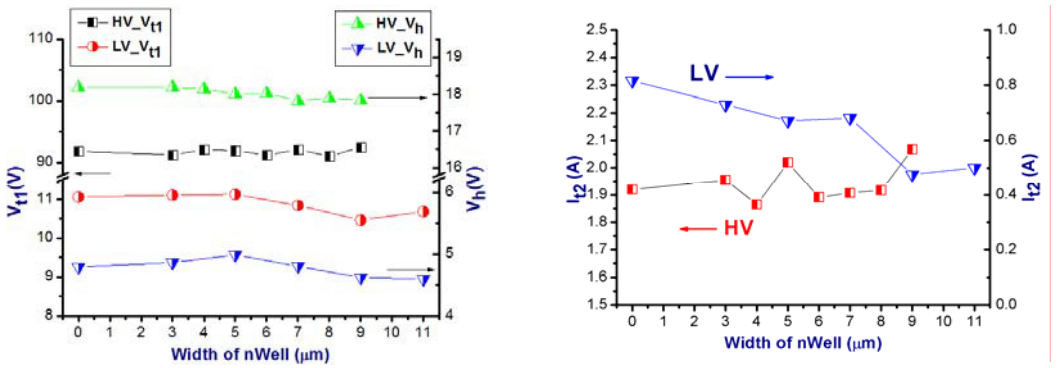
Similarly, Fig. 2 samples had been zapped; the TLP data can be obtained and shown in Fig. 3(b) and Table 1. Excitedly, with the increasing of the nWell width, the I_{t2} value is slowly increased, while an nMOS device whose nWell width is 5-μm or 9-μm has a maximum I_{t2} value. And, the I_{t2} value of an nLDMOS DUT whose width of nWell was set to be 9-μm has 8% higher than that of a Ref. DUT in 0.25-μm HV 60-V process. From Fig. 4, the V_h and V_{t1} values show a nearly constant relationship with nWell width in the HV-nLDMOS device. Meanwhile, the V_h value of nLDMOS DUT whose width of nWell was set to be 9-μm has 2% lower than that of a Ref. DUT.

In Fig. 4, the n-well width increases gradually from a minimum design rule. It can conclude that the ESD ability (I_{t2} values) is improved in nLDMOS DUTs with an additional n-well structure in the drain side. As the S equals to the maximum value of 9-μm, this nLDMOS DUT possess a largest I_{t2} value, improved about 8% as compared with $(I_{t2})_{Reference}$. So, for the HV nLDMOS devices, adding an nWell structure in the drain side is good for ESD capability (I_{t2} value).



(a) (b)

Fig. 3. Characteristic comparisons of (a) LV; and (b) HVnMOS DUTs as the nWell width varied.



(a) (b)

Fig. 4. (a) V_{t1}, V_h ; and (b) I_{t2} vs. nWell width relationship diagrams of LV & HV DUTs in the drain-side.

Table 1. The physical parameters comparisons of LV & HV DUTs as the nWell width (S) varied.

5V nMOST (W_f= 50μm)	V_{t1}(V)	V_h(V)	I_{t2}(A) (mean ± σ)
S= 0μm (Ref. DUT)	11.063	4.793	0.815 ± 0.252
S= 3μm	11.108	4.863	0.730 ± 0.342
S= 5μm	11.127	4.987	0.672 ± 0.272
S= 7μm	10.844	4.806	0.682 ± 0.222
S= 9μm	10.466	4.698	0.476 ± 0.084
S= 11μm	10.686	4.572	0.500 ± 0.115
60V nLDMOS (W_f= 100μm)	**V_{t1}(V)**	**V_h(V)**	**I_{t2}(A) (mean ± σ)**
S= 0μm (Ref. DUT)	91.871	18.183	1.920 ± 0.195
S= 3μm	91.271	18.190	1.955 ± 0.215
S= 4μm	92.131	18.148	1.864 ± 0.175
S= 5μm	91.976	18.007	2.020 ± 0.112
S= 6μm	91.247	18.026	1.891 ± 0.235

S= 7μm	92.146	17.814	1.907 ± 0.164
S= 8μm	91.060	17.885	1.917 ± 0.173
S= 9μm	92.527	17.830	2.068 ± 0.235

5. Conclusion

After the actual samples testing, it can be found that the drain-side with adding an nWell structure can not efficiently promote the ESD robustness in a 0.25-μm 5-V low voltage process. It will make I_{t2} values have a declined trend, accordingly, the ESD capability of a DUT with S= 11-μm as compared with the reference group (none with the nWell) is decreased up to 39%. Then, it should avoid using this structure on applications; On the contrary, furthermore, the drain-side with adding an nWell structure have positive influence on the ESD robustness in a 0.25-μm 60-V high voltage process, for instance, while the nWell width is equal to 9-μm, it has a higher I_{t2} and V_h values. The ESD capability of a DUT with S= 9-μm as compared with the reference group (none with the nWell) is increased up to 8%, therefore, adding an nWell structure in the drain side is a right strategy for ESD robustness in HV MOS devices.

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References

[1] Xin Wang, Siqiang Fan, Hui Zhao, Lin Lin, Qiang Fang, He Tang, Albert Wang. Whole-Chip ESD protection design for RF and AMS ICs. Tsinghua Science and Technology 2010; 15(3): 265-274.
[2] Chia-Tsen Dai, Ming-Dou Ker. Investigation on safe operating area and ESD robustness in a 60V BCD process with different deep P-Well test structures. IEEE International Conference on Microelectronic Test Structures 2013: 127-130.
[3] D. Linten, G. Hellings, Shih-Hung Chen, G. Groeseneken. ESD in FinFET technologies: Past learning and emerging challenges. IEEE International Reliability Physics Symposium 2013: 2B.5.1-2B.5.8.
[4] Shen-Li Chen, Min-Hua Lee, Tzung-Shian Wu, Yi-Sheng Lai, Chun-Ju Lin, Hsun-Hsiang Chen. Source-side Layout on LU/ESD Reliability in the HV 0.25μm 60V nLDMOS. Lecture Notes in Electrical Engineering 2013: 503-511.
[5] Peng‐Heng Chang, R. Hawkins, T.D. Bonifield, L.A. Melton. Aluminum spiking at contact windows in Al/Ti‐W/Si. Applied Physics Letters 1988; 52(4): 272-274.
[6] W.L.T.M. Ramselaar, F.T. Agricola, C.A. Seams. The Influence of Tungsten Contact Filling on Junction Quality and Contact Resistance. 19th European Solid State Device Research Conference 1989: 653-656.
[7] M. Beh, C. Kang, M. Natarajan, M.K. Radhakrishnan. Analysis of HBM and MM ESD failures in nMOS devices. 5th International Symposium on the Physical and Failure Analysis of Integrated Circuits 1995: 111-115.
[8] M. Etherton, V. Axelrod, T. Meuse, J.W. Miller, H. Marom. HBM ESD failures caused by a parasitic pre-discharge current spike. 30th Electrical Overstress/Electrostatic Discharge Symposium 2008: 30-39.
[9] T-Fab. 0.6-μm 1P3M polycide 5-V design rule 1998: 39–41.