Available online at [www.sciencedirect.com](http://www.sciencedirect.com/)

**ScienceDirect**

AASRI Procedia 5 (2013) 249 – 261

## 2013 AASRI Conference on Parallel and Distributed Computing and Systems

Modeling and Simulation of Different System Topologies for DSTATCOM

Pradeep Kumar\*, Niranjan Kumar, A.K.Akella

*Electrical Engineering Department, National Institute of Technology Jamshedpur, 831014, Jharkhand, India*

**Abstract**

Power Quality enhancement in a distribution network is achieved by shunt compensation device known as Distribution static compensator (DSTATCOM).In this paper, three different system topologies for Distribution Static Compensators (DSTATCOMs) are modeled and tested using Simulink’SimPowerSystem Toolbox for power system quality studies. Simulation tests on a distribution system, equipped with the unbalanced and non-linear load. With the different system topologies of Distribution Static Compensators (DSTATCOMs) it is observed that power factor can be improved in supply system. The DSTATCOM controls are based on Synchronous Reference Frame control. The modeled DSTATCOM topologies can be used to develop and test different, control strategies and methods for the DSTATCOM. These models can also aid instructors in teaching power quality courses.

© 2013 The Authors. Published by Elsevier B.V. Open access under [CC BY-NC-ND license.](http://creativecommons.org/licenses/by-nc-nd/3.0/)

© 2013 Published by Elsevier B.V.

Selection and/or peer review under responsibility of American Applied Science Research Institute

Selection and/or peer review under responsibility of American Applied Science Research Institute

*Keywords:* Distribution Static Compensator (DSTATCOM); Simulink’SimPowerSystemToolbox; Control; Modeling; Simulation; power quality; Synchronous Reference Frame (SRF)

##### Introduction

Distribution static compensator (DSTATCOM) is one of the power custom device that is used for Power Factor Improvement on source side [1]. The DSTATCOM has a Six-leg Voltage-Sourced Converter (VSC) with Insulated Gate Bipolar Transistor (IGBT) as a switching element. Different studies have been performed

\* Pradeep Kumar . Tel.:+91-9905205302; fax:+91-657-2382246.

*E-mail address:* [kumarcs08@gmail.com.](mailto:kumarcs08@gmail.com)

2212-6716 © 2013 The Authors. Published by Elsevier B.V. Open access under [CC BY-NC-ND license.](http://creativecommons.org/licenses/by-nc-nd/3.0/) Selection and/or peer review under responsibility of American Applied Science Research Institute doi:10.1016/j.aasri.2013.10.086

to evaluate the performance or propose control strategies for DSTATCOM to improve its performance [2-10]. Time domain simulations and /or practical experiments have been used to perform these studies.Time domain simulations have been shown to provide accurate prediction of the behaviour of Voltage-Sourced Converter (VSC) based FACTS devices [11]. There are many packages available to model and simulate VSC based FACTS devices such as EMTP, PSCAD, MATLAB/SIMULINK, PSIM. MATLAB/SIMULINK is the most widely used package in engineering sciences since it has many toolboxes that cover all engineering applications [12]. This paper models and simulates three different system topologies for Distribution static compensator (DSTATCOM) using Simulink’SimPowerSystem Toolbox. The DSTATCOM topologies are based on Synchronous Reference Frame (SRF) control [13].

##### System Topologies for DSTATCOM

There are different system topologies for the DSTATCOM. Out of which, three are selected and used in this paper. The selected systems are:

* 1. DSTATCOM with supply side-connected rectifier shown in Fig.1. (System 1)
  2. DSTATCOM with load-side-connected rectifier shown in Fig.2. (System 2)
  3. DSTATCOM with constant dc voltage shown in Fig.3. (System 3)

The load which has been selected for these topologies are three phase unbalanced R-L load and diode rectifier as a nonlinear load. A step-up transformer for stepping up the voltage has been used in between the STATCOM and distribution system.



*vS*

*R*

*s*

*L*

*s*

*vt*

*iL*

Unbalanced &Non-linear Load

*iS*

*iC*

Three-phase Uncontrolled rectifier

*Cdc*

*Lf*

*V*dc *i*La *i*Lb *i*Lc *Vt*

SRF controller

a

A

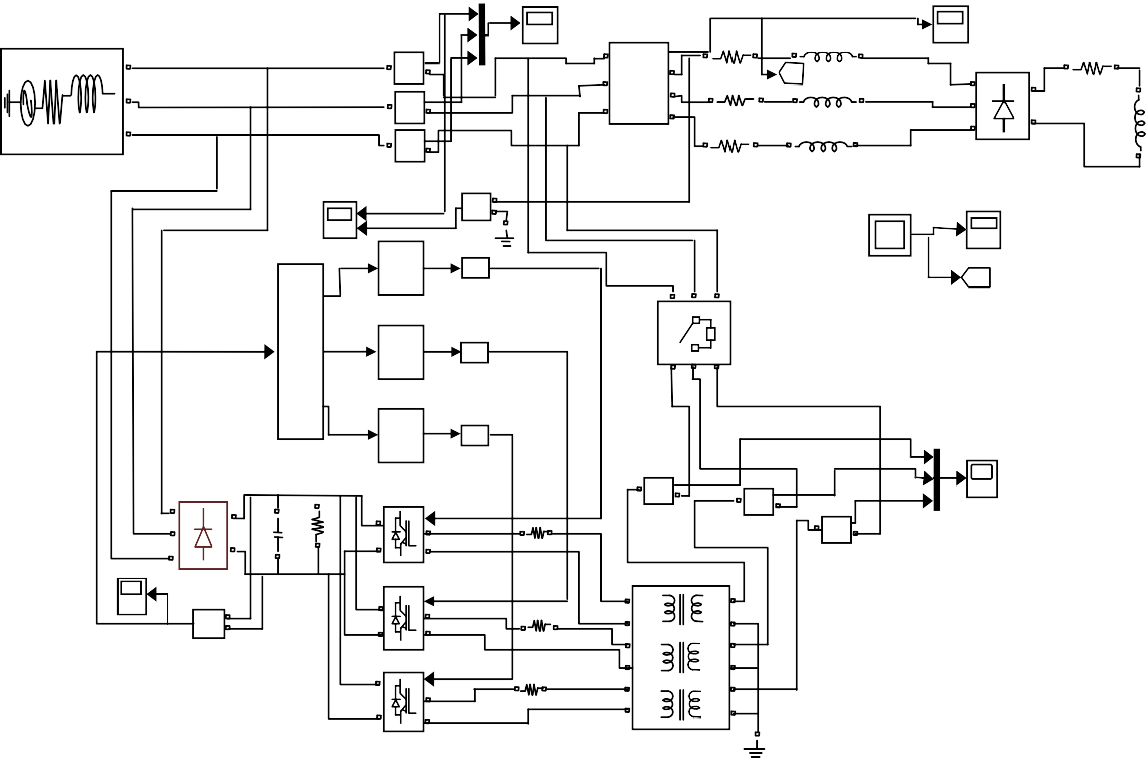
b

B

c

C

Fig. 1. DSTATCOM with supply side-connected rectifier including Simulink Model



IS

Vt1

|

A

Vabc

A

+

a

b

Ra

B

C

-

Current

|

+

Current1

|

+

-

Current2

B

[A]

Goto

La

A

Rd

+

C

c

B

-

Rb

Lb

-

Three-Phase

V-I Measurement

C

Universal Bridge

Ld

Three-Phase Source

Rc

Lc

Isa&Vta

Volt1

+

V

-

3

1/Z Unit Delay1

|La, |Lb, |Lc

|L

Discrete PWM Generator

[B]

Goto1

Three-Phase Breaker

1/Z Unit Delay2

Discrete PWM Generator1

ICa

SRF controller

1/Z Unit Delay3

Discrete PWM Generator2

ICb

|

+ | ICc

A

+

-

Current3

+

+

g

Lf2

-

Current4

IC

|

B

Odc

Rdc

A

+

-

=

B

-

Current5

DC LINK Universal Bridge1

Volt

+

V -

C

IGBT Bridge 2 arm

+

=

g A

B

Lf1

A1+

A1 B1+

A2+

A2 B2+

IGBT Bridge 2 arm1

+ g

Lf

A

=

B

B1

C1+ C1

B2

C2+ C2

IGBT Bridge 2 arm2

Three-phase Linear Transformer

Out3

In1 Out2

Out1

DC LINK

3

|L

|La, |Lb, |Lc

[B]

Goto1

A Rd

+

B

- Ld

C

Universal Bridge

a

A

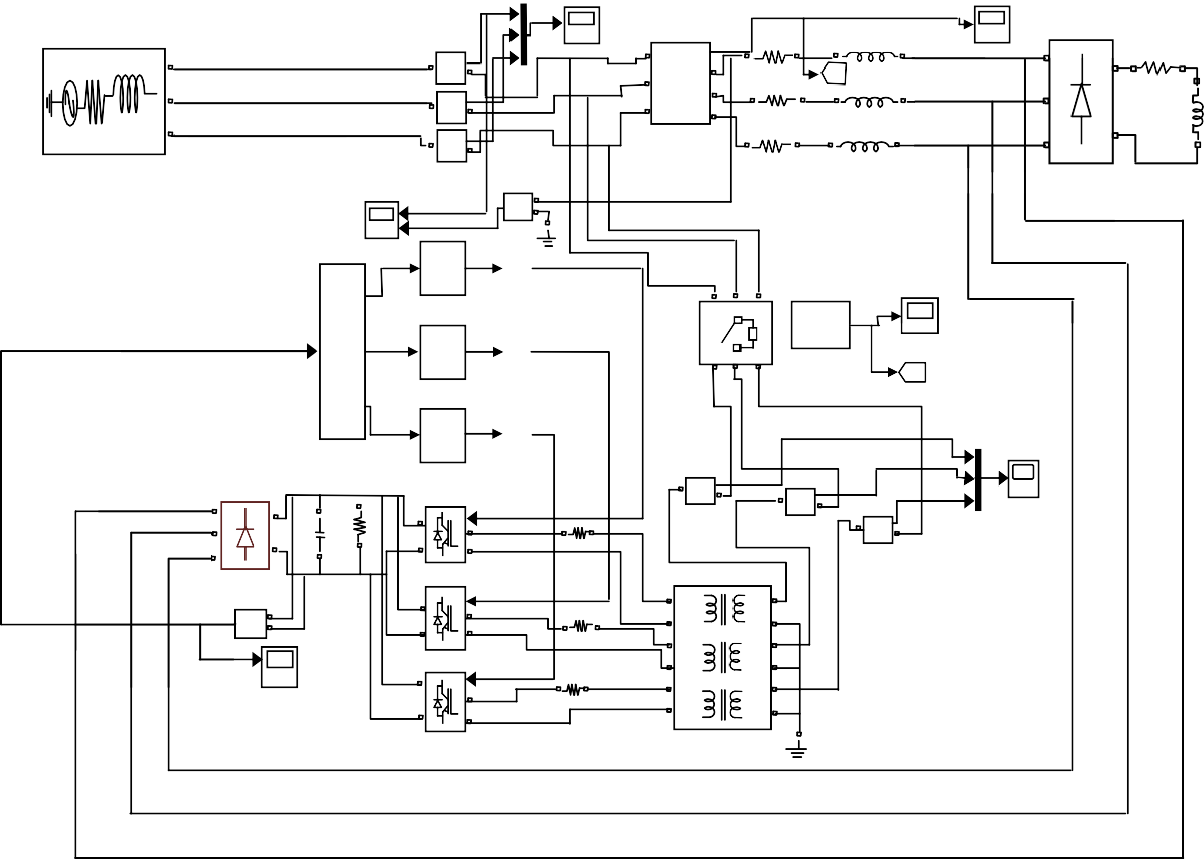
b

B

c

C

Fig. 2. DSTATCOM with Load side-connected rectifier including Simulink Model



IS

|

A

Vabc

Vt1

A

A

+

C

-

Current

|

+

Current1

|

+

-

Current2

a

Ra

B

b

[A]

Goto

La

+

Rd

B

C

c

B

Ld

-

Rb

Lb

Three-Phase

V-I Measurement

-

Three-Phase Source

Rc

Lc

C

Universal Bridge

Isa&Vta

Volt1

+

V

-

Out1

Unit Delay1

Discrete PWM Generator

Three-Phase Breaker

In1 Out2

IL

Ila, Ilb, Ilc

Unit Delay2

Out3

Discrete PWM Generator1

[B]

Goto1

ICa

SRF controller

Unit Delay3

Discrete PWM Generator2

ICb

|

+ |

A

+

-

Current3

ICc

+

-

Current4

IC

B

Odc

Rdc

+

g

Lf2

|

A

+

-

=

B

-

Current5

C

Universal Bridge1

IGBT Bridge 2 arm

Volt

+

V -

+ g

A

Lf1

= B

A1+

A1 B1+

A2+

A2 B2+

IGBT Bridge 2 arm1

+ g

Lf

DC LINK

A

=

B

B1

C1+ C1

B2

C2+ C2

IGBT Bridge 2 arm2

Three-phase Linear Transformer

1/Z

1/Z

3

1/Z



*vS*

*R*

*s*

*L*

*s*

*vt*

*iL*

Unbalanced &Non-linear Load

*iS*

*iC*

*Vdc*

**+**

**|**

*Lf*

*V*dc *i*La *i*Lb *i*Lc *Vt*

SRF controller

##### Control Scheme

Odc

e1

LINK

Fig. 3. DSTATCOM with constant DC voltage including Simulink Model

DSTATCOM Topologies are controlled using Synchronous Reference Frame (SRF) theory.

The three phase load current in *a*–*b*–*c* frame are converted to the two phase load current in *d*–*q* frame using the following formulation

*iLd*

*iLq*



cos *t*

## sin *t*



2

3

cos *t*

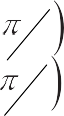
## sin *t*

 2

 2

cos *t *

sin *t *



3

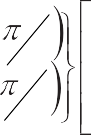
3

2

## 2

*iLa*

*iLb*



3

3

*i*

DC LINK

3

|L

|La, |Lb, |Lc

[B]

Goto1

A Rd

+

B

- Ld

C

Universal Bridge

A B C

Three-Phase Source

Vt1

A

+

B

-

C

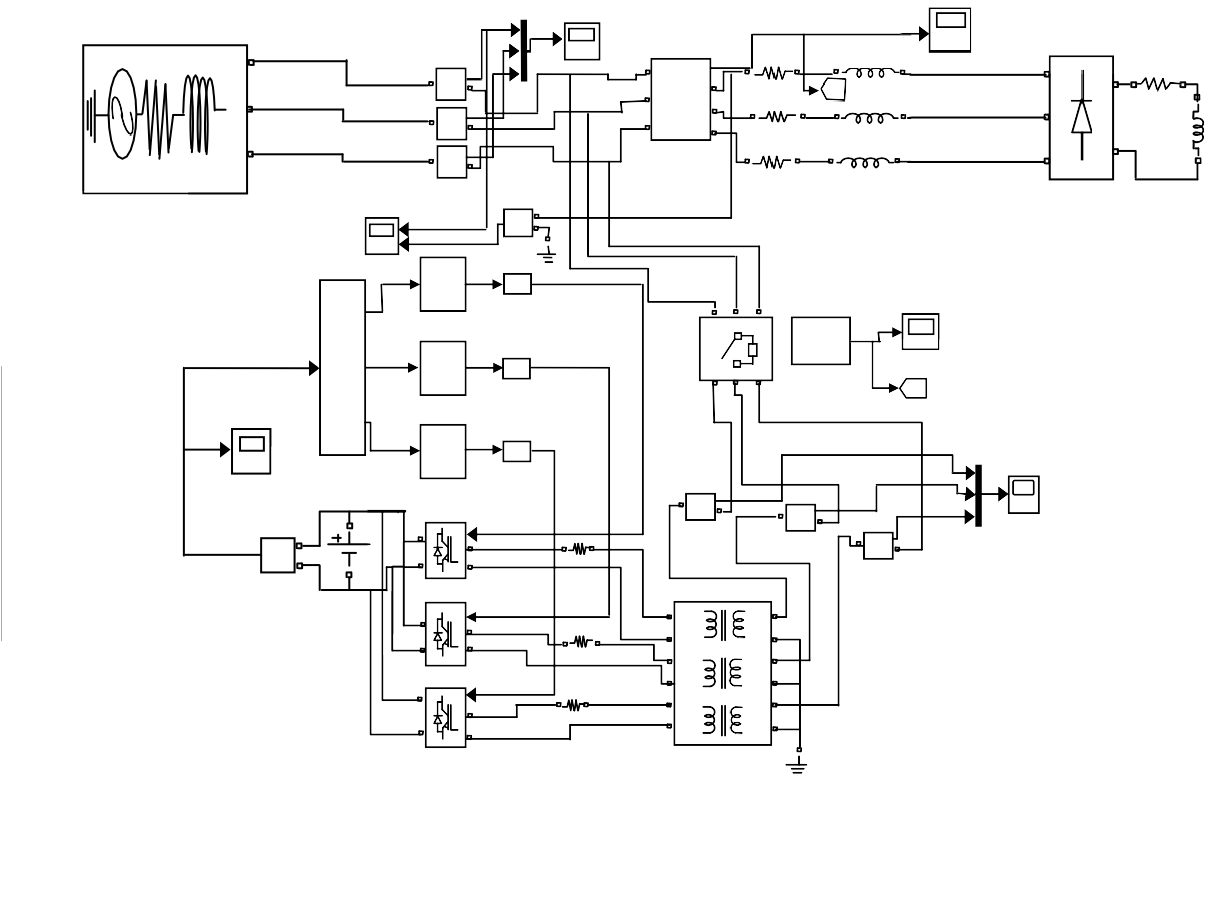
Universal Bridg

Volt

+

V -

DC



A

IS

Vt1

|

A

Vabc

+

-

Current

|

+

Current1

|

+

-

Current2

a

Ra

B

[A]

Goto

La

Rd

B

b

C

c

-

Rb

Ld

Lb

C

Three-Phase

V-I Measurement

Rc

Lc

Universal Bridge

Three-Phase Source

Isa&Vta

Volt1

+

V

-

1/Z Unit Delay1

Discrete PWM Generator

Three-Phase Breaker

IL

1/Z Unit Delay2

Ila, Ilb, Ilc

Discrete PWM Generator1

[B]

Goto1

ICa

SRF controller

1/Z Unit Delay3

DC LINK

Discrete PWM Generator2

ICb

|

+

|

ICc

Volt

+

v

-

-

Current3

+

IC

+

g

DC

Lf2

-

Current4

|

A

+

=

B

-

Current5

IGBT Bridge 2 arm

+

g

A

Lf1

=

B

A1+

A1 B1+

A2+

A2 B2+

IGBT Bridge 2 arm1

+

g

Lf

A

=

B

B1

C1+ C1

B2

C2+ C2

IGBT Bridge 2 arm2

Three-phase Linear Transformer

Out3

In1 Out2

Out1

C

-

B

+

A

3

a

A

b

B

c

C

G (s )i Ld



i Ld

i Lq



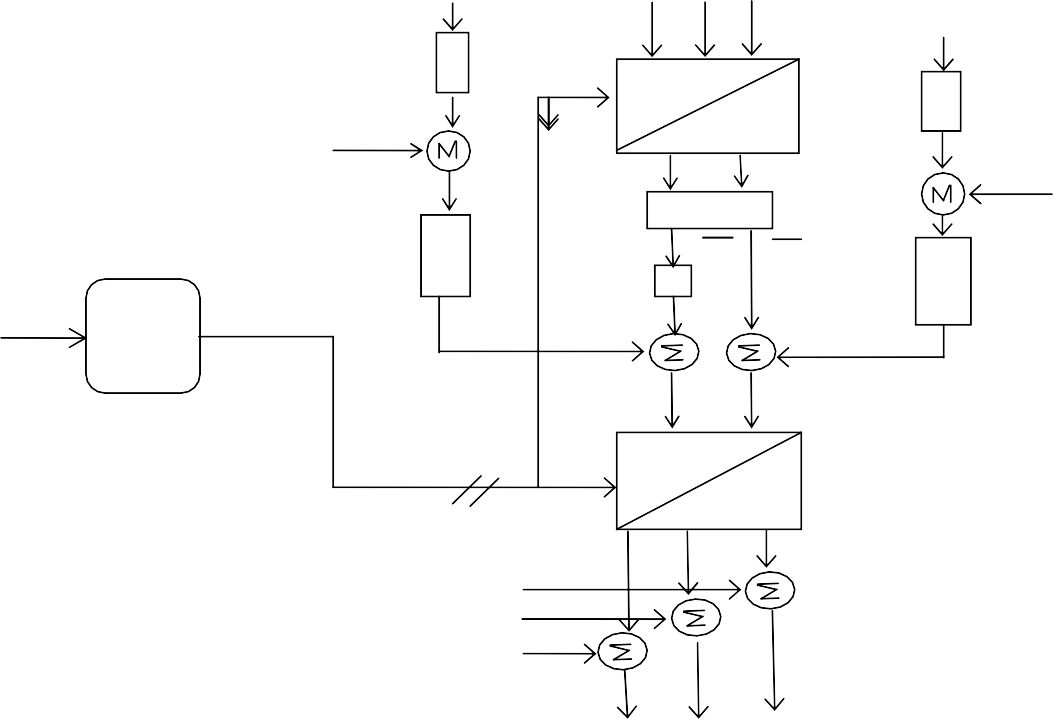
G ( s ) i Lq



*Lc* (1)

(2)

Vt iLa iLb iLc



Vdc

a-b-c

-

d-q

Vt\*

+

iLq

LPF

iLd

-

+

iLq iLd

Kq

PLL

+

+

uiCq

+

i\*

i*Cd*

*Sq*

i\*

+

Sd

sinwt & coswt

d-q

a-b-c

i\* i\* i\*

iLa iLb

iLc

*Sc*

-

+

*Sb* -

+

*Sa*

-

+

LPF

Vdc\*

iLd

iLq

LPF

PI

Controller

Vt

P

Controller

\* \* \*

i

i

i

*Cc Cb Ca*

Fig. 4. Block diagram for Synchronous Reference Frame (SRF) Control Scheme

Q

\*

Gain Kq is defined as the ratio of S to QL and its value will be Zero for Power Factor Improvement.

The d-q component of reference source currents are obtained as

### i\* i i

Sd Ld Cd

i\*  K i  ui

Sq q Lq Cq

(3)

The d-q component of reference source currents are converted to the three phase a*-b-c* frame using the following formulation

2

3

*i* \* *sa*

*i* \* *sb*

### cos

cos

#### *t*



*t*

### 2

### sin

sin

#### *t*



*t*

### 2

*i*\**sd*

\*



3

3

*i* \* *sc*

cos

*t * 2

sin

*t * 2

*i sq*

(4)

The desired compensator currents can be obtained as



3

3

# i\* i i\*

Ca La Sa

i\* i i\*

Cb Lb Sb

# i\* i i\*

##### Simulation Results

Cc Lc Sc

The three DSTATCOM topologies have been simulated for the power factor improvement mode. The total simulation period is 1.0 s. Based on the simulation results,the following analysis can be prepared:

1. The simulation results of sysem1 are depicted in Fig. 6. Load current is unbalanced and non-sinusoidal. Compensator current is sinusoidal in nature. The phase angle between source current and Terminal voltage are Zero degree. This ensure Power factor will be unity i.e. Power factor can be improved after the DSTATCOM is switched on. The dc link voltage Vdc as shown in Fig continues to increase until the DSTATCOM is switched on and finally reach the steady state value of 500V. It starts settling after 0.2 s. The dc voltage Vdc starts to build up on the dc capacitor Cdc.
2. The simulation results of sysem2 are depicted in Fig.7. The waveform of Load current, Compensator current, Source current and Terminal Voltage are same as in Fig.6 but the magnitude of load current is comparatively increased. Power factor can be improved after the DSTATCOM is switched on. The DC link voltage Vdc exponentially increasing with time as shown in Fig. The DC link voltage is not maintained constant but tending towards the value of 250 V.
3. The simulation results of sysem3 are depicted in Fig.8. The waveform of Load current, Compensator current, Source current and Terminal Voltage are same as in Fig. 6. Power factor can be improved after the DSTATCOM is switched on. The DC link voltage is maintained constant at 500 V before and after the DSTATCOM is switched on. This allows the DSTATCOM to improve Power Factor with almost no interruption in the load current.

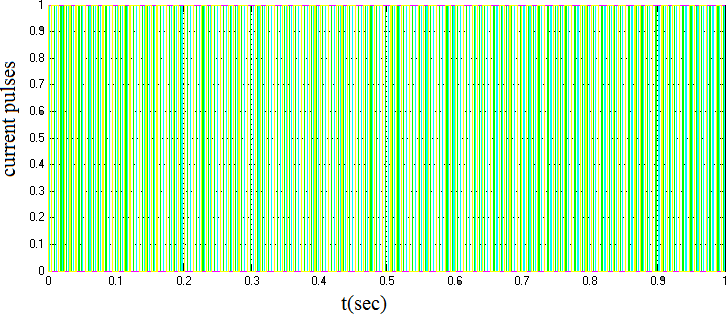
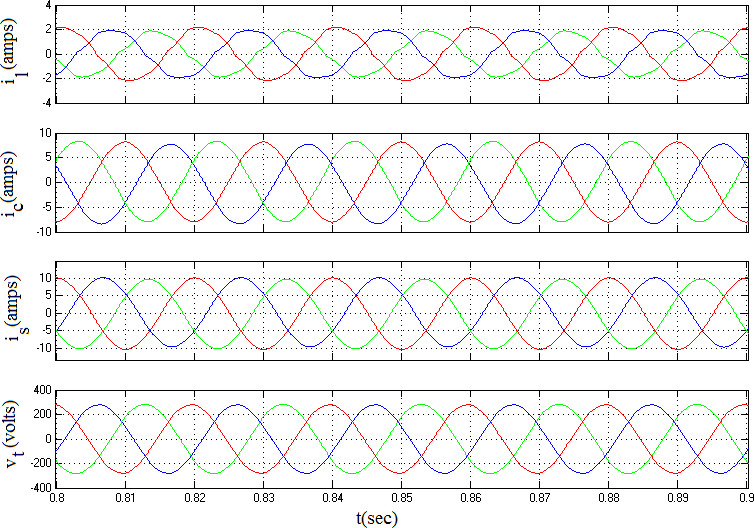


Fig.5. PWM pulses for IGBT



600

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |

500

400

300

Vdc(volts)

200

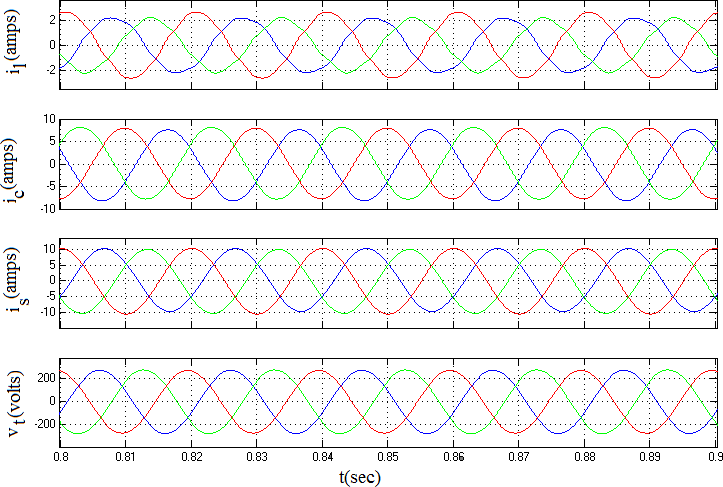
100

0

0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1

t(sec)

Fig. 6. System response with Power Factor Improvement (system1)



250

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |

200

150

Vdc(volts)

100

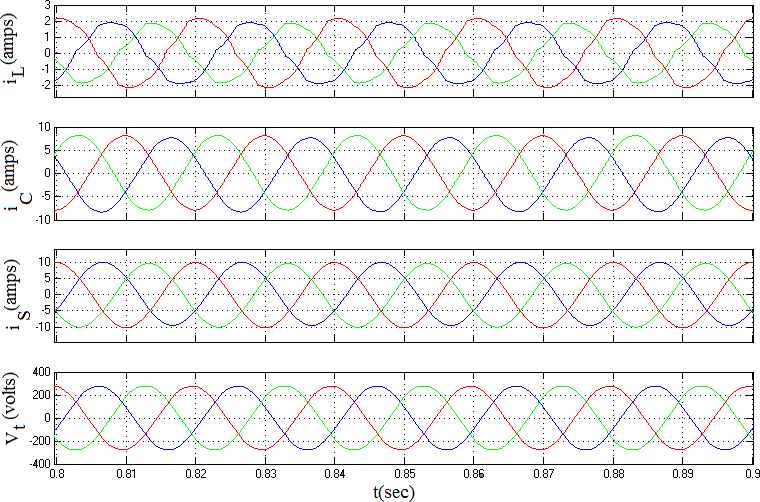
50

0

0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1

t(sec)

Fig. 7. System response with Power Factor Improvement (system2)



501

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |

500.8

500.6

500.4

500.2

Vdc(volts)

500

499.8

499.6

499.4

499.2

4990 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1

t(sec)

Fig. 8. System response with Power Factor Improvement (system3)

##### Conclusion

This paper has developed models for different system topologies of the Distribution Static Compensator (DSTATCOM) using Simulink’SimPowerSystem Toolbox. The control of the DSTATCOM system topologies is based on Synchronous Reference Frame control. Time domain simulations have been used to verify the operation of these models. These models can be easily modified to:

1. Perform different types of power quality studies in a user friendly simulation environment for teaching and researching.
2. Test control strategies and methods for the DSTATCOM.
3. Develop models for other system topologies of the DSTATCOM, which is not considered is this paper, by modifying the existing modeled topologies.

##### Acknowledgments

We would like to thank Director,NIT Jamshedpur for providing financial support to complete the research work under TEQIP scheme for Mr Pradeep Kumar.

##### References

1. Chen B S, Hsu Y Y.A minimal harmonic controller for a STATCOM.IEEE Trans. Ind. Electron. Feb. 2008; 55(2): pp. 655–664.
2. Akagi H, Watanabe E H, Aredes M . Instantaneous Power Theory and Applications to Power Conditioning. Hoboken: NJ Wiley;2007.
3. Herrera R S, Salmeron P, Kim H.Instantaneous reactive power theory applied to active power filter compensation: Different approaches, assessment, and experimental results.IEEE Trans. Ind. Electron. Jan. 2008; 55(1): pp. 184–196.
4. Divan D M, Bhattacharya S, Banerjee B.Synchronous frame harmonic isolator using active series filter. inProc. Eur. Power Electron. Conf. 1991; pp. 3030–3035.
5. Singh B,Verma V.Selective compensation of power-quality problems through active power filter by current decomposition. IEEE Trans. Power Del.Apr. 2008; 23(2): pp. 792–799.
6. Lascu C,Asiminoaei L,Boldea I, Blaabjerg F.Frequency response analysis of current controllers for selective harmonic compensation in active power filters.IEEE Trans. Ind. Electron. Feb. 2009;56(2): pp. 337– 347.
7. Luo A, Shuai Z, Zhu W, Shen Z J.Combined system for harmonic suppression and reactive power compensation.IEEE Trans. Ind Electron. Feb. 2009; 56(2): pp. 418–428.
8. Shyu K K, Yang M J, Chen Y M, Lin Y F. Model reference adaptive control design for a shunt active- power-filter system. IEEE Trans. Ind. Electron. Jan. 2008; 55(1): pp. 97–106.
9. Mohagheghi S, Valle Y,Venayagamoorthy G K, Harley R G. A proportional-integrator type adaptive critic design-based neurocontroller for a static compensator in a multimachine power system. IEEE Trans. Ind. Electron.Feb. 2007; 54(1); pp. 86–96.
10. Shu Z, Guo Y, Lian J. Steady-state and dynamic study of active power filter with efficient FPGA-based control algorithm.IEEE Trans. Ind. Electron. Apr. 2008; 55(4): pp. 1527–1536.
11. Sen K. K, Keri A J F. Comparison of field results and digital simulation results of Voltage-Sourced Converter-based FACTS controllers.IEEE Trans. Power Delivery. January 2003;18(1): pp. 300-306.
12. [https:\\www.mathworks.com](http://www.mathworks.com/)
13. Padiyar K R. FACTS controllers in power transmission and distribution. India: New age international publishers; 2007.

##### APPENDIX

AC line voltage: VLL= 415 V, 50 Hz, Source inductance and resistance: Ls= 42 mH, Rs= 1.57  Unbalanced R-L Load at each phases: Phase a- 45  , 195 mH, Phase b- 70  , 220 mH,

Phase c- 30  , 170 mH

Diode resistance and inductance- 120  , 35 mH

Proportional controller gain: Kp= 0.6 , Proportional gain = -0.2 , Integral gain = -40

DC Voltage : Vdc = 400V, DC capacitance: Cdc = 3500 μF, DC resistance: Rdc = 5500  Filter inductance: Lf = 5.0 mH, PWM switching frequency: 20 kHz