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| 2014 4 AASRI C onference o on Circuit an nd Signal P Processing ( CSP 2014)  Design an nd Imple ementati ion of SO ORIGA--optimiz ed Powe ers-of-  two FI IR Filter r on FPG GA  Abhijit Cha andraa\*, Su udipta Chat ttopadhyay yb, Beetan G Ghoshc  *aDep partment of Elect tronics & Telecom mmunication Eng gineering, Indian Institute of Engin neering Science a and Technology, S Shibpur, India*  *bDe epartment of Elec ctronics & Teleco ommunication Eng gineering, Jadavp pur University, K Kolkata, India*  *cDepartm ment of Electroni cs & Communica ation Engineering g, National Institu ute of Technology y, Durgapur, Indi ia*  **Abst tract**  With h the introductio on of sophistica ated algorithms s, the field of si ignal processing g has experienc ced enormous d diversification | | | | | | | | |
| of la ate. In addition n to this, desig gn of hardwar re efficient dig gital systems h has grown suff ficient interest | | | | | | | | amongst the |
| resea archers in recen nt past. In this a article, an attem mpt has been m made to realize h hardware friend dly powers-of-t two FIR filter | | | | | | | | |
| by u using an evolut tionary comput tation, called S Self-organizing | | | | | | Random Imm migrants Geneti c Algorithm (S SORIGA). In | | |
| conn nection to this, | | | this work ma akes one comp parative study | | amongst vario ous multiplier-l less FIR filters s in terms of | | | |
| hardw ware complexit ty when implem mented on an F FPGA chip. Fin nally, supremac cy of the propo osed design ha | | | | | | | | s firmly been |
| estab blished by comp paring its hardw ware cost with m many of the stat te-of-the-art po wers-of-two FI IR filters.  © 2014 The Authors. Published by Elsevier B. V. This is an open access article under the CC BY-NC-ND license © 20 014 Abhijit Ch handra, Sudip pta Chattopadh hyay and Beet tan Ghosh. Pu ublished by El lsevier B.V.  (http://creativecommons.org/licenses/by-nc-nd/3.0/).  Peer-review under responsibility of Scientific Committee of American Applied Science Research Institute Sele ection and/or p peer review un nder responsib bility of Amer rican Applied Science Rese earch Institute  *Keyw words:* Finite impu ulse response (FI R) filter; Field Pr rogrammable Gat te Array (FPGA) , hardware cost, m multiplier-less fil ter, Self-  organ nizing Random Im mmigrants Geneti ic Algorithm (SO ORIGA). | | | | | | | | |
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**1. Introduction**

Implementation of a general purpose multiplier in an FIR or IIR structure by means of Very Large Scale Integration (VLSI) technique is becoming a very complicated and costlier task to be performed. This problem may be solved by considering multiplication operation as repeated addition and hence substituting the filter coefficients as sequence of shifts and additions. These multiplier-less filters are less power hungry and require less hardware blocks for its implementation [1-2]. In connection to this, SPT representation of filter coefficients is very much popular where the effect of multiplier is substituted by means of adders and delay elements only [3-8].

Several algorithms have been proposed so far in the literature where each of which deals with the powers-of-two design of FIR filter. These include traditional techniques like mixed integer linear programming [9], polynomial time algorithm [10], discrete semi-infinite linear programming [11], branch & bound technique [12] and so on. Recently, the domain of circuit and system design has been noticeably influenced by means of a variety of intelligent optimization techniques of current interest like Genetic Algorithm (GA) [13], Orthogonal Genetic Algorithm (OGA) [14], and Differential Evolution (DE) [15-16] and so on.

In this communication, we have employed Self-organizing Random Immigrants Genetic Algorithm (SORIGA) for the design of multiplier-less low-pass FIR filters. Designed filter has been implemented on real time hardware and the requirement of resulting hardware blocks like digital gates, latches, buffers and so on has been calculated using XILINX Design Suite 12.3 software.

**2. Design Strategy**

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| --- |
| ��with impulse response ���� can simply be written in accordance with the following equations [1-2]:  Filters, in which multiplication operation is carried out by means of shifting and addition, will be  System function ���� and the corresponding transfer function �������of any causal FIR filter of length  ���� � ������� � ���� ���������� ��������� *(1)*  *(2)*  characterized by its impulse response as outlined below [2]:  such a filter due to an excitation ���� is given by For binary representation scheme, ��� may assume a value from the set � � ��� �� and � signifies the  In order to compute the output of this filter at any instant ��� at most � multiplications and �� � ��  ���� � ����� � � ��� ���� ��� ��� ����� ��� � �� ���� � ������ � � � � � � �*(3)* �����*(4)*���� � ����������� ���� ���� ��� � �� *(5)* |

|  |  |
| --- | --- |
| *Abhijit Chandra et al. / AASRI Procedia 9 ( 2014 ) 51 – 56*  concerned since, for every � and �, it keeps the term ���� ��� � �� intact or make it zero depending upon its assignment over the binary space. The term ���, when multiplied with ��� � ��, causes the multiplier to get shifted right by � bits. For an input word length of �, allowable maximum word length of the product ���� ��� � �� thus becomes �� � ��. As a matter of fact, resulting complexity from the architecture of full-adder is proportionately related to��� � �� in accordance with equation (5). *2.2. Design of powers-of-two FIR filter using SORIGA* The parameter ��� does not put any overheads as far as the computational or hardware complexity is  SORIGA [17-18] has been judiciously employed in this work for the synthesis of FIR tap coefficients  ����may be represented by means of a binary row vector as shown below: ���� � ����������������������������� � � � ������������ � ������ � � � � � � � *(6)* which are encoded in the form of sum of signed powers-of-two. In connection to this, any arbitrary coefficient  its central coefficient. Proposed scheme has accumulated all such �� �row vector of length � � �� �evolutionary computation. Being a population-based algorithm, our design strategy generates � such chromosomes randomly of length � which form the pool of potential solution. Based upon the fitness of subsequently in accordance with the steps of SORIGA. This has been symbolically outlined as follows: � �� � which has been regarded as a single chromosome � in the process of � � different binary vectors into a single  Parameter �� and ���identify the total number of chromosomes allowed to take part in the operation of Where, the operations of selection, cross-over and mutation are symbolized by �� ��������respectively. ��� ������ ������ �������������  ����� � ������ � � � � �� *(9)* �������  *(7)* | 53 |

algorithm calculates this fitness as an inverse of the maximum difference between the designed and ideal frequency response of the low-pass filter and makes an attempt to minimize this difference to a significant extent. In this connection, maximum difference over the entire frequency band of interest has been regarded as the cost function of the individual chromosome.

**3. Results and Analysis**

This section demonstrates the outcome of the proposed algorithm analytically. Since the design incorporates evolutionary algorithm, convergence characteristics of our proposition has been depicted in Fig. 1 below which exhibits the variation of averaged cost function with the number of iterations for three different values of cross-over probability. Size of population has been considered as 100 in the entire analysis.

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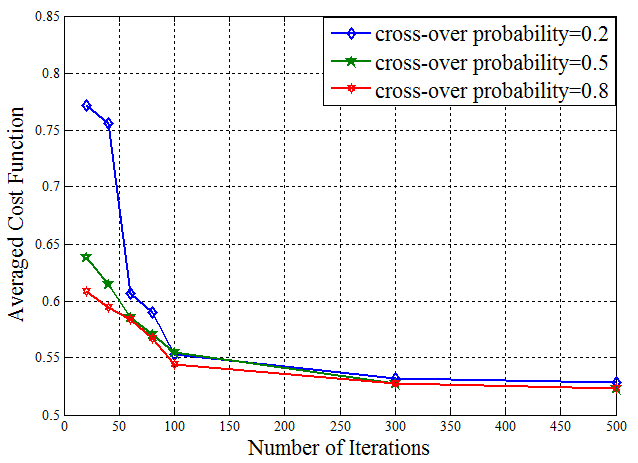


Fig. 1: Convergence characteristics of the proposed scheme

In order to establish the supremacy of the proposed design, frequency response of SORIGA-optimized multiplier-less low-pass FIR filter of order 35 has been compared with few such state-of-the-art filters in Fig. 2 below.

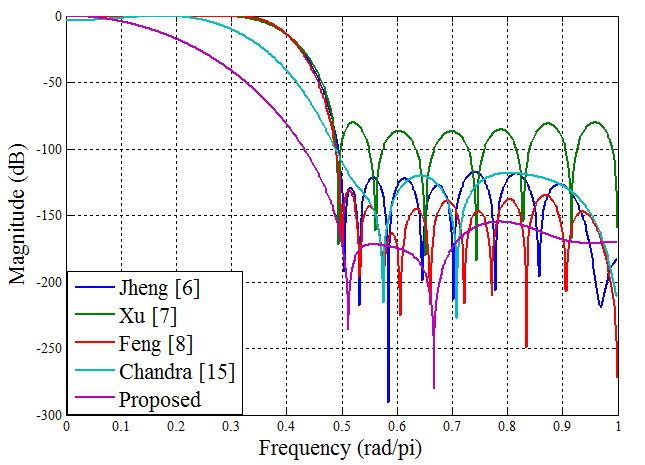


Fig. 2: Comparison in terms of frequency response amongst various multiplier-less low-pass FIR filters

It can be well apprehended from the above comparison that the proposed filter yields more attenuation in transition and stop-band region of frequency characteristics. As for example, at a frequency of 0.65 rad/pi, SORIGA-optimized filter produces an attenuation of about 193.9 dB while the filters designed in [6], [7], [8] and [15] yields approximately 151.6 dB, 180.3 dB, 157.1 dB and 120.6 dB attenuation respectively.

Subsequent part of this section elaborately describes the requirement of different hardware blocks used to realize the powers-of-two filter on an FPGA chip. Quite a few recent algorithms, nurturing the concept of multiplier-less FIR filter design, have also been considered into our analysis and the resulting hardware elements have been listed in Table 1 below. Since the filters designed by means of different algorithms are of

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different length; required number of hardware blocks per unit length of the filter has also been included for fair comparison. Word length of input signal has been taken as 8 in the entire analysis.

Table 1 Comparison in terms of hardware elements amongst different multiplier-less FIR filters

|  |
| --- |
| Name of the hardware block |
| |  |  |  |  |  | | --- | --- | --- | --- | --- | | 2-input OR | 2-input AND | 2-input XOR | Flip flop | I/O buffer | |
| |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | Algorithms | Total | Per | Total | Per | Total | Per | Total | Per | Total | Per | | unit | unit | unit | unit | unit | | length | length | length | length | length | |
| |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | Samueli [3] | 672 | 26.88 | 763 | 30.52 | 672 | 26.88 | 184 | 7.36 | 125 | 5 | |
| |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | Chen [4] | 1012 | 36.143 | 1134 | 40.5 | 1012 | 36.143 | 240 | 8.571 | 151 | 5.393 | |
| |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | Yao [5] | 1395 | 49.821 | 465 | 16.607 | 1355 | 48.393 | 216 | 7.714 | 145 | 5.179 | |
| |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | Jheng [6] | 1016 | 35.034 | 508 | 17.517 | 1016 | 35.034 | 232 | 8 | 153 | 5.276 | |
| |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | Xu [7] | 580 | 20.714 | 290 | 10.357 | 580 | 20.714 | 119 | 4.25 | 93 | 3.321 | |
| |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | Feng [8] | 871 | 25.618 | 1163 | 34.206 | 1356 | 39.882 | 285 | 8.382 | 138 | 4.059 | |
| |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | Chandra[15] | 530 | 18.276 | 531 | 18.31 | 352 | 12.138 | 65 | 2.241 | 128 | 4.414 | |
| |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | Proposed | 425 | 11.806 | 487 | 13.528 | 378 | 10.5 | 184 | 5.111 | 139 | 3.861 | |

It can be unambiguously observed from Table 1 that the proposed architecture outperforms most of the state-of-the-art multiplier-less FIR filters by a large margin in terms of the hardware blocks. However, performance of the proposed SORIGA-optimized filter is slightly inferior to that of [7] in terms of 2-input AND, flip-flop and I/O buffer counts. Architecture of the proposed filter as obtained using XILINX Design Suite 12.3 has been depicted in Fig. 3 below.

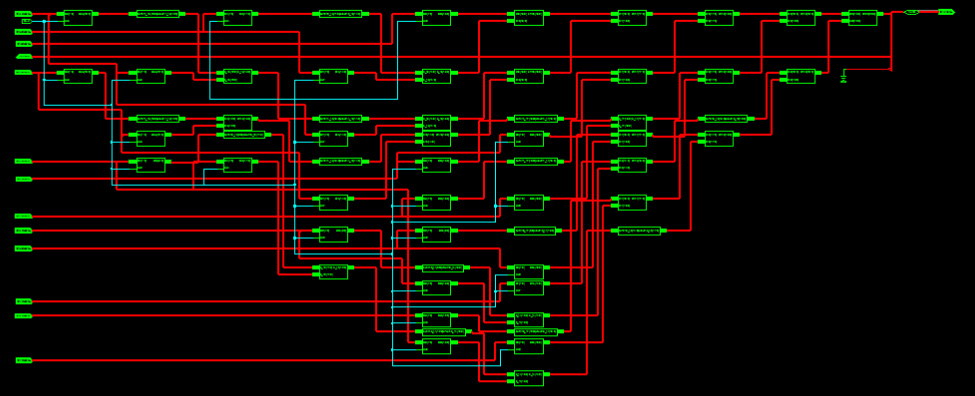


Fig. 3: RTL schematic of the proposed multiplier-less FIR filter realized on FPGA

**4. Conclusion**

This article deals with design of a multiplier-less low-pass FIR filter has been carried out by means of a recently proposed evolutionary optimization algorithm, called Self-organizing Random Immigrants Genetic Algorithm (SORIGA). Effectiveness of the optimization technique has been evaluated in terms of its convergence speed. Moreover, the supremacy of the proposed design has been established in terms of frequency response of the filter. Furthermore, tap coefficients of the designed filter have been encoded as sums of powers-of-two and implemented on a real time hardware chip using XILINX Design Suite 12.3. It

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has been observed that the proposed architecture is superior to other existing design methodologies as far as hardware complexity of the design is concerned. Performance of the solution may further be improved by proper modification of the fitness function of the optimization process as a future scope of this work.

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