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[](http://crossmark.crossref.org/dialog/?doi=10.1016/j.eij.2022.01.001&domain=pdf)Combined two-dimensional word-based serial-in/serial-out systolic processor for multiplication and squaring over *GF* 2*m*

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# a r t i c l e i n f o

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# a b s t r a c t

This paper presents a combined two-dimensional word-based serial-in/serial-out systolic processor for field multiplication and squaring over GF(2*m*) to improve hardware utilization and power consumption. The proposed processor is extracted by applying non-linear scheduling and projection functions to the algorithm dependency graph. The extracted processor features scalability that gives the designer more flexibility to control the processor size and the execution time. ASIC Implementation results of the pro- posed combined two-dimensional word-serial design and the best existing designs show that the pro- posed structure realizes a considerable saving in the area and consumed energy up to 93.7% and 98.2%, respectively. This makes it more suitable for restricted implementations of cryptographic primi- tives in resource-constrained consumer electronics devices such as hand-held devices, wearable and implantable medical devices, smart cards, wireless sensor nodes, restricted nodes in the Internet of Things (IoT), and radio frequency identification (RFID) devices.

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1. Introduction and related work

Finite field arithmetic operations are substantial in many appli- cations such as RSA cryptography [[1]](#_bookmark20), epileptic curve cryptography (ECC) [[2]](#_bookmark21), error correction codes [[3]](#_bookmark22), and pairing-based cryptogra- phy (PBC) [[4]](#_bookmark23). Field multiplication in GF(2*m*) is very crucial in sev- eral field operations such as modular exponentiation and inversion/division as they performed using a sequence of multiplications.

Most of the previously reported multipliers over GF(2*m*) have high area and time complexities that make their realization in resource-constrained consumer electronics devices are highly challenging [[5–8]](#_bookmark24). Therefore, it becomes important to have multi-

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plier architectures that target this type of applications. Word- serial multiplier architectures are reported in the literature to solve this problem. They have a trade-off between speed and area com- plexities and thus they give the designer more flexibility to reach the desired design. The structures of word-serial multipliers are classified into four types: Serial-In/Serial-Output (SISO) structures, Serial-In/Parallel-Output (SIPO) structures, Parallel-In/ Serial- Output (PISO), and Scalable structures. The polynomial basis word-serial systolic multipliers using SISO structure are presented in [[9–13]](#_bookmark17). The polynomial basis word-serial multipliers with the SIPO structure is reported in [[14–17]](#_bookmark17). The word-serial type-T Gaus- sian normal basis (GNB) multiplier with PISO structure is reported in [[18]](#_bookmark17). The scalable systolic multiplier structures are reported in [[19–25]](#_bookmark18).

Modular exponentiation is a fundamental part of cryptographic algorithms. There are two binary approaches used to compute modular exponentiation: Most Significant Bit (MSB)-first approach and Least Significant Bit (LSB)-first approach. In LSB-first approach, the modular multiplication and squaring operations can be exe- cuted concurrently to reduce the processing time. There are many attempts in the literature to combine the multiplication and squar- ing operations in a unified structure to increase performance and hardware utilization [[7,8,26]](#_bookmark25). To the best of our knowledge, the suggested combined multiplier-squarer structures are dedicated

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for high-speed applications and do not target the resource- constrained applications.

In this paper, we propose word-based two-dimensional SISO systolic processor for the combined field multiplication and squar- ing over GF(2*m*). It computes the multiplication and squaring oper- ations concurrently using a unified hardware core. The proposed processor can be managed to have the smallest size to fit all the resource-constrained applications that have more restrictions on area and power consumption. Moreover, it has a regular structure and local interconnections that make it more suitable for VLSI implementation. The proposed processor is extracted by applying non-linear scheduling and projection functions to the algorithm dependency graph [[27–32]](#_bookmark26). These non-linear functions provide the required flexibility to control the processor workload and the execution time.

This paper is organized as follows. Section [2](#_bookmark3) gives a brief expla- nation to the combined polynomial multiplication-squaring algo- rithm in *GF* 2*m* . Section [3](#_bookmark4) develops its associated dependency graph (DG). Section [4](#_bookmark7) explains the explored two-dimensional word-based SISO systolic processor. Section [5](#_bookmark14) provides the area and delay complexities of the proposed design and the best of the existing word-serial designs. Section [6](#_bookmark19) concludes this work.

1. Combined polynomial multiplication-squaring algorithmin

G/ 2m

Algorithm 1 Algorithmfor multiplication and squaring over GF(2*m*) [[7]](#_bookmark25).

Input: *C x* , *D x* , and *G x*

( ) ( ) ( )

Mult. Output:

*R*(*x*) = (*C*(*x*). *D*(*x*)) mod *G*(*x*)

Square Output: *Q x C x* . *C x* mod *G x*

( ) = ( ( ) ( )) ( )

Initialization:

*R*0 ← 0, *Q* 0 ← 0, *C*(0) ← *C*(*x*), *D* ← *D*(*x*), *G* ← *G*(*x*)

Algorithm:

1: for 1 6 *i* 6 *m*

2: *Ci* = *Ci*—1. *x* mod *G*(*x*)

3: *Ri* ← *Ri*—1 + *di*—1*Ci*—1 4: *Qi Qi*—1 *ci*—1*Ci*—1 5: end for

← +

Algorithm 2 Bit-level algorithm for multiplication and squaring over GF(2*m*).

Input: *C*(*x*), *D*(*x*), and *G*(*x*)

Mult. Output: *R*(*x*) = (*C*(*x*). *D*(*x*)) bmod *G*(*x*) Square Output: *Q x C x* . *C x* mod *G x* Initialization:

( ) = ( ( ) ( )) ( )

*m*—1

1 0

Let *C*(*x*) and *D*(*x*) be two polynomials in *GF* 2*m* and *G*(*x*) be the irreducible polynomial in standard basis representation. These

*R*0 = *r*0

*Q* 0 = *q*0

polynomials can be represented as:

*m*—1

··· *r*0*r*0 ← (0 ··· 00)

··· *q*0*q*0 ← (0 ··· 00)

1 0

*C*0 = *c*0 ··· *c*0*c*0 ← (0*cm*—1 ·· · *c*1*c*0)

*m*

1 0

*m*—1

X

*C*(*x*) =

*i*=0

*m*—1

X

*D*(*x*) =

### *cixi*

*dixi*

## (1)

(2)

*D* ← (*dm*—1 ··· *d*1*d*0) *G gm*—1 *g*1*g*0 Algorithm:

1: for 1 6 *i* 6 *m*

← ( ··· )

2: for 0 6 *j* 6 *m* — 1

=

*j*

*m*—

*i*=0

X *i*

*m*

*G*(*x*) =

*gix*

3: *ci*

*j*+1

(3)

4: *ri* = *ri*—1 + *di*—1*ci*—1

*ci*—1 +

*ci*—11*g*⟨ *j*+1⟩

*i*=0

*j j j*

5: *qi* = *qi*—1 + *ci*—1*ci*—1

where *ci*, *di*, *gi* ∈ *GF*(2).

The polynomial multiplication and squaring over *GF* 2*m* defined as follows:

can be

*j j j*

6: end for

7: end for

*R*(*x*) = *C*(*x*)*D*(*x*) mod *G*(*x*) (4)

*Q* (*x*) = *C*(*x*)*C*(*x*) mod *G*(*x*) (5)

The products *R x* and *Q x* can be calculated using the com- bined algorithm, Algorithm 1, proposed by Choi in [[7]](#_bookmark25). This algo- rithm calculates three partial polynomials *C*(*x*), *R*(*x*), and *Q* (*x*).

( ) ( )

Variables *Ci*, *Ri*, and *Qi* are used to indicate the values of

*C*(*x*), *R*(*x*) and *Q* (*x*) at iteration *i*. *di*—1 and *ci*—1 represent the (*i* — 1) coefficients of input polynomials *D*(*x*) and *C*(*x*), respec- tively. The initial variables *R*0, and *Q* 0 are assigned zero values

*th*

and the initial variable *C*0 is assigned the coefficients of input poly- nomial *C x* . In each *i* iteration of the for loop, the intermediate variables are updated as follows:

( )

Variable *Ci* is updated by shifting left *Ci*—1 and reducing using the irreducible polynomial *G*.

●

* Variable *Ri* is updated by multiplying *Ci*—1 by coefficient *di* 1 and

=

Algorithm 2 is the bit-level representation of Algorithm 1. *ci*

*j*+1

represents the ( *j* + 1 *th* bit of *C* at the *ith* iteration. Also, *ri* and *qi*

)

*j*

*j*

represent the *ith* bit of *R* and *Q* at the *ith* iteration, respectively. Notice that ⟨ *j* + 1⟩ indicates that *j* + 1 is to be reduced modulo *m*.

1. Algorithmdependency graph

Algorithm 1 is an example of a Regular Iterative Algorithm (IRA). Reference [[27]](#_bookmark26) showed how to obtain the dependency graph (DG) of an RIA algorithm. [Fig. 1](#_bookmark5) shows the DG based on Algorithm 2 for combined polynomial multiplication-squaring in *GF* 2*m* . The nodes in [Fig. 1](#_bookmark5) represent points in the two-dimensional integer domain D with indices *i* and *j* indicates the rows and columns,

respectively, and have the ranges:

1 6 *i* 6 *m*, 0 6 *j* 6 *m* — 1 (6)

adding the obtained result to *Ri*—1.

— The figure is for the case when *m* 5 bits. The algorithm has three input variables *C*, *D*, and *G*; and two output variables *R* and

* Variable *Qi* is updated by multiplying *Ci*—1 by coefficient *ci* 1 and adding the obtained result to *Qi*—1.

—

*Q*. Variables *R*, *Q* and *G* are represented by the vertical lines. Vari- able *C* is represented by the slanted lines (red lines). Input bits

*j n*(p) = l*m*m ,*i* — 1, + ,*m* — 1 — *j*, + 1 (7)

0 0

*r*4*,q*4 *,g*

0

0 0

*r*3*,q*3 *,g*4

0

*r*2*,q*2 *,g*3

0 0

*r*1*,q*1 *,g*2

0 0

*r*0*,q*0 *,g*1

*w*

*w*

*w*

*d*0 *, c*0



0

0

0

0

0

4

*c*4

4

*c*3

4

*c*2

4

*c*1

0

*d , c*

where 1 6 *i* 6 *m* l and l 6 *j* < *m* 1

[Fig. 2](#_bookmark8) shows the node timing (scheduling time) for the case when *m* 5 and *w* 2. Notice that we added an extra column on the right and extra row at the bottom to make the number of

= =

+ — —

columns and rows integer multiple of *w*. In general, we should add l extra columns and l extra rows to make the number of col-

umns and rows an integer multiple of *w*, where l = *w* *m* — *m*.

*w*

1 1 [Fig. 3](#_bookmark9) shows the node timing (scheduling time) for the case when *m* = 5, and *w* = 4. In this case l = 3, thus we had to add

*d*2 *, c*2 *d*3 *, c*3 *d*4 *, c*4

*i* three extra columns on the right and three extra rows at the bot- tom to make the number of columns and rows an integer multiple of *w*. Therefore, the LSBs of inputs *C* and *G* and LSBs of the initial

values of intermediate variables *R*, *Q* should be padded by l zeros

on the right as shown in [Fig. 3](#_bookmark9). Also, the MSBs of inputs *D* and *C* should be padded by l zeros at the bottom as shown in the same figure.

The equitemporal zones are shown as light red boxes with the associated time index values indicated in red numerals within each

zone. Notice that the bits of *ci*—1 are computed at the nodes of col-

5 5

*r ,q*

4

5*,q*5

3

5 5

*r*2*,q*2

5

*r*1*,q*1

5*,q*5

0

umn *m*

4

*r*3

5

*r*0

*m*—1

— 2 as shown in [Fig. 3](#_bookmark9) and broadcasted horizontally along

—

Fig. 1. Dependence graph for the combined multiplication-squaring algorithm for

*m* = 5.

with the bits of *di*—1 and *ci*—1 to the nodes of row *i* 1.

One last detail needs to be mentioned here and is best explained with reference to two adjacent equitemproal zones exe-

*ci*—1, *di*—1 along with the resulted intermediate bits *ci*—1 are broad-

*m*—1

cuting at times *n* and *n* + 1. [Fig. 4](#_bookmark11) illustrates this situation. The

north and east inputs to zone *i* are available at times *n* and *n* + 1,

casted horizontally. The initial bits *r*0, *q*0, *c*0, and *g*⟨ *j*+1⟩ are inputs to

*j*

*j*

*j*

respectively. However, we notice that input *C* affects only west

the DG as shown at the top of [Fig. 1](#_bookmark5). The DG nodes (circles) execute Algorithm 2 main operations, steps 3–5. Output bits *rm*, *qm* are pro-

*j j*

duced from the bottom of the DG as indicated in [Fig. 1](#_bookmark5).

The DG in [Fig. 1](#_bookmark5) can be used for design space exploration of the combined multiplication and squaring operations. The design exploration involves finding valid node scheduling functions and mapping or projecting the graph nodes to processing elements (PEs). Reference [[27]](#_bookmark26) explains how design space exploration could be performed using affine and non-linear scheduling and projec- tion functions.

The affine scheduling and projection functions can not be used to explore word-serial systolic processors. Thus, our goal is to apply the non-linear scheduling and projection techniques dis- cussed in [[27]](#_bookmark26) to the developed algorithm, Algorithm 2, to explore the most efficient two-dimension word-serial systolic processor that is able to satisfy any Input/Output (I/O) limitations/ restrictions.

1. Combined two-dimensional SISO multiplier-squarer

A SISO combined multiplier-squarer requires feeding in polyno- mials *C*, *D*, and *G* in a word-serial fashion at the start of iterations then obtaining the *Q* and *R* polynomials in a word-serial fashion.

Assume we would like to perform *w* iterations at the same time;

i.e. we would like to feed in *w* bits of the polynomial inputs and

*n*

output *Cw* and *Ce* affects only south output *Cs*. Hence at time *n* out- put *Cw* is valid while output *Cs* is not since we need to add to it *Ce*. This will result in increasing the total number of iterations needed to produce the final result by one time step. Therefore, The total number of iterations needed to complete the combined multiplica- tion/squaring computation will be given by:

*j*

0 0

*r*4*,q*4 *,g*

0

0 0

*r*3*,q*3 *,g*4

0 0

*r*2*,q*2 *,g*3

0 0

*r*1*,q*1 *,g*2

0 0

*r*0*,q*0 *,g*1

0, 0, 0

*d*0 *, c*0



0

1

*c*1

2

4

0

*c*2

4

0

4 3

*c*4

5

0

*c*4

4

0

7

*c*5

8

4

0

9

6

3

*d*1 *, c*1 *i*

*d*2 *, c*2

*d , c*

obtain *w* bits of the partial results. There are several nonlinear task 3 3

scheduling and projection functions that can be used to obtain dif-

ferent two-dimensional SISO combined multiplier-squarer. The most efficient ones are discussed in the following sections.

* 1. *Two-dimensional SISO task scheduling*

Following the scheduling methodology explained in [[27]](#_bookmark26), we can extract the following nonlinear scheduling function to parti- tion D into *w* × *w* equitemporal zones:

*d*4 *, c*4

0, 0

6

6

6

Fig. 2. Scheduling time for the case when *m* = 5 and *w* = 2.

6 6

*r ,q*

4

4

6*,q*3

*r*3

6

*r*2*,q*2

6

*r*1*,q*1

6*,q*6

*r*0

0

0, 0

*j*

*G*

*w*

*G*

*C*

*C*

*w w*

*w*

*w*

*Rin*

*Qin Gin Cin*

*w*

1 0 *M*G 1 0 *M*C

*w*

*w*

*w*

*w*

*w w*

Systolic Array

*R*

1

1

*w*

*O*

*Q*

*w*

*O*

*G C*

*O O*

*w*

*z*

*y FIFO-C*

*u*-1

*w*

*FIFO-G*

*u*-1

*w*

*w*

*w*

*R Q*

0 0

*r*4*,q*4 *,g*

0

0

0

*r*3*,q*3 *,g*4

0 0

*r*2*,q*2 *,g*3

*r*1*,q*1 *,g*2

0

0 0

*r*0*,q*0 *,g*1

0, 0, 0

0, 0, 0

0, 0, 0

*d*0 *, c*0



0

*c*1

4

0

*c*4

2

1

0

*c*3

4

0

*c*4

4

0

*c*5

4

0

*c*6

3

4

0

*c*7

4

0

4

2

0

*d*1 *, c*1 *i*

*Di-*1 *Ci-*1

*d*2 *, c*2 *d*3 *, c*3 *d*4 *, c*4

0, 0

*u*-1

*FIFO-R*

*FIFO-Q*

*u*-1

0, 0

0, 0

8 8

8

8*,* 8

0

Fig. 3. Scheduling time for the case when *m* = 5 and *w* = 4.

8 8

*r*4*,q*4

*r*3*,q*3

8

*r*2*,q*2

*r*1 *q*1

8*,q*8

*r*0

0, 0

0, 0

0, 0

*Cn*



*Cw*

zone

*n*

*Ce*

zone

*n+*1

*Cs*

Fig. 5. Word-based two-dimensional SISO systolic processor.

of *w* bits and a depth size of *u* — 1, where *u* = *m* . The word update block ensures the proper number of bits are extracted from the bottom outputs of the systolic array block shown in [Fig. 5](#_bookmark10). Notic that we added two registers for the input *C*, the north *C* register feeds the words of operand *C* to the systolic array starting from the most significant words, while the east register *Ci*—1 feeds the words of operand *C* to the systolic array starting from the least sig- nificant words.

*w*

[Fig. 6](#_bookmark12) shows the details of the two-dimensional word-based SISO systolic array for the case when *m* 5 and *w* 4. The PEs of the systolic array are divided into two different types with each type has different color. The logic details of the PEs are shown in



*Cin*

*cm-*1

*c*

*y*

*D*

*cm-*1

*c*

*y*

*D*

*c* *m-*1

*c y*

*D*

*cm-*1

*y D*

*c*

*CO*

*D*

*D*

*D*

= =

*in*

Fig. 4. Data dependencies of two adjacent equitemporal zones from [Fig. 3](#_bookmark9).

l*m*m2

*#*Iterations =

+ 1 (8)

*w*

*Rin,Q , Gin*

* + 1. *Two-dimentional SISO task projection*

Given the scheduling time in [Fig. 3](#_bookmark9), we note that only *w w* nodes are active at a given time. Following the projection tech- nique explained in [[27]](#_bookmark26), we can extract the following nonlinear

×

projection function that maps a point p *i*, *j* D of [Fig. 3](#_bookmark9) to a point

*Di-*1*,Ci-*1

( ) ∈

p in the PE space:

p(*o*, *l*) = P*siso* p(*i*, *j*) (9)

*o* = *i* mod *w* (10)

*l* = *j* mod *w* (11)

P*siso* = [ . mod *w* . mod *w* ] (12)

where ‘‘dot” is a place holder for the argument.

Our systolic array will now consist of *w*2 PEs arranged in *w* rows and *w* columns plus the necessary registers. [Fig. 5](#_bookmark10) shows the word- based two-dimensional SISO systolic processor. It consists of *w w* systolic array block as well as input/output registers and FIFO buf- fers besides two 2-input MUXes to select between the inputs of *C* and *G* and their intermediate values. The resulted intermediate

×

words of *R*, *Q* , *C* and the words of *G* are pipelined through the FIFO

buffers of *R*, *Q* , *C*, and *G*, respectively. These FIFOs have a width size

*z*

*RO ,QO , GO*

Fig. 6. Word-based two-dimensional SISO systolic array.

[Figs. 7 and 8](#_bookmark13). The light blue PEs have an extra tri-state buffer that is enabled (*y* = 0) at time steps *n* = *k*)*m*e+ 1, 0 6 *k* < )*m*e, to pass the

*w*

*w*

nal *y* = 0 forces the bits of *Ci* , 1 6 *i* 6 *w*, through the AND gate

shown in [Fig. 7](#_bookmark13) to have zero values as shown at the left edge of

computed bits of *Ci*—1 . These bits are broadcasted along with the

*m*

*w*

the DG, [Fig. 3](#_bookmark9).

input bits of *D*

*m*—1 *i*—1 and *C*

*i*—1

to the remaining nodes of the systolic

1. At time instances 1 < *n*

6 *m* , MUXs *MC*

and *MG*

still set to pass

array to compute the intermediate words of *R*, *Q* , and *C*. Also, they

have an extra AND gate to enforce the partial results of the MSBs of

the remaining words of inputs *C* and *G*, one word at each time step, to the systolic array. These operand words are used with

*C*, *ci* , to be zero at the same time instances. This is controlled by

*m*

the horizontally passed words of *Ci*—1 , *D*

*m*—1

*i*—1

and *C*

*i*—1

, 1 6 *i* 6 *w*,

the control signal *y* shown in [Fig. 7](#_bookmark13). The operation of the two- dimensional SISO systolic processor can be summarized for generic values of *m* and *w* as follows:

1. At time *n* 1, MUXes *MC* and *MG*, shown in [Fig. 5](#_bookmark10), are set to pass the *w* MSBs of operands *C* and *G*, respectively, to the systolic array block. Also, FIFO buffers of *R* and *Q* are reset at the same time to pass zero inputs to the systolic array block since the ini- tial values of *R* and *Q* are zeros as indicated in Algorithm 1. Notice that, the control signals *y* and *z* are set to 0 and 1, respec- tively, through this time step. The control signal *y* 0 enable the tristate buffer shown in [Fig. 7](#_bookmark13) for all the light blue PEs of

=

=

the systolic array, [Fig. 6](#_bookmark12), to pass the computed *w* bits of

to compute the intermediate words of *R*, *Q* , and *C* in a word serial fashion. The resulted words of *R*, *Q* , and *C* are pipelined through the FIFOs of *R*, *Q* , and *C* shown in [Fig. 5](#_bookmark10), respectively. These FIFOs have a width size of *w* bits and a depth size of

*u* — 1, where *u* = *m* . Notice that the depth of *R* and *Q* FIFOs ensures keeping the initial values of *R* and *Q* equal to zero through these time instances.

*w*

1. At time instances *n* > )*m*e, MUXs *MC* and *MG* passes the com-

*w*

puted *C* words stored in FIFO-C and the *G* words stored in FIFO-G to the systolic array, one word at each time step. These words along with the computed *R* and *Q* words, stored in FIFO-R

and FIFO-Q, and the broadcasted words of *Ci*—1 , *Di* and

*m* 1 1

—

*Ci*—1

*m*—1

, 1 6 *i* 6 *w*. The computed word of *Ci*—1

*m*—1

along with the *w*

*Ci*—1, *kw* < *i* 6 (*k* + 1)*w*, 1 6 *k* 6 )*m*e— 1, are used to update the

intermediate partial results of *R*, *Q* , and *C* in a word serial fash-

*w*

LSBs of *Di*—1 and *Ci*—1, 1 6 *i* 6 *w*, are passed horizontally to the

remaining PEs nodes of the systolic array. Also, the control sig-

ion, one word at each time step.

1. At time instances *n* = *k*)*m*e+ 1, 0 6 *k* 6 )*m*e— 1, the tri-sate buf-

=

*w*

*w*

*i-*1 *j*



*r*

*i-*1 *j*

*g<j+*1*>*

*i-*1 *j*

*c*

fer shown in [Fig. 7](#_bookmark13) is enabled (*y* 0) in all the light blue PEs of the systolic array, [Fig. 6](#_bookmark12), to pass horizontally the computed *w*

bits of *Ci*—1 , *kw* < *i* 6 (*k* + 1)*w*, along with the *w* bits of inputs

*q*

*y Di*—1

*m*—1

*Ci*—1, *kw* < *i*

and

6 (*k*

+ 1)*w*, to the remaining PEs nodes of

*i-*1

*c*

*m-*1

*ci*-1 *di*-1

the systolic array. Notice that the *Di*—1 and *Ci*—1 registers, shown in [Fig. 5](#_bookmark10), feeds the systolic array with the input words of *Di*—1 and *Ci*—1 through these time instances. Also, through these time instances the control signal (*y* = 0) forces the bits of *Ci* , *kw* < *i* 6 (*k* + 1)*w*, through the AND gate shown in [Fig. 7](#_bookmark13) to have zero values as shown at the left edge of the DG of [Fig. 3](#_bookmark9). At the remaining time instances, this control signal is equal to one.

1. Through time instances *n* = *k*)*m*e+ 1, 1 6 *k* 6 )*m*e, the control

*m*

*w*

*w*

*i j+*1

*c*

*rji* *i*

*q*

*j*

*y*

*g<j+*1*>*

signal *z* shown at the right side of [Fig. 6](#_bookmark12) is equal to zero to feed the zero values of *C*, shown at the right edge of DG of [Fig. 3](#_bookmark9), to the systolic array. At the remaining time instances, this control signal is equal to one.

1. Through time instances *n* P *m* j*m*+l—1k, the resulted output

*w w*

Fig. 7. Light blue PE details of SISO two-dimensional systolic array.

words of *R* and *Q* will be loaded in a word serial fashion, one word at each time step, in registers *R* and *Q* shown in [Fig. 5](#_bookmark10), respectively.

*i-*1 *j*



*r*

*i-*1 *j*

*g<j+*1*>*

*i-*1 *j*

*c*

An important notice that should be considered here, the vertical

*w* bit words of *R*, *Q* , and *G* and the horizontal *w* bit words of

*Ci*—1 , *Di*

*q*

and *C*

are delayed one time step inside the systolic

*m*—1 —1 *i*—1

*i-*1

*c*

*m-*1

*ci*-1 *di*-1

array as shown in [Fig. 6](#_bookmark12). This is represented by the *D* registers (squares) shown in this figure. This makes a one time step differ- ence between the PEs above the *D* registers (squares) and the PEs below of them. This time difference is attributed to the intermedi- ate words of *C*, resulted from the left column (blue cells) of the sys- tolic array shown in [Fig. 6](#_bookmark12), are produced starting from the second

time step and the words of *R*, *Q* , *G*, *Ci*—1 , *Di*

, and *C*

should be

*m*—1 1

*i*—1

*i j+*1

*c*

*rji* *i*

*q*

*j*

*g<j+*1*>*

delayed as shown in [Fig. 6](#_bookmark12) to synchronize the operation. This resulted in the extra time step needed to complete the combined multiplication/squaring computation as explained before in Eq. [(8)](#_bookmark6).

1. Complexities comparison

In this section, we compare the proposed two-dimensional

Fig. 8. Light Orange PE details of SISO two-dimensional systolic array.

word-serial combined multiplier-squarer structure and the best

of the existing word-serial multiplier structures [[12,17,33,34]](#_bookmark17) in terms of area and time complexities. The area is estimated in terms of numbers of Tri-State buffers, 2-input AND gate, 2-input XOR gate, 2-input Multiplexers, and Flip-Flops. The time is represented by latency and Critical Path Delay (CPD).

The estimated area and time complexities of the compared structures are given in [Table 1](#_bookmark15). The notations used in this table can be defined as follows:

1. *w* is the word size
2. *TA* is the delay of 2-input AND gate.
3. *TX* is the delay of 2-input XOR gate.
4. *TMUX* is the delay of 2-to-1 MUX.
5. *F*1 = 7*m* + *m*()log *m*e) + *w* + 3
6. *F*2 = 2*w*2 + 2*w*()*m*/*w*e) + 4*w* + 1
7. *F*3 = 2*w* + 3*w*()*m*/*w*e) + 2*w*

2

1. *L*1 = *w* + )*m*/*w*e2 + )*m*/*w*e
2. s1 = *TA* + ()log2*w*e+ 1)*TX*
3. s2 = *TA* + 2*TX*
4. s3 = *TA* + *TX*
5. s4 = (*w* + 1)*TA* + *wTX* + *TMUX*

For fair comparison, we added the area complexity of Input/ Output registers for each design structure.

The designs in [Table 1](#_bookmark15) are described using VHDL code and syn- thesized for *m* 409 and different values of *w* (8, 16, 32) to obtain real implementation results. We used for synthesizing the NanGate

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(15 nm, 0.8 V) Open Cell Library and Synopsys tools version 2005.09-SP2. We used the typical corner (*VDD* = 0.8 V and *Tj* = 25◦ *C*) and unit drive strength for all the utilized primitives. The obtained results are listed in [Table 2](#_bookmark16). The design metrics used to compare the proposed and the existing word-serial designs can be defined as follows:

1. Latency: is the total number of clock cycles needed to complete a single operation.
2. Area (A): is the estimated design area in terms of the equivalent area of 2-input NAND gate.
3. CPD: is the synthesised critical path delay.
4. Time (T): is the total computation time required to complete a single operation.
5. Power (P): is the consumed power obtained at 1 KHZ.
6. Energy (E): is the consumed energy which obtained by multi- plying power (P) by the total computation time (T).

For a fair comparison, the compared multiplier structures of [[12,17,33,34]](#_bookmark17) should perform multiplication and squaring opera- tions in sequence and this doubles the obtained synthesis results of the time and consumed power/energy of these designs as indi- cated in [Table 2](#_bookmark16). By observing the results in [Table 2](#_bookmark16), we can con- clude the following: 1) The proposed design structure saves area at the different values of *w* (by percentages ranging from 9.1% to 92.6% at *w* 8, 11.6% to 93.7% at *w* 16, and 20.7% to 91.9% at *w* 32) over the existing designs. 2) The design of Pan [[12]](#_bookmark17) saves 40% time, at *w* 8, over the best of the other designs including the proposed one. 3) The design of Xie [[17]](#_bookmark17) saves 0.6% and 26.5% time (at *w* 16 and *w* 32, respectively) over the best of the other designs including the proposed one. 4) The proposed design struc- ture saves energy at the different values of *w* (by percentages rang- ing from 9.6% to 97.3% at *w* 8, 17.1% to 97.5% at *w* 16, and 29.0% to 98.2% at *w* 32) over the existing designs.

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As we notice, the proposed designs have the lower area and consumed energy at most of the embedded word sizes and this makes the proposed designs are suitable for application in resource-constrained consumer electronics devices such as hand- held devices, wearable and implantable medical devices, wireless sensor nodes, smart cards, restricted nodes in IoT, and radio fre- quency identification (RFID) devices.

Table 1

Comparison between different word-serial field multipliers.

Design Tri-State AND XOR MUXs Flip-Flops Latency CPD Xie [[17]](#_bookmark17) 0 2*mw* 2*mw* + 6*m* — 6 *m* + 6 0 4*mw* + 4*m* + 2*w* 2)*m*/*w*e+ 2)log2 *w*e 2*TX*

*w*

Pan [[12]](#_bookmark17) 0 *m*,ﬃ*m*ﬃﬃﬃ

,ﬃ*m*ﬃﬃﬃﬃ*w*ﬃﬃﬃ(2 + *m*) + *w* 0 *F*1 2)p*m*ﬃﬃﬃﬃﬃ/ﬃﬃ*w*ﬃﬃﬃﬃe s1

Hua [[33]](#_bookmark27) 0 *w*2 *w*2 + 4 — 5*w* + 1(1) 0 *F*2 6*w*)*m*/*w*e2 s2

Chen [[34]](#_bookmark28) 0 *w*2 + *w w*2 + 2*w* 2*w*(2) *F*3 *L*1 s3

Proposed *w* 3*w*2 + 2*w* 3*w*2 2*w* 4*w*()*m*/*w*e— 1) + 8*w* )*m*/*w*e2 + 1 s4

1. Area of 3-input XOR gate as 1.5× a 2-input XOR gate.
2. Multiplier of [[34]](#_bookmark28) uses switches that having same transistor count as 2-input MUX.

Table 2

Implementation results of different word-serial field multipliers for *m* = 409 and different values of *w*.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Multiplier | *w* | Latency | Area (A) [*Kgates*] | CPD  [*ps*] | Time (T) [*ns*] | power (P) [*nW*] | Energy (E) [*fJ*] |
| Xie [[17]](#_bookmark17) | 8 | 324 | 92.98 | 50.8 | 16.46 | 225.56 | 3.71 |
|  | 16 | 172 | 146.96 | 50.8 | 8.74 | 375.5 | 3.28 |
|  | 32 | 98 | 195.13 | 50.8 | 4.98 | 477.4 | 2.38 |
| Pan [[12]](#_bookmark17) | 8 | 48 | 97.46 | 206.3 | 9.90 | 252.91 | 2.50 |
|  | 16 | 36 | 123.93 | 244.4 | 8.80 | 320.07 | 2.82 |
|  | 32 | 24 | 164.34 | 282.5 | 6.78 | 425.09 | 2.88 |
| Hua [[33]](#_bookmark27) | 8 | 259584 | 7.99 | 73.4 | 19053.47 | 4.35 | 82.88 |
|  | 16 | 129792 | 10.40 | 73.4 | 9526.73 | 5.85 | 55.73 |
|  | 32 | 64896 | 19.91 | 73.4 | 4763.37 | 11.15 | 53.11 |
| Chen [[34]](#_bookmark28) | 8 | 11946 | 10.16 | 55.2 | 659.42 | 5.11 | 3.37 |
|  | 16 | 3678 | 13.51 | 55.2 | 203.03 | 8.38 | 1.70 |
|  | 32 | 1572 | 26.58 | 55.2 | 86.77 | 15.95 | 1.38 |
| Proposed | 8 | 2705 | 7.26 | 215.7 | 583.47 | 3.88 | 2.26 |
|  | 16 | 677 | 9.19 | 407.7 | 276.01 | 5.12 | 1.41 |
|  | 32 | 170 | 15.78 | 791.7 | 134.59 | 7.28 | 0.98 |

6. Summary and conclusion

This paper presented new efficient two-dimensional word- based SISO systolic processor to perform the multiplication and squaring operations concurrently over *GF* 2*m* . The proposed sys- tolic processor structure shares the data-path and this leads to sav- ing more area and power resources. We applied non-linear scheduling and projection functions to the algorithm dependency graph to explore the proposed systolic processor core. The applied non-linear scheduling and projection functions give the designer more flexibility to control the processor work load and the execu- tion time. The size of the systolic array in the processor core does not depend on the field size and that makes the proposed design more suitable for implementation in embedded and ultra-low power devices. Implementation results of the proposed two- dimensional combined word-serial processor systolic structure and the best of the existing word-serial multiplication designs show that the proposed structure achieves a significant saving in area and consumed energy at different values of the embedded word sizes. This makes it more suitable for constrained implemen- tations of cryptographic primitives in resource-constrained con- sumer electronics devices such as hand-held devices, wearable and implantable medical devices, wireless sensor nodes, smart cards, restricted nodes in IoT, and radio frequency identification (RFID) devices.

Declaration of Competing Interest

The authors declare that they have no known competing finan- cial interests or personal relationships that could have appeared to influence the work reported in this paper.

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References

1. [Rivest RL, Shamir A, Adleman L. A method for obtaining digital signatures and](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0005) [public-key cryptosystems. Mag Commun ACM 1978;21(2):120–6](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0005).
2. [Lidl R, Niederreiter H. Introduction to finite fields and their](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0010) [applications. Cambridge, UK: Cambridge University Press; 1994](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0010).
3. [Reed IS, Solmon G. Polynomial codes over certain finite fields. SIAM J Appl](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0015) [Math 1960;8:300–4](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0015).
4. [Boneh D, Franklin MK. Identity-based encryption from the Weil pairing. SIAM J](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0020) [Comput 2003;32(3):586–615](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0020).
5. [Chiou C-W, Lee C-Y, Deng A-W, Lin J-M. Concurrent error detection in](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0025) [Montgomery multiplication over gf(](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0025)2*m*[). IEICE Trans Fundam Electron](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0025) [Commun Comput Sci 2006;E89-A(2):566–74](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0025).
6. [Kim KW, Jeon JC. Polynomial basis multiplier using cellular systolic](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0030) [architecture. IETE J Res 2014;60(2):194–9](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0030).
7. [Choi S, Lee K. Efficient systolic modular multiplier/squarer for fast](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0035) [exponentiation over gf(](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0035)2*m*[). IEICE Electron Express 2015;12(11):1–6](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0035).
8. [Kim KW, Kim SH. Efficient bit-parallel systolic architecture for multiplication](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0040) [and squaring over gf(](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0040)2*m*[). IEICE Electron Express 2018;15(2):1–6](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0040).
9. [Kim CH, Hong CP, Kwon S. A digit-serial multiplier for finite field GF(](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0045)2*m*[). IEEE](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0045) [Trans Very Large Scale Integr (VLSI) Syst 2005;13(4):476–83](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0045).
10. [Talapatra S, Rahaman H, Mathew J. Low complexity digit serial systolic](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0050) [Montgomery multipliers for special class of gf(](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0050)2*m*[). IEEE Trans Very Large Scale](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0050) [Integr (VLSI) Syst 2010;18(5):847–52](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0050).
11. [Guo JH, Wang CL. Hardware-efficient systolic architecture for inversion and](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0055) [division in gf(](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0055)2*m*[). IEE Proc Comput Digital Techniques 1998;145(4):272–8](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0055).
12. [Pan JS, Lee CY, Meher PK. Low-latency digit-serial and digit-parallel systolic](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0060) [multipliers for large binary extension fields. IEEE Trans Circ Syst-I 2013;60](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0060) [(12):3195–204](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0060).
13. [Lee C-Y, Fan C-C, Yuan S-M. New digit-serial three-operand multiplier over](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0065) [binary extension fields for high-performance applications. In: Proc. 2017](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0065) 2*nd* [IEEE International Conference on Computational Intelligence and Applications.](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0065)

[p. 498–502](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0065).

1. [Hariri A, Reyhani-Masoleh A. Digit-serial structures for the shifted polynomial](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0070) [basis multiplication over binary extension fields. In: Proc. LNCS Intl Workshop](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0070) [Arithmetic of Finite Fields (WAIFI). p. 103–16](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0070).
2. [Kumar S, Wollinger T, Paar C. Optimum digit serial multipliers for curve-based](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0075) [cryptography. IEEE Trans Comput 2006;55(10):1306–11](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0075).
3. Lee C-Y. Super digit-serial systolic multiplier over gf(2*m*). In Proc. 6*th* Int. Conf. Genetic Evolutionary Computing, Kitakyushu, Japan; 2012. pp. 509–513..
4. [Xie J, Meher PK, Mao Z. Low-latency high-throughput systolic multipliers over](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0085) [gf(](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0085)2*m*[) for NIST recommended pentanomials. IEEE Trans Circuits Syst 2015;62](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0085) [(3):881–90](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0085).
5. [Namin AH, Wu H, Ahmadi M. A word-level finite field multiplier using normal](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0090) [basis. IEEE Trans Comput 2011;60(6):890–5](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0090).
6. [Lee C-Y, Chiou CW, Lin JM, Chang CC. Scalable and systolic montgomery](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0095) [multiplier over generated by trinomials. IET Circuits Devices Syst 2007;1](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0095) [(6):477–84](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0095).
7. [Chen LH, Chang PL, Lee C-Y, Yang YK. Scalable and systolic dual basis](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0100) [multiplier over GF(](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0100)2*m*[). Int J Innov Comput Inf Control 2011;7(3):1193–208](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0100).
8. Orlando G, Paar C. A super-serial Galois fields multiplier for FPGAs and its application to public-key algorithms. In Proc. IEEE Symp. Field-Programm. Custom Comp.; 1999. pp. 232–239..
9. [Bayat-Sarmadi S, Kermani MM, Azarderakhsh R, Lee C-Y. Dual-basis](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0110) [superserial multipliers for secure applications and lightweight cryptographic](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0110) [architectures. IEEE Trans Circ Syst-II 2014;61(2):125–9](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0110).
10. [Gebali F, Ibrahim A. Efficient scalable serial multiplier over gf(](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0115)2*m*[) based on](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0115) [trinomial. IEEE Trans Very Large Scale Integr VLSI Syst 2015;23(10):2322–6](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0115).
11. [Ibrahim A, Gebali F, El-Simary H, Nassar A. High-performance, low-power](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0120) [architecture for scalable radix 2 Montgomery modular multiplication](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0120) [algorithm. Can J Electr Comput Eng 2009;34(4):152–7](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0120).
12. [Ibrahim A, Gebali F. Scalable and unified digit-serial processor array](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0125) [architecture for multiplication and inversion over](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0125) *gf* 2*m* [. IEEE Trans Circuits](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0125) [Syst I Regul Pap 2017;22(11):2894–906](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0125).

1. [Kim KW, Lee JD. Efficient unified semi-systolic arrays for multiplication and](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0130) [squaring over gf(](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0130)2*m*[). IEICE Electron Express 2017;14(12):1–10](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0130).
2. [Gebali F. Algorithms and Parallel Computers. New York, USA: John Wiley;](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0135) [2011](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0135).
3. [Ibrahim A, Elsimary H, Gebali F. New systolic array architecture for finite field](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0140) [division. IEICE Electron Express 2018;15(11):1–11](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0140).
4. [Ibrahim A, Elsimary H, Aljumah A, Gebali F. Reconfigurable hardware](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0145) [accelerator for profile hidden Markov models. Arab J Sci Eng 2016;41](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0145) [(8):3267–77](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0145).
5. [Ibrahim A. Scalable digit-serial processor array architecture for finite field](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0150) [division. Microelectron J 2019;85:83–91](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0150).
6. [Ibrahim A, Alsomani T, Gebali F. Unified systolic array architecture for field](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0155) [multiplication and inversion over gf(](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0155)2*m*[). Comput Electr Eng J-Elsevier](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0155) [2017;61:104–15](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0155).
7. [Ibrahim A, Alsomani T, Gebali F. New systolic array architecture for finite field](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0160) [inversion. Can J Electr Comput Eng 2017;40(1):23–30](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0160).
8. [Hua YY, Lin J-M, Chiou CW, Lee C-Y, Liu YH. Low space-complexity digit-serial](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0165) [dual basis systolic multiplier over gf(](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0165)2*m*[) using hankel matrix and karatsuba](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0165) [algorithm. IET Inf Secur 2013;7(2):75–86](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0165).
9. [Chen C-C, Lee C-Y, Lu E-H. Scalable and systolic Montgomery multipliers over](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0170) [GF(](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0170)2*m*[). IEICE Trans Fundam Electron Commun Comput Sci 2008;E91-A](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0170) [(7):1763–71](http://refhub.elsevier.com/S1110-8665(22)00001-9/h0170).