[Engineering Science and Technology, an International Journal 48 (2023) 101590](https://doi.org/10.1016/j.jestch.2023.101590)



Contents lists available at [ScienceDirect](https://www.elsevier.com/locate/jestch)

Engineering Science and Technology, an International Journal

journal homepage: [www.elsevier.com/locate/jestch](http://www.elsevier.com/locate/jestch)

[](http://crossmark.crossref.org/dialog/?doi=10.1016/j.jestch.2023.101590&domain=pdf)Full length article

Single CFOA-based active Negative Group Delay circuits for signal anticipation

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A R T I C L E I N F O A B S T R A C T

*Keywords:*

Audio signal processing

Current feedback operation amplifier Design method

Negative Group Delay NGD

Time-domain validation

The group delay of a signal prior to data monitoring is a crucial consideration in today’s real-time applications, especially for those that involve long sensor arrays or high-order filters. In this article, nine new second-order Negative Group Delay (NGD) circuits based on Current Feedback Operation Amplifier (CFOA) are proposed, and their transfer functions are demonstrated. These circuits have a wide range of applications, from audio to mechanical signals and sensor signal anticipation. An example design procedure is provided for one of the introduced circuits. A time-domain analysis is performed using both a single-tone sinusoidal and a band-limited audio recording in the frequency range of 1 Hz to 500 Hz. The article assesses the change in the signal using Root Mean Square Error (RMSE) and cross-correlation. Furthermore, the relationship between the NGD value and the operation range of the circuit is investigated and verified experimentally. The results show that an

NGD value of approximately 100 μs can be achieved with an amplitude error of 0.86% for a single-tone input

and 1.54% for an audio recording, and an operation range of about 650 Hz.

# Introduction

Negative Group Delay (NGD) is an intriguing physical phenomenon that can be utilized for signal prediction. In these circuits, the output visually appears to be time-advanced compared to the input, making signal prediction possible, but this effect does not violate the causality principle [[1](#_bookmark57)]. The crucial aspect is that the input signal must be band-limited, meaning that sudden jumps in the input signal are not allowed, and the derivatives of the input signal must remain bounded. Furthermore, NGD typically occurs within a specific frequency band in these circuits [[2](#_bookmark58)]. Although NGD can be observed in passive circuits, active elements are necessary if the output signal is to be used to drive other circuits or systems. The phase delay of a system refers to the phase shift of the single sinusoidal input to the output of that system, while the group delay denotes the time delay of the signal envelope. Group delay is an important term for systems that process signals with multiple frequency components, which is the norm in real- world applications [[3](#_bookmark59)]. A nonlinear group delay means that different phase delays occur for the different frequency components of the input, resulting in distortion in the output. There have been studies of NGD in both physics and electronics disciplines. The causality and applicability of NGD, as well as its physical aspects, are discussed in Refs. [[4](#_bookmark60)–[9](#_bookmark62)],

which show that the system does not violate causality. The output is a reshaped signal such that its peak is ahead of the input.

In this article, we presented nine new second-order single Current Feedback Operation Amplifier (CFOA)-based NGD circuits, obtained by computer-aided design method [[10](#_bookmark63)], which may be useful for commu- nication or control applications. Section [2](#_bookmark2) introduces the NGD circuit theory, describes the CFOA, a literature review of active NGD topolo- gies, and presents the new circuits. Section [3](#_bookmark10) describes the circuit design method, while a non-ideal study of a selected NGD circuit is given in Section [4](#_bookmark32). Section [5](#_bookmark37) is focused on the simulation and experimental validations. Performance comparison with selected state- of-the-art solutions is shown in Section [6](#_bookmark54). Finally, Section [7](#_bookmark55) concludes the study.

# Description of the theory, C/OA, and active NGD topologies

This section introduces the NGD circuit theory. The description of the CFOA and the literature review of active NGD topologies are presented.

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<https://doi.org/10.1016/j.jestch.2023.101590>

Received 6 August 2023; Received in revised form 10 November 2023; Accepted 24 November 2023

Available online 2 December 2023

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**/ig. 1.** (a) Phase response example of a stable NGD circuit and (b) its group delay.

**Table 1**

The NGD circuit topologies in the literature.

Reference Circuit topology Transfer function

*𝑏*2 *𝑠*2 + *𝑏*1 *𝑠* + *𝑏*0

This article introduces nine novel circuits obtained by computer- aided design method [[10](#_bookmark63)]. In [Fig.](#_bookmark19) [2](#_bookmark19), all presented circuits have a second-order TF using five passive components, as listed in [Table](#_bookmark20) [2](#_bookmark20). Although, in practice, circuits employing only grounded capacitors are preferred, new IC technologies offer floating capacitor realization pos- sibility as a double poly (poly1-poly2) or metal–insulator–metal (MIM) capacitor [[19](#_bookmark72)]. Alternatively, P-channel MOS (PMOS) varactors also implement floating capacitors [[3](#_bookmark59)]. In the introduced CFOA-based NGD

circuits, the highest-order *𝑠* parameter coefficient in the denominator

has the same value as the highest-order *𝑠* parameter coefficient in the numerator. Moreover, the coefficient of the denominator’s *𝑠* parameter can always be made smaller than the coefficient of the numerator’s *𝑠* parameter. The general TF for the second-order *𝐻*2(*𝑠*) system is given

by ([5](#_bookmark6)).

*𝑎*0 + *𝑎*1*𝑠* + *𝑎*2*𝑠*2

[[6](#_bookmark61)] OA Based Active RLC Filter

*𝑎 𝑠*2 + *𝑎 𝑠* + *𝑎 ,*

*𝐻*2(*𝑠*) = *𝑏*

+ *𝑏 𝑠* + *𝑏 𝑠*2 *,* (5)

2 1 0

0 1 2

*𝑎*1 = *𝑏*1 *, 𝑎*0 = *𝑏*0

1. Passive RLC Network (*𝑎*1 *𝑏*0 + 1)*𝑏*1 *𝑠* + *𝑎*1

*𝑏*1 *𝑎*1 *𝑠*

1. OA Based Differentiator *𝑏*1 *𝑠* + *𝑏*0

while from ([5](#_bookmark6)), the phase and group delay responses can be expressed as ([6](#_bookmark7)) and ([7](#_bookmark8)):

*𝜙* (*𝜔*) = arg *[𝐻* (*𝑗𝜔*)*]* = arctan *(*  *𝑎*1*𝜔 )* − arctan *(*  *𝑏*1*𝜔 ) ,* (6)

[[14](#_bookmark67),[17](#_bookmark70)] Passive RC Filter *𝑏*1 *𝑠* + *𝑏*0

*𝑏*1 *𝑠* + *𝑎*0 + *𝑏*0

1. OA Based Active RC Filter *𝑏*1 *𝑠* + *𝑏*0

2 2

*𝑑𝜙* (*𝜔*)

*𝑎*0 − *𝑎*2*𝜔*2

*𝑏*0 − *𝑏*2*𝜔*2

*𝑎*1 *𝑠* + *𝑎*0

1. Cascaded CFOA-Based Active Filter *𝑏*2 *𝑠*2 + *𝑏*1 *𝑠* + *𝑏*0

*𝜏𝑔*2(*𝜔*) = −

2

*𝑑𝜔*

*.* (7)

*𝑎*1 *𝑠* + *𝑎*0

* 1. *Theory and mathematical description*

In a linear time-invariant (LTI) system, for the output *𝑦* and the input *𝑥*, the transfer function (TF) of the system is given as ([1](#_bookmark9)).

*𝐻* (*𝑗𝜔*) = *𝑌* (*𝑗𝜔*) *,* (1)

*𝑋*(*𝑗𝜔*)

where *𝑌* (*𝑗𝜔*) and *𝑋*(*𝑗𝜔*) are the output and the input signal’s Laplace transforms, with (*𝑠* →←← *𝑗𝜔*), respectively. For the given system TF, the

NGD can be achieved in the second-order TFs where *𝑎*1 is smaller than *𝑏*1 and both are positive numbers. The operation ranges and

parameters are defined in the design section.

# NGD circuit design method

This section describes a CFOA-based NGD circuit synthesis method. After the topological description, the detailed NGD analysis is intro- duced.

* 1. *Description of the design example*

phase and group delay are respectively defined as ([2](#_bookmark11)) and ([3](#_bookmark12)).

*𝜙*(*𝜔*) = arg [*𝐻* (*𝑗𝜔*)] = arg(*𝑌* ) − arg(*𝑋*)*,* (2)

*𝑑𝜙*(*𝜔*)

The circuit shown in [Fig.](#_bookmark19) [2](#_bookmark19)(a) has been selected as an example to demonstrate the design method. Its TF is given in ([8](#_bookmark13)).

*𝐺*1*𝐺*2 + *𝐺*1*𝐺*3 + *𝐶*1*𝐺*1*𝑠* + *𝐶*1*𝐶*2*𝑠*2

*𝜏𝑔* (*𝜔*) = −

*.* (3)

*𝑑𝜔*

*𝐻*2(a)(*𝑠*) =

*𝐺 𝐺*

+ (*𝐶 𝐺*

– *𝐶 𝐺* )*𝑠* + *𝐶 𝐶 𝑠*2 *.* (8)

Eq. ([3](#_bookmark12)) indicates that a phase that increases monotonically with frequency results in a negative group delay. This, however, implies an unstable system. A stable system with negative group delay may have a phase response as shown in [Fig.](#_bookmark4) [1](#_bookmark4), where the phase increases to a certain point and then decreases. In this case, the group delay is negative as long as the phase is increasing with frequency [[11](#_bookmark64)].

The summary of the previously proposed NGD circuit (NGDC)

topologies can be found in [Table](#_bookmark5) [1](#_bookmark5). An intriguing electronic circuit with negative group delay is presented in [[12](#_bookmark65)]. There have been several

1 3 1 1 2 2 1 2

* + 1. *Stability constraints*

First, the stability constraints of the circuit are determined. The stability condition for the TF given in ([8](#_bookmark13)) can be found in ([9](#_bookmark14)).

*𝐶*1*𝑅*2 *> 𝐶*2*𝑅*1*.* (9)

* + 1. *The phase and group delay calculation*

The phase response of the system can be expressed as ([10](#_bookmark15)).

*( )*

studies on NGD systems utilizing active RC and RLC filters with opera- tional amplifiers (OA) [[6](#_bookmark61),[12](#_bookmark65),[13](#_bookmark66)]; passive RC and RLC networks [[11](#_bookmark64),[14](#_bookmark67)]; or through mathematical modeling of NGD-based circuits using Taylor

series prediction [[15](#_bookmark68)]. Only one topology is a cascadable NGD circuit

*𝜙*2(a)

(*𝜔*) = arctan *𝐶*1*𝐺*1*𝜔*

*𝐺*1*𝐺*2 + *𝐺*1*𝐺*3 − *𝐶*1*𝐶*2*𝜔*2

*(* (*𝐶*1*𝐺*1 − *𝐶*2*𝐺*2)*𝜔 )*

– arctan

– *𝐶 𝐶 𝜔*2

*.*

1

3

*𝐺 𝐺*

1

2

(10)

ns to μs. In the next section, novel CFOA-based active NGDCs will be based on CFOA [[16](#_bookmark69)]. The NGD values reported in the studies vary from

Using ([3](#_bookmark12)) and ([10](#_bookmark15)), the group delay is given in ([11](#_bookmark16)).

(*𝐶 𝐺* − *𝐶 𝐺* )(*𝐺 𝐺* + *𝐶 𝐶 𝜔*2)

introduced, followed by a design and application example.

*2.2. The CFOA and proposed active NGD topologies*

*𝜏𝑔* 2(a)(*𝜔*) =

1 1 2 2 1 3 1 2

(*𝐶*1*𝐺*1 − *𝐶*2*𝐺*2)2*𝜔*2 + (*𝐺*1*𝐺*3 − *𝐶*1*𝐶*2*𝜔*2)2

– *𝐶*1*𝐺*1[*𝐺*1(*𝐺*2 + *𝐺*3) + *𝐶*1*𝐶*2*𝜔*2]

(11)

*.*

*𝐶*2*𝐺*2*𝜔*2 + [*𝐺* (*𝐺* + *𝐺* ) − *𝐶 𝐶 𝜔*2]2

The mathematical description of the CFOA is given in ([4](#_bookmark17)) [[18](#_bookmark71)].

1 1 1 2 3 1 2

*⎡* − *⎤* = *⎡*0 1 0*⎤ ⎡*

*𝑣* 1 0 0 *𝑣*+*⎤*

(4)

In the design parameters section, the component values are selected to meet the conditions ([12](#_bookmark18)) at low frequencies.

*𝑖*Z

*⎣𝑣*W*⎦*

*⎢ ⎥*

*⎥ ⎢ ⎥*

*⎢⎣*0 0 1

*𝑖*− *.*

*⎦ ⎣𝑣*Z *⎦*

*𝐶*1*𝐺*1*𝜔*

*𝐺*1*𝐺*2 + *𝐺*1*𝐺*3 − *𝐶*1*𝐶*2*𝜔*2

*<* 1*,*

(*𝐶*1*𝐺*1 − *𝐶*2*𝐺*2)*𝜔*

*𝐺*1*𝐺*3 − *𝐶*1*𝐶*2*𝜔*2

*<* 1*.* (12)





**/ig. 2.** (a)–(i) Proposed second-order NGD circuits.

**Table 2**

The transfer functions *𝐻* (*𝑠*) of proposed second-order circuits, depicted in [Fig](#_bookmark19). [2](#_bookmark19), 1/Gn = Rn.

1 3 1 1 2 2 1 2

|  |  |
| --- | --- |
| Circuit Transfer function Matching condition | # Passive components |
| *𝐺*1 *𝐺*2 + *𝐺*1 *𝐺*3 + *𝐶*1 *𝐺*1 *𝑠* + *𝐶*1 *𝐶*2 *𝑠*2  (a) *𝐶*1 *𝐺*1 *> 𝐶*2 *𝐺*2  *𝐺 𝐺* + (*𝐶 𝐺* − *𝐶 𝐺* )*𝑠* + *𝐶 𝐶 𝑠*2 | 5 |
| *𝐺*1 *𝐺*2 + *𝐺*2 *𝐺*3 + (*𝐶*1 *𝐺*2 + *𝐶*2 *𝐺*1 )*𝑠* + *𝐶*1 *𝐶*2 *𝑠*2  (b) *𝐶*1 *𝐺*2 + *𝐶*2 *𝐺*1 *> 𝐶*2 *𝐺*3  *𝐺 𝐺* + (*𝐶 𝐺* + *𝐶 𝐺* − *𝐶 𝐺* )*𝑠* + *𝐶 𝐶 𝑠*2 | 5 |
| *𝐺*1 *𝐺*2 + *𝐶*1 *𝐺*1 *𝑠* + *𝐶*1 *𝐶*2 *𝑠*2  (c) *𝐶*1 *𝐺*1 + *𝐶*2 *𝐺*3 *> 𝐶*2 *𝐺*2  *𝐺 𝐺* + (*𝐶 𝐺* + *𝐶 𝐺* − *𝐶 𝐺* )*𝑠* + *𝐶 𝐶 𝑠*2 | 5 |
| *𝐺*1 *𝐺*2 + 2*𝐺*1 *𝐺*3 + *𝐶*1 *𝐺*1 *𝑠* + *𝐶*1 *𝐶*2 *𝑠*2  (d) 2*𝐺 𝐺* + (*𝐶 𝐺* − *𝐶 𝐺* )*𝑠* + *𝐶 𝐶 𝑠*2 *𝐶*1 *𝐺*1 *> 𝐶*2 *𝐺*2 | 5 |
| *𝐺*1 *𝐺*3 + *𝐺*1 *𝐺*2 + (*𝐶*1 *𝐺*1 + *𝐶*1 *𝐺*3 )*𝑠* + *𝐶*1 *𝐶*2 *𝑠*2  (e) *𝐶*1 *𝐺*1 + *𝐶*1 *𝐺*3 *> 𝐶*2 *𝐺*2 ; *𝐺*1 *> 𝐺*2  *𝐺 𝐺* − *𝐺 𝐺* + (*𝐶 𝐺* + *𝐶 𝐺* − *𝐶 𝐺* )*𝑠* + *𝐶 𝐶 𝑠*2 | 5 |
| *𝐺*1 *𝐺*3 + *𝐺*1 *𝐺*2 + (*𝐶*1 *𝐺*1 + *𝐶*2 *𝐺*1 + *𝐶*2 *𝐺*3 )*𝑠* + *𝐶*1 *𝐶*2 *𝑠*2  (f) *𝐶*1 *𝐺*1 + *𝐶*2 *𝐺*1 + *𝐶*2 *𝐺*3 *> 𝐶*2 *𝐺*2  *𝐺 𝐺* + (*𝐶 𝐺* + *𝐶 𝐺* + *𝐶 𝐺* − *𝐶 𝐺* )*𝑠* + *𝐶 𝐶 𝑠*2 | 5 |
| *𝐺*1 *𝐺*2 + *𝐺*1 *𝐺*3 + (*𝐶*1 *𝐺*1 + *𝐶*2 *𝐺*1 )*𝑠* + *𝐶*1 *𝐶*2 *𝑠*2  (g) *𝐶*1 *𝐺*1 + *𝐶*2 *𝐺*1 *> 𝐶*2 *𝐺*2  *𝐺 𝐺* + (*𝐶 𝐺* + *𝐶 𝐺* − *𝐶 𝐺* )*𝑠* + *𝐶 𝐶 𝑠*2 | 5 |
| *𝐺*1 *𝐺*2 + (*𝐶*1 *𝐺*1 + *𝐶*2 *𝐺*1 )*𝑠* + *𝐶*1 *𝐶*2 *𝑠*2  (h) *𝐶*1 *𝐺*1 + *𝐶*2 *𝐺*1 + *𝐶*2 *𝐺*3 *> 𝐶*2 *𝐺*2  *𝐺 𝐺* + (*𝐶 𝐺* + *𝐶 𝐺* − *𝐶 𝐺* + *𝐶 𝐺* )*𝑠* + *𝐶 𝐶 𝑠*2 | 5 |
| *𝐺*1 *𝐺*2 + 2*𝐺*1 *𝐺*3 + (*𝐶*1 *𝐺*1 + *𝐶*2 *𝐺*1 )*𝑠* + *𝐶*1 *𝐶*2 *𝑠*2  (i) 2*𝐺 𝐺* + (*𝐶 𝐺* + *𝐶 𝐺* − *𝐶 𝐺* )*𝑠* + *𝐶 𝐶 𝑠*2 *𝐶*1 *𝐺*1 + *𝐶*2 *𝐺*1 *> 𝐶*2 *𝐺*2 | 5 |

1 2 1 2 2 1 2 3 1 2

1 3 1 1 2 3 2 2 1 2

1 3 1 1 2 2 1 2

1 3 2 3 1 1 1 3 2 2 1 2

1 3 1 1 2 1 2 3 2 2 1 2

1 3 1 1 2 1 2 2 1 2

1 3 1 1 2 1 2 2 2 3 1 2

1 3 1 1 2 1 2 2 1 2

The values of the capacitors are in the order of 10−9 Farads, while the conductance values are in the order of 10−4 Siemens.

The phase response in ([10](#_bookmark15)) is approximated as ([13](#_bookmark21)):

*𝜙* (*𝜔*) ≅ *𝐶*1*𝐺*1*𝜔* − (*𝐶*1*𝐺*1 − *𝐶*2*𝐺*2)*𝜔 .* (13)

factor in our case in terms of the NGD value, and it is assumed to determine the frequency where the group delay changes from negative to positive. The frequency at which the group delay changes from negative to positive is estimated by finding the root of the denominator

2(a)

*𝐺*1*𝐺*2 + *𝐺*1*𝐺*3 − *𝐶*1*𝐶*2*𝜔*2

*𝐺*1*𝐺*3 − *𝐶*1*𝐶*2*𝜔*2

of the second term and is given in ([15](#_bookmark22)).

* + 1. *Zero cross frequency calculation*

Using ([3](#_bookmark12)) and ([13](#_bookmark21)), the approximate group delay can be expressed as ([14](#_bookmark23)).

*𝜔𝑧𝑒𝑟𝑜*\_*𝑐𝑟𝑜𝑠𝑠*\_2(a)

≅ *𝑅*2 + *𝑅*3 *.* (15)

*𝑅*1*𝑅*2*𝑅*3*𝐶*1*𝐶*2

*√*

*𝜏𝑔* 2(a)(*𝜔*) =

(*𝐶*1*𝐺*1 − *𝐶*2*𝐺*2)(*𝐺*1*𝐺*3 + *𝐶*1*𝐶*2*𝜔*2) (*𝐶*1*𝐶*2*𝜔*2 − *𝐺*1*𝐺*3)2

(14)

Note that this is a rough estimate of the zero crossing frequency

and does not give its actual value. The exact value can be determined from the simulation graph. Considering above given conditions and to

– *𝐺*1*𝐶*1(*𝐺*1*𝐺*2 + *𝐺*1*𝐺*3 + *𝐶*1*𝐶*2*𝜔*2)

(*𝐶*1*𝐶*2*𝜔*2 − *𝐺*1*𝐺*2 − *𝐺*1*𝐺*3)2

The first term of ([14](#_bookmark23)) is positive at low frequencies in accordance with the stability condition ([9](#_bookmark14)). Meanwhile, the second term of ([14](#_bookmark23)) is

simplify the design complexity, ([14](#_bookmark23)) is reduced to ([16](#_bookmark24)). This reduced form is used in the group delay calculations within the stability region.

*𝜏* (*𝜔*) ≅ − *𝐶*1*𝐺*1 + *𝐶*1*𝐺*1 − *𝐶*2*𝐺*2 *.* (16)

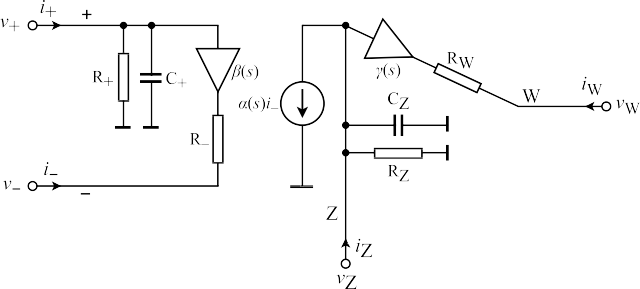
negative at low frequencies. The second term of ([14](#_bookmark23)) is the dominant

*𝑔* 2(a)

*𝐺*1*𝐺*3 + *𝐺*1*𝐺*2 − *𝐶*1*𝐶*2*𝜔*2

*𝐺*1*𝐺*3 − *𝐶*1*𝐶*2*𝜔*2

At low frequencies, the group delay becomes as in ([17](#_bookmark25)):



*𝜏* (*𝜔*) ≅ − *𝐶*1*𝐺*1 + *𝐶*1*𝐺*1 − *𝐶*2*𝐺*2 *.* (17)

*𝑔* 2(a)

*𝐺*1*𝐺*3 + *𝐺*1*𝐺*2

*𝐺*1*𝐺*3

* 1. *Design simplification & constraints*

To simplify the calculation of NGD, equal resistances are selected, as expressed by Eq. ([18](#_bookmark26)):

*𝑅*1 = *𝑅*2 = *𝑅*3*.* (18)

Moreover, the capacitance values are selected as:

*𝐶*2 = *𝛼𝐶*1*,* where 0 *< 𝛼* ≤ 1*.* (19)

By rearranging Eqs. ([15](#_bookmark22)) and ([17](#_bookmark25)) with the assumption of equal resistor values, the expressions ([20](#_bookmark27)) are obtained.

*𝜏𝑔*

(*𝜔*) ≅ *𝐶*1*𝑅*1 *(* 1 − *𝛼) , 𝜔𝑧𝑒𝑟𝑜*\_*𝑐𝑟𝑜𝑠𝑠*\_2(a) ≅ *√* 2

1 *.* (20)

The magnitude of the NGD decreases as the operating frequency increases. Therefore, it is necessary to maximize the magnitude of both values at the same time when the group delay is negative.

2(a)

2

*𝛼 𝑅*1*𝐶*1

* 1. *Performance metric*

The zero crossing of the NGD function is given in ([15](#_bookmark22)), where the NGD value changes from negative to positive at that frequency. Therefore, a Figure of Merit (FoM) is determined as [[17](#_bookmark70)]:

**/ig. 3.** An equivalent non-ideal circuit of CFOA including parasitic impedances.

terminals of the CFOA, respectively. Parameters *𝛼*(*𝑠*), *𝛽*(*𝑠*), and *𝛾*(*𝑠*) are, respectively, frequency-dependent non-ideal current and voltage gains. Ideally, these parameters are equal to unity. Using a single-pole model,

they can be defined as ([24](#_bookmark30)):

*𝛼*o

*𝛽*o

*𝛾*o

*√* 2 *(* 1 *)*

FoM = *𝜔𝑧𝑒𝑟𝑜*\_*𝑐𝑟𝑜𝑠𝑠*\_2(a) × *𝜏𝑔* 2(a)(*𝜔*) ≅

– *𝛼*

*,* (21)

*𝛼*

*𝛽*

*𝛾*

2

*𝛼*

*𝛼*(*𝑠*) = 1 + *𝜏 𝑠 , 𝛽*(*𝑠*) = 1 + *𝜏 𝑠 , 𝛾*(*𝑠*) = 1 + *𝜏 𝑠 .* (24)

where 0 *< 𝛼* ≤ 1. Note that the product of the zero crossing point

can be achieved when *𝛼* = 1, which is the stability margin point and the NGD value is given in ([21](#_bookmark29)). By minimizing ([21](#_bookmark29)), the NGD

where the two capacitors are equal in value. Eq. ([21](#_bookmark29)) also shows that the stability boundary occurs where the magnitude of the NGD value and the operating frequency range are maximized. To achieve a stable

system, *𝑅*2 is selected to be larger than *𝑅*1, when the capacitors are

selected equal valued. The parameters for this selection are introduced

CFOA, respectively. The bandwidths 1∕*𝜏𝛼* , 1∕*𝜏𝛽* , and 1∕*𝜏𝛾* depend on the

fabrication of devices. In current technologies, also used for the fabri-

Here, *𝛼*o is DC current, and *𝛽*o and *𝛾*o are DC voltage gains of the

cation of Analog Devices AD844AN [[20](#_bookmark73)], the order of a few gigarad/s is ideally equal to infinity. Hence, at low and medium frequencies,

i.e., *𝑓 ≪* (1∕(2*𝜋*)) × min{1∕*𝜏𝛼,* 1∕*𝜏𝛽 ,* 1∕*𝜏𝛾* }, ([24](#_bookmark30)) becomes:

*𝛼*(*𝑠*) ≅ *𝛼* = 1 + *𝜀𝛼*i *, 𝛽*(*𝑠*) ≅ *𝛽* = 1 + *𝜀𝛽*v *, 𝛾*(*𝑠*) ≅ *𝛾* = 1 + *𝜀𝛾*v *,* (25)

whereas *𝜀* , *𝜀* , and *𝜀* are current and voltage tracking errors,

in the Section [5](#_bookmark37).

*𝛼*i

*𝛽*v

*𝛾*v

1 1

*| |*

It is important to note that in some cases, the gain can be reduced

respectively, and satisfy the inequalities *𝜀𝛼*i *≪*

1.

*| |*

, *|𝜀𝛽*v *| ≪*

, and

to zero when the group delay is negative. Therefore, the gain of the system at low frequencies is expressed as ([22](#_bookmark31)):

( ≅ 0) ≅ 1 + *𝑅*3 *.* (22)

*𝜀𝛾*v *≪*

Considering the non-ideal current and voltage gains of the CFOA and re-analyzing the proposed circuits depicted in [Fig.](#_bookmark19) [2](#_bookmark19), a routine analysis yields non-ideal TFs of the circuits, presented in [Table](#_bookmark34) [3](#_bookmark34).

*|𝐻 𝜔* [*|*](#_bookmark31)

*𝑅*2

Eq. ([22](#_bookmark31)) shows that a gain exists in the frequencies of operation where NGD is achieved.

# Non-ideal and parasitic effects analysis

The present section is focused on a non-ideal study of the proposed NGD circuit.

* 1. *Description of non-ideal CFOA*

An equivalent non-ideal circuit of CFOA, including parasitic impedance, is shown in [Fig.](#_bookmark28) [3](#_bookmark28). Using standard notation, relations between its individual terminals can be described by the following hybrid matrix ([23](#_bookmark33)):

* 1. *Non-ideal analysis of the design example*

For a complete analysis of the circuit, it is also important to consider in detail the non-idealities of the readily available CFOA device Analog Devices AD844AN [[20](#_bookmark73)], as also shown in [Fig.](#_bookmark28) [3](#_bookmark28), where:

* the parasitic resistance *𝑅*+ and parasitic capacitance *𝐶*+ appear between the high-impedance terminal + of the CFOA and ground and their values are *𝑅*+ = 10 M*𝛺* ∥ *𝐶*+ = 2 pF, respectively,
* the non-zero parasitic resistance *𝑅*− at current input terminal −

has value *𝑅*− = 50 *𝛺*,

* the parasitic resistance *𝑅*Z and parasitic capacitance *𝐶*Z appear between the auxiliary terminal Z of the CFOA and ground and their values are *𝑅*Z = 3 M*𝛺* ∥ *𝐶*Z = 4*.*5 pF, respectively,
* the non-zero parasitic resistance *𝑅*W at voltage output terminal

*⎡ 𝑖*+ *⎤*

*⎡ 𝑌*+ 0 0 0 *⎤ ⎡𝑣*+*⎤*

W has value *𝑅*W = 15 *𝛺*.

*𝑣*− *𝛽*(*𝑠*) *𝑍*− 0 0 *𝑖*−

*⎢ ⎥* = *⎢ ⎥ ⎢ ⎥ ,* (23)

Taking into account the non-ideal current and voltage gains of the

*⎢ 𝑖*Z *⎥*

*⎢* 0 *𝛼*(*𝑠*) *𝑌*Z

0 *𝑣*Z

*⎥ ⎢ ⎥*

2(a)

CFOA and simultaneously the effect of non-idealities as mentioned

*⎢⎣𝑣*W*⎥⎦*

*⎢⎣* 0 0 *𝛾*(*𝑠*) *𝑍*W*⎦ ⎣𝑖*W*⎦*

above and re-analyzing the proposed NGD circuit shown in [Fig.](#_bookmark19) [2](#_bookmark19)(a),

and *𝑍𝑘*

where *𝑌*+ = *𝑠𝐶*+ + 1∕*𝑅*+, *𝑌*Z = *𝑠𝐶*Z + 1∕*𝑅*Z are parasitic admittances

the coefficients *𝑎𝑚* and *𝑏𝑚* for *𝑚* = {0*,* 1*,* 2} of non-ideal TF *𝐻* ′′

= *𝑅𝑘*

(*𝑘* = − and W) are the parasitic resistances at relevant

phase *𝜙*′′

(*𝜔*), and group delay *𝜏*′′ (*𝜔*)

2(a)

responses in ([5](#_bookmark6))–([7](#_bookmark8)) are as

*𝑔*2

(*𝑠*),

**Table 3**

Non-ideal transfer functions *𝐻* ′(*𝑠*) of proposed second-order circuits, depicted in [Fig](#_bookmark19). [2](#_bookmark19), 1/Gn = Rn.

(a) *𝐶*1 *G*1 + *𝛼𝛾𝐶*2 *G*3 *> 𝛼𝛽𝛾𝐶*2 (*G*2 + *G*3 )

|  |  |
| --- | --- |
| Circuit Transfer function Matching condition | # Passive components |
| *𝛾 (𝛼𝛽G*1 *G*2 + *𝛼𝛽G*1 *G*3 + *𝐶*1 *G*1 *𝑠* + *𝐶*1 *𝐶*2 *𝑠*2*)* | 5 |
| *𝛾 [G*1 *G*2 + *𝛼𝛽G*2 *G*3 + (*𝐶*2 *G*1 + *𝐶*1 *G*2 )*𝑠* + *𝐶*1 *𝐶*2 *𝑠*2*]* | 5 |
| *𝛾*(*𝛼𝛽G*1 *G*2 + *𝐶*1 *G*1 *𝑠* + *𝐶*1 *𝐶*2 *𝑠*2)  (c) *𝐶*1 *G*1 + *𝐶*2 *G*3 *> 𝛼𝛽𝛾𝐶*2 *G*2  *G G* + (*𝐶 G* − *𝛼𝛽𝛾𝐶 G* + *𝐶 G* )*𝑠* + *𝐶 𝐶 𝑠*2 | 5 |
| (d) *𝐶*1 *G*1 + *𝐶*2 *G*3 (1 + *𝛼*) *> 𝛽𝛾𝐶*2 [*𝛼*(*G*2 + *G*3 ) + *G*3 ]  *G G* + *𝛼G G* + [*𝐶 G* − *𝛼𝛽𝛾𝐶 G* + *𝐶 G* (1 + *𝛼* − *𝛽𝛾* − *𝛼𝛽𝛾*)]*𝑠* + *𝐶 𝐶 𝑠*2 | 5 |
| 1 3 1 3 1 1 2 2 2 3 1 2 |  |
| (e) *𝐶*1 *G*1 + *𝐶*1 *G*3 + *𝐶*2 *G*3 *> 𝛾𝐶*2 (*𝛼𝛽G*2 + *G*3 ); *G*1 *> 𝛼𝛽G*  *G G* − *𝛼𝛽G G* + [*𝐶 G* − *𝛼𝛽𝛾𝐶 G* + *𝐶 G* + *𝐶 G* (1 − *𝛾*)]*𝑠* + *𝐶 𝐶 𝑠*2 | 2 5 |
| 1 3 2 3 1 1 2 2 1 3 2 3 1 2 |  |
| *𝛾 [𝛼𝛽G*1 *G*2 + *G*1 *G*3 + (*𝐶*1 *G*1 + *𝐶*2 *G*1 + *𝐶*2 *G*3 )*𝑠* + *𝐶*1 *𝐶*2 *𝑠*2*]* | 5 |
| *𝛾 [𝛼𝛽G*1 *G*2 + *𝛼𝛽G*1 *G*3 + (*𝐶*1 *G*1 + *𝐶*2 *G*1 )*𝑠* + *𝐶*1 *𝐶*2 *𝑠*2*]* | 5 |
| *𝛾 [𝛼𝛽G*1 *G*2 + (*𝐶*1 *G*1 + *𝐶*2 *G*1 )*𝑠* + *𝐶*1 *𝐶*2 *𝑠*2*]* | 5 |
| *𝛾 [𝛼𝛽G*1 *G*2 + *𝛽G*1 *G*3 + *𝛼𝛽G*1 *G*3 + (*𝐶*1 *G*1 + *𝐶*2 *G*1 )*𝑠* + *𝐶*1 *𝐶*2 *𝑠*2*]* | 5 |

*𝛼𝛾G G* + [*𝐶 G* − *𝛼𝛽𝛾𝐶 G* + *𝛼𝛾𝐶 G* (1 − *𝛽*)]*𝑠* + *𝐶 𝐶 𝑠*2

1 3 1 1 2 2 2 3 1 2

(b) *𝐶*1 *G*2 + *𝐶*2 *G*1 *> 𝛼𝛽𝛾𝐶*2 *G*3

*G G* + (*𝐶 G* + *𝐶 G* − *𝛼𝛽𝛾𝐶 G* )*𝑠* + *𝐶 𝐶 𝑠*2

1 2 1 2 2 1 2 3 1 2

1 3 1 1 2 2 2 3 1 2

(f)

*𝛾 (𝛼𝛽G*1 *G*2 + *𝛽G*1 *G*3 + *𝛼𝛽G*1 *G*3 + *𝐶*1 *G*1 *𝑠* + *𝐶*1 *𝐶*2 *𝑠*2*)*

*𝛾 [𝛼𝛽G*1 *G*2 + *G*1 *G*3 + (*𝐶*1 *G*1 + *𝐶*1 *G*3 )*𝑠* + *𝐶*1 *𝐶*2 *𝑠*2*]*

*G G* + (*𝐶 G* + *𝐶 G* − *𝛼𝛽𝐶 G* + *𝐶 G* )*𝑠* + *𝐶 𝐶 𝑠*2 *𝐶*1 *G*1 + *𝐶*2 *G*1 + *𝐶*2 *G*3 *> 𝛼𝛽𝐶*2 *G*2

1 3 1 1 2 1 2 2 2 3 1 2

(g) *𝐶*1 *G*1 + *𝐶*2 *G*1 + *𝛼𝛾𝐶*2 *G*3 *> 𝛼𝛽𝐶*2 (*G*2 + *G*3 )

*𝛼𝛾G G* + [*𝐶 G* + *𝐶 G* − *𝛼𝛽𝐶 G* − *𝛼𝐶 G* (*𝛽* − *𝛾*)]*𝑠* + *𝐶 𝐶 𝑠*2

1 3 1 1 2 1 2 2 2 3 1 2

(h) *𝐶*1 *G*1 + *𝐶*2 *G*1 + *𝐶*2 *G*3 *> 𝛼𝛽𝐶*2 *G*2

*G G* + (*𝐶 G* + *𝐶 G* − *𝛼𝛽𝐶 G* + *𝐶 G* )*𝑠* + *𝐶 𝐶 𝑠*2

1 3 1 1 2 1 2 2 2 3 1 2

(i) *𝐶*1 *G*1 + *𝐶*2 [*G*1 + *G*3 (1 + *𝛼*)] *> 𝛽𝐶*2 [*𝛼*(*G*2 + *G*3 ) + *G*3 ]

*G G* + *𝛼G G* + [*𝐶 G* + *𝐶 G* − *𝛼𝛽𝐶 G* + *𝐶 G* (1 + *𝛼* − *𝛽* − *𝛼𝛽*]*𝑠* + *𝐶 𝐶 𝑠*2

1 3 1 3

1 1 2 1

2 2 2 3 1 2

*𝑎*0 = *𝛽G*1[*𝛼𝛾*(*G*2 + *G*3) + *G*3*G*Z*𝑅*W]*,*

*𝑎*1 = *𝛾𝐶*1(*G*1 + *G*+)(*G*2*𝑅*− + *G*3*𝑅*− + 1) + *G*1*𝑅*W[*𝛽G*3(*𝐶*1 + *𝐶*Z) + *𝐶*2*G*Z(1 + *G*2*𝑅*− + *G*3*𝑅*−)]*,*

*𝑎*2 = (*G*2*𝑅*− + *G*3*𝑅*− + 1)[*𝛾𝐶*1(*𝐶*2 + *𝐶*+) + *𝐶*2*G*1*𝑅*W(*𝐶*1 + *𝐶*Z)]*,*

*𝑏*0 = (*G*1 + *G*+)(*G*Z + *𝛼𝛾G*3 + *G*2*G*Z*𝑅*− + *G*3*G*Z*𝑅*W + *G*2*G*3*G*Z*𝑅*W*𝑅*− + *G*3*G*Z*𝑅*−)*,*

*𝑏*1 = *G*3{*𝑅*−{*𝑅*W{*G*Z[*𝐶*2(*G*1 + *G*2 + *G*+) + *G*2*𝐶*+] + *G*2(*𝐶*1 + *𝐶*Z)(*G*1 + *G*+)} + *G*Z(*𝐶*2 + *𝐶*+) + (*𝐶*1 + *𝐶*Z)(*G*1 + *G*+)}

+ *𝑅*W{*G*Z[*𝐶*2(1 − *𝛽*) + *𝐶*+] + (*𝐶*1 + *𝐶*Z)(*G*1 + *G*+)} − *𝛼𝛾*[*𝐶*2(*𝛽* − 1) − *𝐶*+]} + *G*2*𝑅*−[*𝐶*2*G*Z*𝑅*W(*G*1 + *G*+)

+ *G*Z(*𝐶*2 + *𝐶*+) + (*𝐶*1 + *𝐶*Z)(*G*1 + *G*+)] + *𝐶*2*G*Z*𝑅*W(*G*1 + *G*+) + *G*Z(*𝐶*2 + *𝐶*+) − *𝛼𝛽𝛾𝐶*2*G*2 + (*𝐶*1 + *𝐶*Z)(*G*1 + *G*+)*,*

*𝑏*2 = *𝐶*2{*𝑅*W{*𝑅*−{*G*3[(*G*1 + *G*2 + *G*+)(*𝐶*1 + *𝐶*Z) + *G*Z*𝐶*+] + *G*2[(*G*1 + *G*+)(*𝐶*1 + *𝐶*Z) + *𝐶*+*G*Z]} − *G*3(*𝐶*1 + *𝐶*Z)(*𝛽* − 1)

+ (*G*1 + *G*+)(*𝐶*1 + *𝐶*Z) + *𝐶*+*G*Z} + (1 + (*G*2 + *G*3)*𝑅*−)(*𝐶*1 + *𝐶*Z)} + *𝐶*+(*𝐶*1 + *𝐶*Z)[*G*3*𝑅*W(*G*2*𝑅*− + 1) + *𝑅*−(*G*2 + *G*3) + 1]*.*

(26)

**Box I.**

in [Box](#_bookmark35) [I](#_bookmark35). The effect of non-idealities on the proposed NGD circuit can be significantly minimized by properly selecting external passive components and/or by the precise design of the CFOA.

# Simulations and experimental validations

**Table 4**

Description of the 4th-order SK-LPF with Bessel response.

Pass-band/Stop-band Frequency (Hz) 100/1 k

Gain (V/V) 1

Stop-band Attenuation (dB) −65.9

Group Delay (μs) 3400

The present section is focused on the simulation and experimental validations.

* 1. *Simulation results*

*|𝐻*

Using Eq. ([22](#_bookmark31)) gives ([28](#_bookmark38)):

(*𝜔* ≅ 0) ≅ 2*.* (28)

*|*

To achieve a NGD operation range of up to 650 Hz, the capacitors

in the stability region with constant *𝑅*3. The empty space on the right In [Fig.](#_bookmark42) [4](#_bookmark42), it is shown that the negative group delay is almost constant

on the left side represents the unstable region. Additionally, when *𝑅*1 part of the plot represents positive group delay, while the empty space and *𝑅*2 are equal, *𝑅*3 affects the group delay value. However, it can

are selected as follows:

*𝐶*1 = *𝐶*2 = 22 nF*.* (29)

As mentioned, this selection is based on Eq. ([15](#_bookmark22)). To mitigate the

risk of instability in the system, the value of resistor *𝑅* is set 2% higher

be seen in [Fig.](#_bookmark42) [4](#_bookmark42) that *𝑅*3 does not affect whether the group delay is positive or negative when *𝑅*1 and *𝑅*2 are equal. For design purposes,

than the other resistors, with a scaling factor of

2

*𝛽* = 0*.*98. The param-

let us also assume *𝑅*3 is equal to *𝑅*1 and *𝑅*2 as a starting point. This

results in the flexibility of achieving NGD with the single parameter

*𝐶*1 = *𝐶*2, without dependence on gain. The NGD and NGD range can be

seen in [Fig.](#_bookmark44) [5](#_bookmark44). The capacitor values are selected as 2.2 nF, 22 nF, and

220 nF. The higher the capacitor value, the higher the NGD, but this also decreases the operation frequency given in ([15](#_bookmark22)).

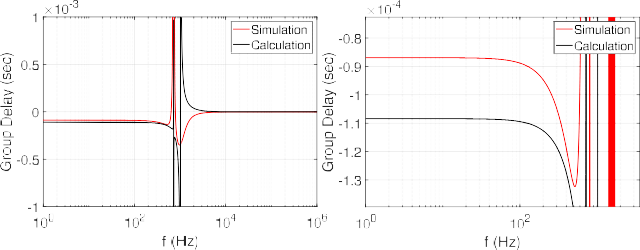
The resistors are selected as:

*𝑅*1 = *𝑅*2*𝛽* = *𝑅*3 = 10 kΩ*.* (27)

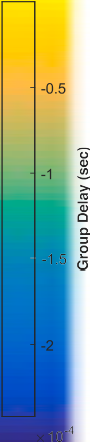
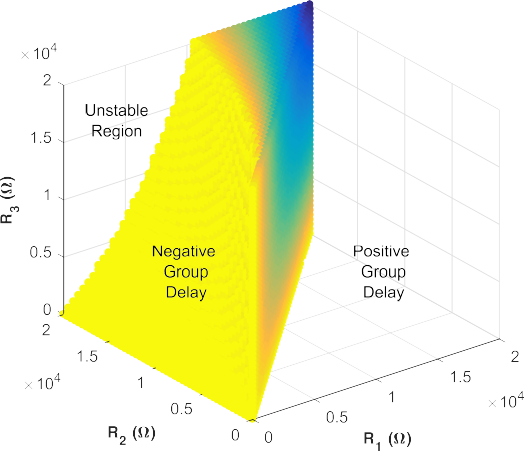
eters specified in ([27](#_bookmark40)) and ([29](#_bookmark39)) are used to generate the results shown

in [Fig.](#_bookmark44) [5](#_bookmark44), which demonstrates that the base-band gain is independent of the NGD value. The simulation results and theoretical calculations of the group delay are in good agreement at low frequencies, up to 650 Hz, as demonstrated in [Fig.](#_bookmark41) [6](#_bookmark41). The simulation was performed using the Analog Devices AD844AN [[20](#_bookmark73)] and OP200 [[21](#_bookmark74)] SPICE models and LT Spice simulation software.

The proposed NGD circuit was tested using a 4th-order Sallen-Key low-pass filter (SK-LPF) topology with Bessel response, as depicted in

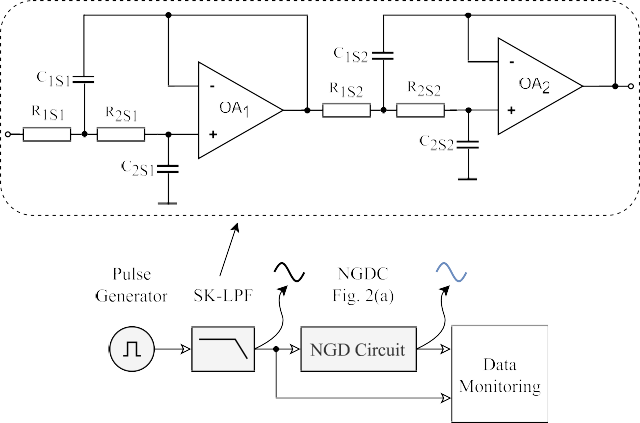




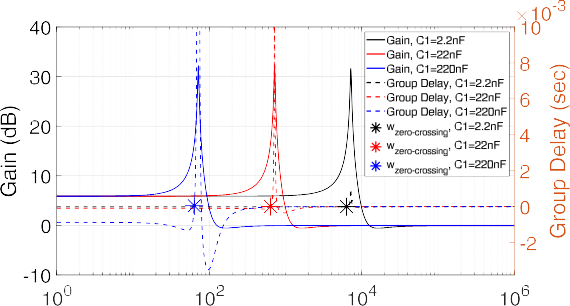
**/ig. 6.** Calculated and simulated (a) group delay-frequency responses, (b) zoom at low frequency.

**/ig. 4.** Group delay vs. resistors @100 Hz, *𝑅*1, *𝑅*2, and *𝑅*3 swept from 1 Ω to 20 kΩ,

*𝐶*1 = *𝐶*2 = 22 nF.

**/ig. 7.** Block diagram of the test system.



**/ig. 5.** AC analysis of the circuit II. *𝑅*1 = *𝑅*2 *𝛽* = *𝑅*3 = 10 kΩ, *𝐶*1 = *𝐶*2 is 2*.*2 nF, 22 nF, and 220 nF, *𝛽* = 0*.*98 factor of *𝑅*2 for the stability.

**Table 5**

4th-Order SK-LPF passive component values.

**Table 7**

**Table 6**

The component values of NGD circuit shown in [Fig.](#_bookmark19) [2](#_bookmark19)(a).

Components Values

*𝑅*1*,*2*,*3 (kΩ) 9.8, 10.26, 9.8

*𝐶*1*,*2 (nF) 22, 22

Performance comparison of the circuit in [Fig.](#_bookmark19) [2](#_bookmark19)(a).

|  |  |  |
| --- | --- | --- |
| Components | Values  Simulation | Experiments |
| *𝑅*1*𝑠*1*,*2*𝑠*1*,*1*𝑠*2*,*2*𝑠*2 (kΩ) | 9.76, 11.8, 5.76, 6.65 | 9.64, 11.76, 5.71, 6.57 |
| *𝐶*1*𝑠*1*,*2*𝑠*1*,*1*𝑠*2*,*2*𝑠*2 (nF) | 110, 100, 261, 100 | 116, 100, 262, 95 |

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter | Calculation | Simulation | Experiment |
| NGD (μs) | 108 | 101.6–112.5 | 98.4 |
| Flat Group Delay Range (Hz) | 1–650 | 1–650 | 700 |

[Fig.](#_bookmark43) [7](#_bookmark43). The simulation was again performed using the Analog Devices AD844AN [[20](#_bookmark73)] and OP200 [[21](#_bookmark74)] SPICE models and LT Spice simulation software. The parameters of the SK-LPF are summarized in [Table](#_bookmark36) [4](#_bookmark36), and the passive component values selected for the SK-LPF are listed in [Table](#_bookmark45) [5](#_bookmark45). The test was conducted by applying a pulse input signal to the test circuit and operation range of NGD up to 650 Hz was achieved. To illustrate the time advancement at the output of the NGD, a zoom of time-domain responses is provided in [Fig.](#_bookmark48) [8](#_bookmark48)(a). To validate the circuit in a practical application, the SK-LPF in the circuit shown in [Fig.](#_bookmark43) [7](#_bookmark43) was substituted with an audio signal. The input audio signal was filtered to be within the operational range of the NGD, up to 500 Hz. The time-domain responses are presented in [Fig.](#_bookmark48) [8](#_bookmark48)(b) and [Fig.](#_bookmark48) [8](#_bookmark48)(c). The simulation results are in good agreement with theory.

*5.2. Experimental verification*

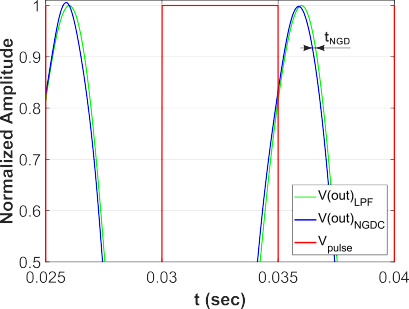
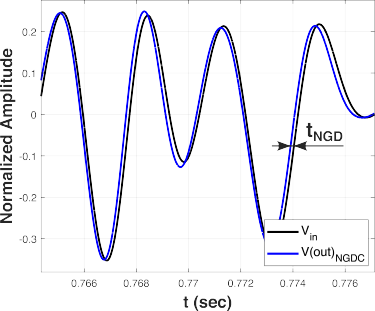
The experiment was performed to demonstrate the correlation be- tween the simulated and measured values of the NGD circuit. The circuit in [Fig.](#_bookmark19) [2](#_bookmark19)(a) was used for the setup, which consisted of an Analog Devices AD844AN [[20](#_bookmark73)], an OA OP200 [[21](#_bookmark74)] for the SK-LPF, a signal generator AFG3032C Tektronix, a signal analyzer MDO3104 Tektronix,

supplied by ±12 V. The component values used for the 4th-order SK- and a voltage supply SPD-3606 GW INSTEK; see [Fig.](#_bookmark49) [9](#_bookmark49). Amplifiers were

LPF and NGD circuit are listed in [Table](#_bookmark45) [5](#_bookmark45) and [Table](#_bookmark46) [6](#_bookmark46), respectively, and correspond to the circuit schematic in [Fig.](#_bookmark43) [7](#_bookmark43). The measurement

of capacitor values (*𝐶*1 = *𝐶*2 = 2*.*2 nF) on the operation range of results are depicted in [Fig.](#_bookmark50) [10](#_bookmark50). Moreover, to demonstrate the impact

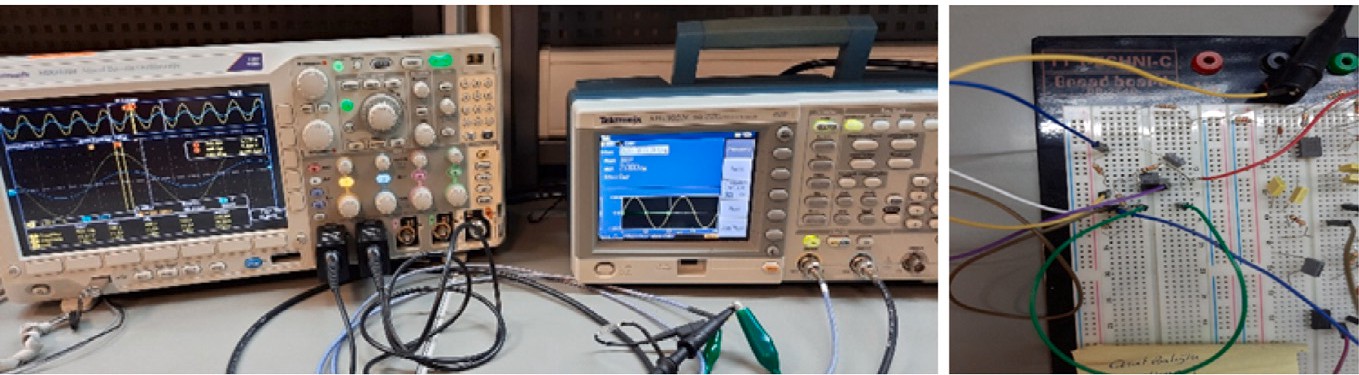
the NGD circuit, the system was subjected to a sinusoidal input, as shown in [Fig.](#_bookmark52) [11](#_bookmark52). The results are in good agreement with the theory, as demonstrated in [Table](#_bookmark47) [7](#_bookmark47).

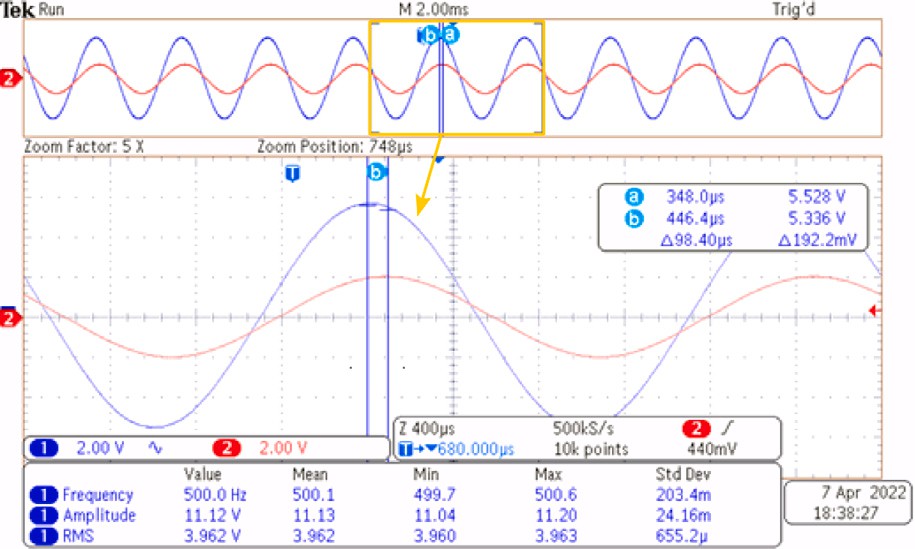
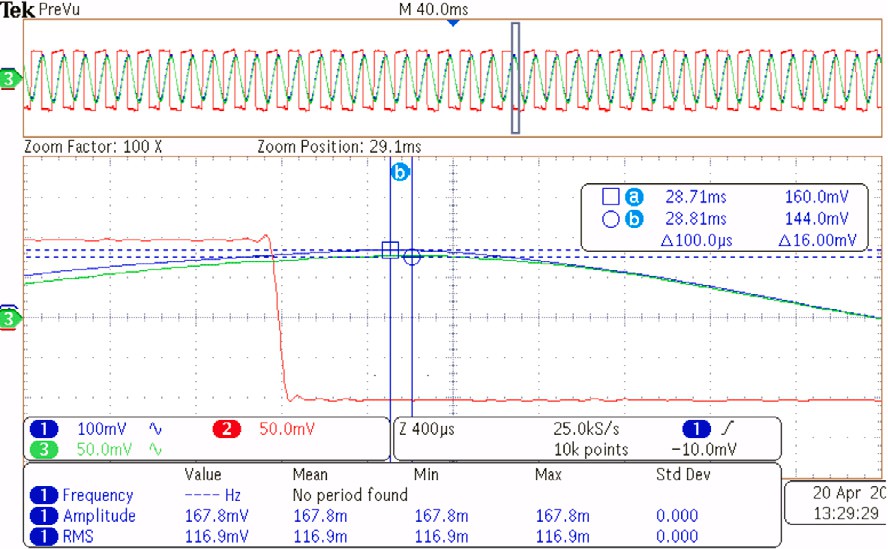




**/ig. 8.** Time domain results: (a) Simulated NGDC output with SK-LPF output (zoom in 0*.*025 *< 𝑡 <* 0*.*04 s, (b) audio input and NGDC output with *𝐶*1 = *𝐶*2 = 22 nF, a 1 second record; (c) its zoom. (Red—square wave input signal, green—output of SK-LPF, blue—output of NGDC.)



**/ig. 9.** Measurement setup.



**/ig. 10.** Measured time domain results of a NGDC with 100 μs value. (Red—square

wave input signal, green—output of SK-LPF, blue—output of NGDC.)

**Table 8**

Performance comparison with state-of-the-art solutions.

**/ig. 11.** Measured time domain results of a NGDC with 98*.*40 μs value. (Red—input

of the NGD circuit, blue—output of the NGD circuit.)

circuit, respectively. *𝑎* and *𝑏* are the starting and ending indices of the sampled signals. The input and output signals of the NGD circuit were

sampled with *𝑇𝑠𝑎𝑚𝑝𝑙𝑒 < |𝜏𝑛𝑔𝑑 |* to perform the calculations in MATLAB,

|  |  |  |  |
| --- | --- | --- | --- |
| Reference | This study | [[16](#_bookmark69)] | [[17](#_bookmark70)](a) |
| NGD | 100 μs | 800 ns | 100 μs |
| Flat Group Delay Range | 650 Hz | 10 kHz | ≅150 Hz[a](#_bookmark53) |
| RMSE (Single Tone) | 0.0086 | 0.0674 | 0.0013 |
| RMSE (Audio Record) | 0.0154 | 0.0012 | 0.0053 |

a The NGD operation range is 1 kHz [[17](#_bookmark70)].

# Performance comparison

Performance comparison with selected state-of-the-art solutions is given in [Table](#_bookmark51) [8](#_bookmark51). The Root Mean Square Error (RMSE) was calculated as follows:

where *𝑖* is the index of the sampled input and output signals. It is noted

that the term *𝜏𝑛𝑔𝑑* ∕*𝑇𝑠𝑎𝑚𝑝𝑙𝑒* is selected as an integer and *𝜏𝑛𝑔𝑑* is a negative

value of the group delay.

# Conclusion

Nine new single CFOA-based second-order NGD topologies, includ- ing a comprehensive design methodology, are presented. Presented circuits perform slightly differently in the time and frequency domain due to the real performance of the CFOA and matching conditions. The simulation results demonstrate that these active NGD circuits are

*√√√*  1 *∑𝑏 (*

RMSE =

*𝑏* − *𝑎*

*𝑥𝑖𝑛*[*𝑖*] − *𝑥𝑜𝑢𝑡*[*𝑖* + *𝜏𝑛𝑔𝑑* ∕*𝑇𝑠𝑎𝑚𝑝𝑙𝑒*]

*𝑖*=*𝑎*

suitable for low-frequency applications, with a group delay of approx-

2

*.* (30)

imately 100 μs achieved in the frequency range of 1 Hz to 650 Hz.

The proposed parameters offer a unique advantage as the NGD value

*)*

In Eq. ([30](#_bookmark56)), *𝑥𝑖𝑛*[*𝑖*] and *𝑥𝑜𝑢𝑡*[*𝑖* + *𝜏𝑛𝑔𝑑* ∕*𝑇𝑠𝑎𝑚𝑝𝑙𝑒*] represent the normalized

input to the NGD circuit and the normalized delayed output of the NGD

can be achieved without dependency on gain, providing a specific NGD operation range.

# CRediT authorship contribution statement

**Onat Baloglu:** Conceptualization, Software, Validation, Formal analysis, Investigation, Data curation, Writing – original draft, Writing – review & editing, Visualization. **Oguzhan Cicekoglu:** Conceptualization, Methodology, Formal analysis, Writing – orig- inal draft, Writing – review & editing, Supervision, Project administration. **Norbert Herencsar:** Conceptualization, Methodology, Resources, Writing – original draft, Writing – review & editing, Visualization, Supervision, Funding acquisition.

# Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

# Acknowledgment

The authors would like to acknowledge the technical support pro- vided by the Information Technologies Institute (BTE) at the Infor- matics and Information Security Research Center (TUBITAK, BILGEM), Kocaeli, Turkey.

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