MP2263

Wide Input 3.3V - 30V, 3A, 12µA I_Q, Synchronous, Step-Down Converter with External Soft Start and Power Good in Small 2x3mm QFN Package

The Future of Analog IC Technology

DESCRIPTION

The MP2263 is a frequency-programmable (350kHz to 2.5MHz), synchronous, step-down, switching regulator with integrated, internal, high-side and low-side power MOSFETs. The MP2263 provides 3A of highly efficient output current with current-mode control for fast loop response.

The wide 3.3V-to-30V input range accommodates a variety of step-down applications. A 1µA shutdown mode quiescent current allows the MP2263 to be used in battery-powered applications.

High power conversion efficiency over a wide load range is achieved by scaling down the switching frequency at light-load condition to reduce switching and gate driving losses.

An open-drain power good signal indicates the output.

Frequency foldback helps prevent inductor current runaway during start-up. Thermal shutdown provides reliable and fault-tolerant operation. High-duty cycle and low drop-out mode are provided for battery-powered systems.

The MP2263 is available in a QFN-15 (2mmx3mm) package.

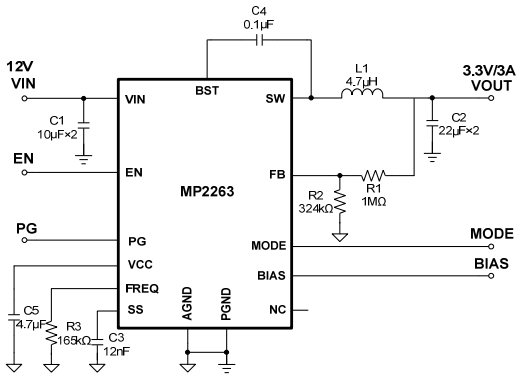
FEATURES

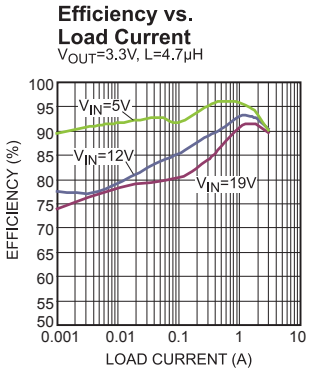
- Wide 3.3V to 30V Operating Voltage Range
- 3A Continuous Output Current
- 1µA Low Shutdown Supply Current
- 12µA Sleep Mode Quiescent Current
- 90mΩ/38mΩ High-Side/Low-Side $R_{DS(ON)}$ for Internal Power MOSFETs
- 350kHz to 2.5MHz Programmable Switching Frequency
- Power Good Output
- External Soft Start
- 80ns Minimum On Time
- Selectable Forced PWM Mode and Auto PFM/PWM Mode
- Low Dropout Mode
- Hiccup Over-Current Protection (OCP)
- Available in a QFN-15 (2mmx3mm) Package

APPLICATIONS

- Battery-Powered Systems
- Smart Homes
- Wide Input Range Power Supplies
- Standby Power Supplies

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2263GD	QFN-15 (2mmx3mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP2263GD–Z)

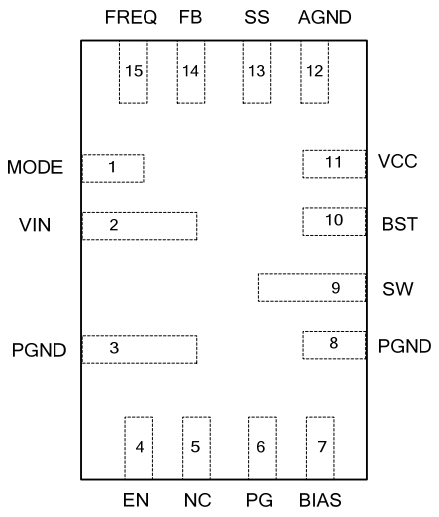
TOP MARKING

ATL
YWW
LLL

ATL: Product code of MP2263GD
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-15 (2mmx3mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.3V to 40V
Switch voltage (V_{SW}) .....-0.6V (-5V < 5ns) to V_{IN} + 0.3V (43V < 5ns)
BST voltage (V_{BST}) ..... $V_{SW (MAX)}$ + 6.5V
EN voltage (V_{EN}) ..... -0.3V to 40V
BIAS voltage ..... -0.3V to 20V
All other pins ..... -0.3V to 6V
Continuous power dissipation (T_A = +25°C) (2)
QFN-15 (2mmx3mm)..... 1.7W
Operating junction temperature..... 150°C
Lead temperature..... 260°C
Storage temperature.....-65°C to 150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 3.3V to 30V
Operating junction temp (T_J).....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-15 (2mmx3mm)	70	15	°C/W

NOTES:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C(5), typical values are at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN under-voltage lockout threshold rising	$INUV_{Vth}$		2.5	2.8	3.2	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			150		mV
VIN quiescent current	I_Q	FB = 0.85V, no load, sleep mode		12		µA
VIN shutdown current	I_{SHDN}	EN = 0V		1	5	µA
FB voltage	V_{FB}	T_J = -40°C to +125°C	784	800	816	mV
		T_J = 25°C	792	800	808	mV
Switching frequency	F_{SW}	R_{FREQ} = 164k	425	500	575	kHz
		R_{FREQ} = 82k	850	1000	1150	kHz
		R_{FREQ} = 27k	2250	2500	2750	kHz
Minimum on time(6)	T_{ON_MIN}			80		ns
Switch current limit	I_{LIMIT_HS}	Duty cycle = 40%	4.1	5.2	6.7	A
Valley current limit	I_{LIMIT_LS}	V_{OUT} = 3.3V, L = 4.7µH	3.1	4.4	5.7	A
ZCD current	I_{ZCD}			0.1		A
LS reverse current limit	$I_{LIMIT\_REVERSE}$			3		A
Switch leakage current	I_{SW_LKG}			0.01	1	µA
HS switch on resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		90		mΩ
LS switch on resistance	R_{ON_LS}			38		mΩ
MODE high level			V_{CC} - 0.4			V
MODE low level					0.4	V
MODE internal pull-down resistance	R_{MODE}			1.55		MΩ
Soft-start current	I_{SS}	V_{SS} = 0.8V		10		µA
EN rising threshold voltage	V_{EN_RISING}		0.9	1.05	1.2	V
EN hysteresis voltage	V_{EN_HYS}			120		mV
PG OV rising (V_{FB}/0.8V)	$PG_{Vth\_OV\_Rising}$		105	110	115	%
PG OV falling (V_{FB}/0.8V)	$PG_{Vth\_OV\_Falling}$		113	118	123	%
PG UV rising (V_{FB}/0.8V)	$PG_{Vth\_UV\_Rising}$		85	90	95	%
PG UV falling (V_{FB}/0.8V)	$PG_{Vth\_UV\_Falling}$		79	84	89	%
PG output voltage low	V_{PG_LOW}	I_{SINK} = 2mA		0.2	0.4	V
PG deglitch timer rising	$T_{PG\_DEGLITCH\_Rising}$			34		µs
PG deglitch timer falling	$T_{PG\_DEGLITCH\_Falling}$			57		µs
Thermal shutdown(6)	T_{SD}			170		°C
Thermal shutdown hysteresis(6)	T_{SD_HYS}			20		°C

NOTES:

5) Not tested in production. Guaranteed by over-temperature correlation.
6) Guaranteed by characterization test.

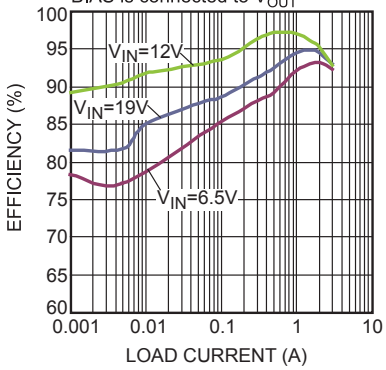
PIN FUNCTIONS

Pin # QFN-15 (2mmx3mm)	Name	Description
1	MODE	**Mode selection.** Pull MODE low or float MODE to set auto PFM/PWM mode; pull MODE to VCC to set forced PWM mode. MODE is pulled down internally. Select MODE before the part starts up.
2	VIN	**Input supply.** VIN supplies power to all of the internal control circuitries and the power switch connected to SW. A decoupling capacitor to ground must be placed close to VIN to minimize switching spikes.
3, 8	PGND	**Power ground.**
4	EN	**Enable.** Pull EN below the specified threshold to shut down the MP2263. Pull EN above the specified threshold to enable the MP2263.
5	NC	**No connection.** NC must be left floating.
6	PG	**Power good output.** The output of PG is an open drain.
7	BIAS	**Bias input.** BIAS must be connected to GND if the bias function is not used.
9	SW	**Switch node.** SW is the output of the internal power switch.
10	BST	**Bootstrap.** BST is the positive power supply for the high-side MOSFET driver connected to SW. Connect a bypass capacitor between BST and SW.
11	VCC	**Internal LDO output.** VCC supplies power to the internal control circuit and gate drivers. A decoupling capacitor to ground is required close to VCC.
12	AGND	**Analog ground.**
13	SS	**Soft-start input.** Place a capacitor from SS to GND to set the soft-start period. The MP2263 sources 10μA from SS to the soft-start capacitor at start-up. As the SS voltage rises, the feedback threshold voltage increases to limit the inrush current during start-up.
14	FB	**Feedback input.** Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.8V.
15	FREQ	**Switching frequency set.** Connect a resistor from FREQ to ground to set the switching frequency.

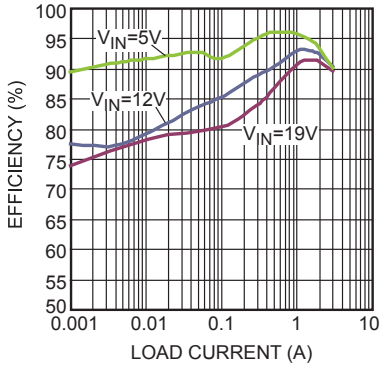
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section. V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, F_{SW} = 500kHz, C_{SS} = 12nF, T_A = 25°C, BIAS is connected to GND, unless otherwise noted.

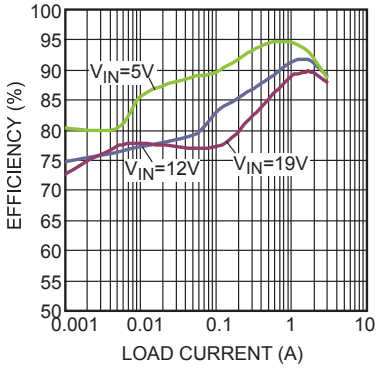
Efficiency vs. Load Current
V_{OUT}=5V, L=4.9µH, BIAS is connected to V_{OUT}



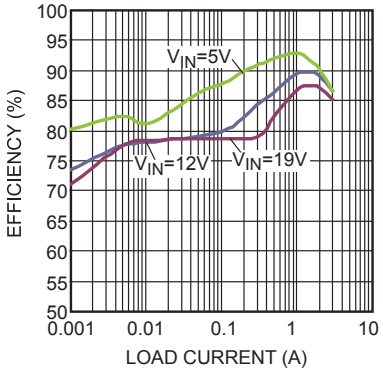
Efficiency vs. Load Current
V_{OUT}=3.3V, L=4.7µH



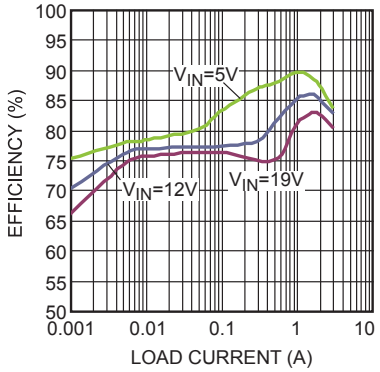
Efficiency vs. Load Current
V_{OUT}=2.5V, L=3.3µH



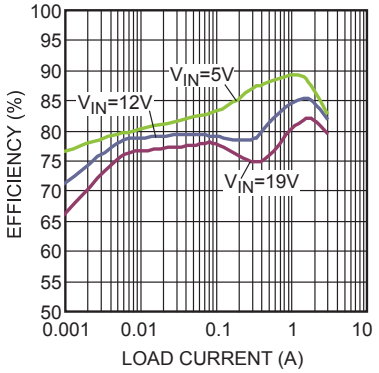
Efficiency vs. Load Current
V_{OUT}=1.8V, L=2.2µH



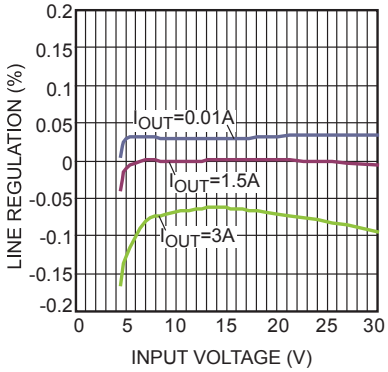
Efficiency vs. Load Current
V_{OUT}=1.2V, L=1.5µH



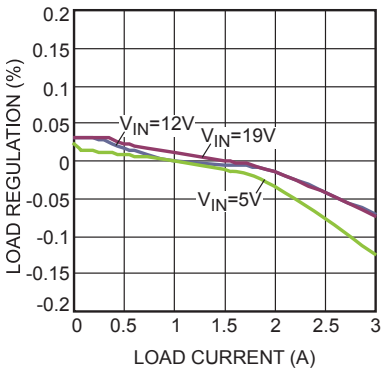
Efficiency vs. Load Current
V_{OUT}=1.05V, L=1.2µH



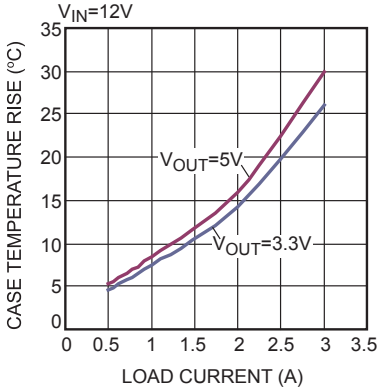
Line Regulation
V_{IN}=4.5V to 30V



Load Regulation
I_{OUT}=0.01A to 3A



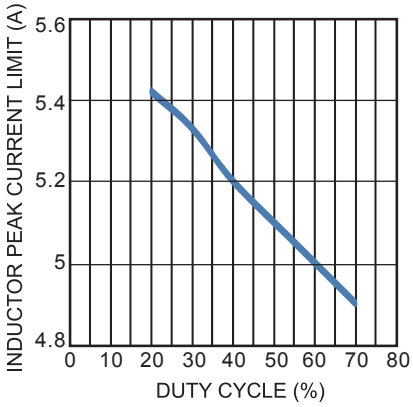
Case Temperature Rise vs. Load Current
V_{IN}=12V



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

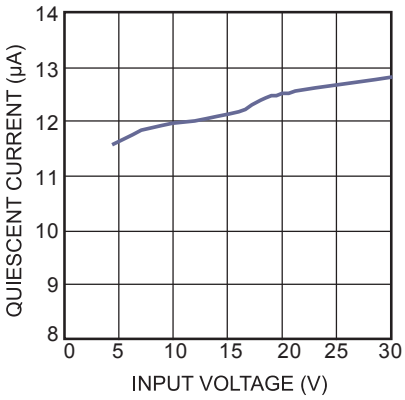
Performance waveforms are tested on the evaluation board of the Design Example section. V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, F_{SW} = 500kHz, C_{SS} = 12nF, T_A = 25°C, BIAS is connected to GND, unless otherwise noted.

Inductor Peak Current Limit vs. Duty Cycle



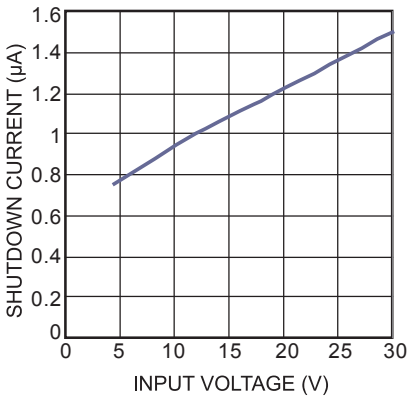
Quiescent Current vs. Input Voltage

V_{IN}=4.5V to 30V, V_{EN}=2V, V_{FB}=0.85V



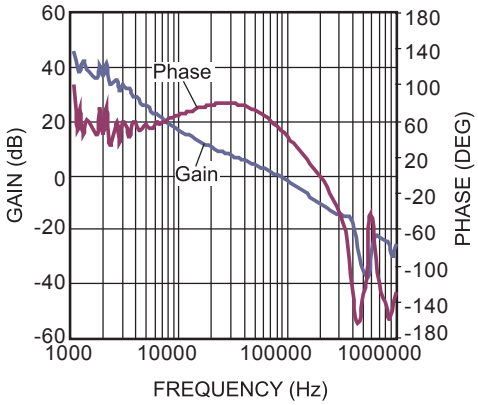
Shutdown Current vs. Input Voltage

V_{IN}=4.5V to 30V, V_{EN}=0V



Bode Plot

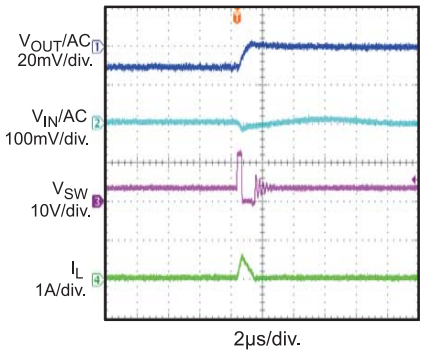
I_{OUT}=3A



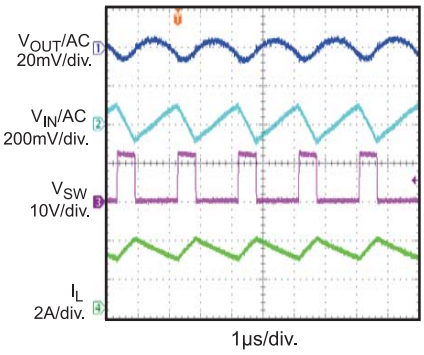
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section. V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, F_{SW} = 500kHz, C_{SS} = 12nF, T_A = 25°C, BIAS is connected to GND, unless otherwise noted.

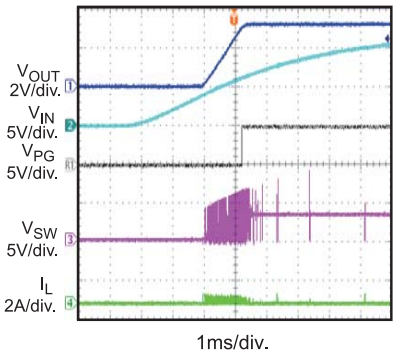
Input/Output Ripple
I_{OUT} = 0A



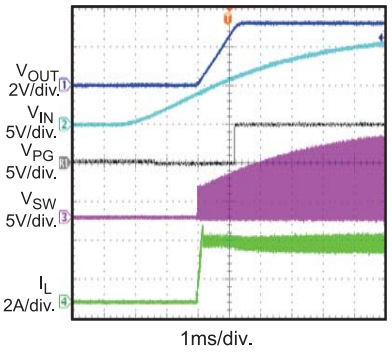
Input/Output Ripple
I_{OUT} = 3A



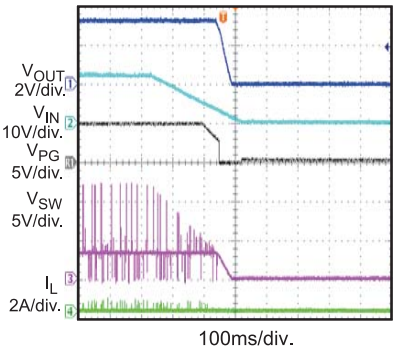
Start-Up through Input Voltage
I_{OUT} = 0A



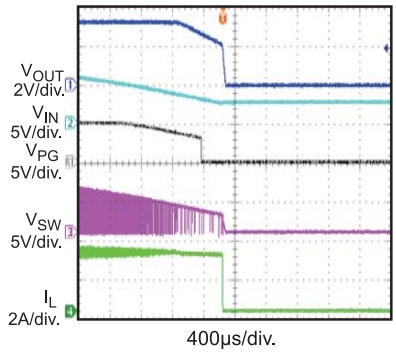
Start-Up through Input Voltage
I_{OUT} = 3A



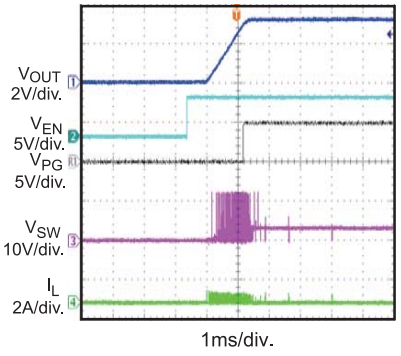
Shutdown through Input Voltage
I_{OUT} = 0A



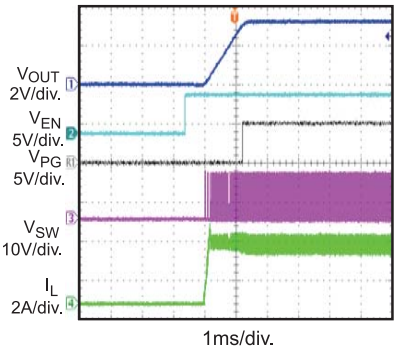
Shutdown through Input Voltage
I_{OUT} = 3A



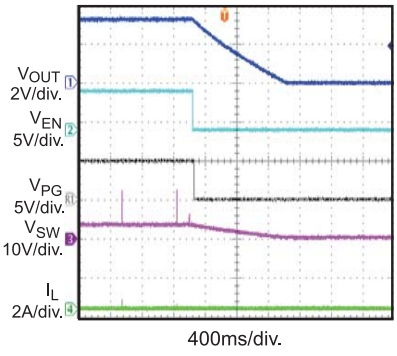
Start-Up through EN
I_{OUT} = 0A



Start-Up through EN
I_{OUT} = 3A



Shutdown through EN
I_{OUT} = 0A

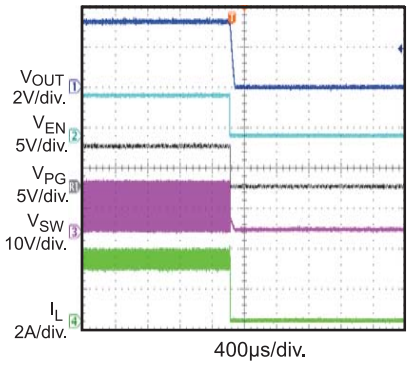


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

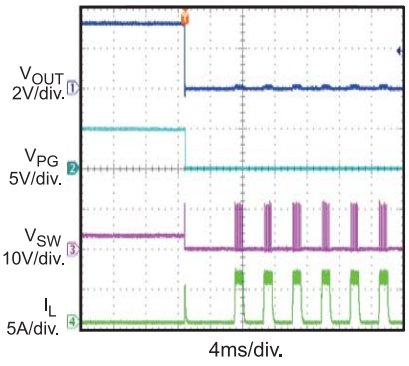
Performance waveforms are tested on the evaluation board of the Design Example section. V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, F_{SW} = 500kHz, C_{SS} = 12nF, T_A = 25°C, BIAS is connected to GND, unless otherwise noted.

Shutdown through EN

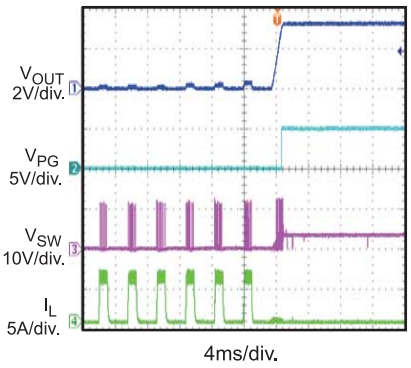
I_{OUT} = 3A



Short Circuit Protection Entry

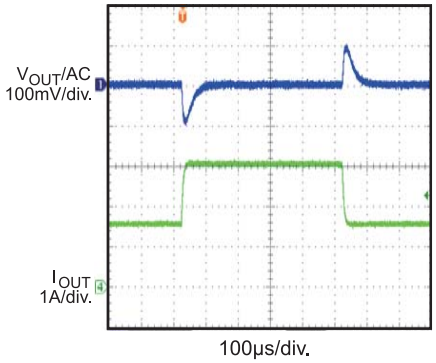


Short Circuit Protection Recovery



Load Transient Response

I_{OUT} = 1.5A to 3A



BLOCK DIAGRAM

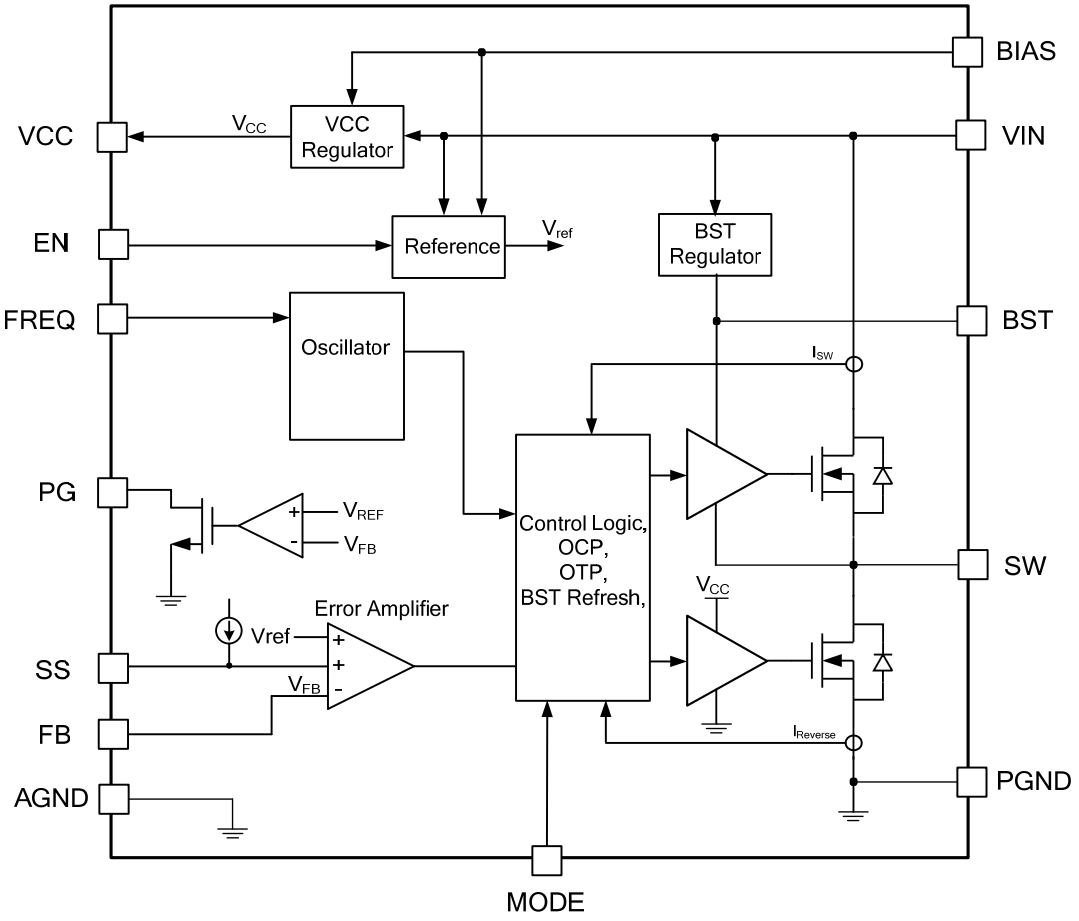


Figure 1: Functional Block Diagram

OPERATION

The MP2263 is a synchronous, step-down, switching regulator with integrated, internal, high-side and low-side power MOSFETs. It provides 3A of highly efficient output current with current-mode control. The MP2263 has a wide input voltage range, programmable 350kHz to 2.5MHz switching frequency, external soft start, and current limit. Its very low operational quiescent current makes it suitable for battery-powered applications.

PWM Control

At moderate-to-high output currents, the MP2263 operates in a fixed-frequency, peak-current-control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. At the rising edge of the clock, the high-side power MOSFET (HS-FET) turns on and remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the high-side power switch is off, the low-side MOSFET (LS-FET) turns on and remains on until the next cycle begins. If the current in the HS-FET does not reach the COMP-set current value in one PWM period, the HS-FET remains on, saving a turn-off operation.

Advanced Asynchronous Mode (AAM)

The MP2263 employs advanced asynchronous mode (AAM) functionality to optimize efficiency during light-load or no-load conditions. AAM is selectable. AAM is enabled by connecting MODE to a low level or floating MODE. AAM is disabled by connecting MODE to a high level.

When AAM is enabled, the MP2263 first enters non-synchronous operation for as long as the inductor current approaches zero at light load. If the load is further decreased or is at no load, V_{COMP} is below V_{AAM}, and the MP2263 enters AAM or sleep mode, which consumes very low quiescent current to improve light-load efficiency further.

In AAM, the internal clock is reset whenever V_{COMP} crosses over V_{AAM}. The crossover time is taken as the benchmark for the next clock. When the load increases, and the DC value of V_{COMP} is higher than V_{AAM}, the operation mode is DCM or CCM, which have a constant switching frequency.

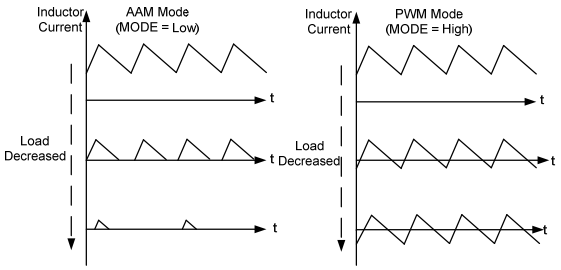


Figure 2: AAM and PWM Mode

The MP2263 has a mode selection function. Pull MODE low or float MODE to set auto PFM/PWM mode; pull MODE to VCC to set forced PWM mode. MODE is pulled down internally. Select MODE before the part starts up.

Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage with the internal reference (typically 0.8V) and outputs a current proportional to the difference between the two. This output current is then used to charge the internal compensation network to form V_{COMP}, which is used to control the power MOSFET current.

Bias and VCC Regulator

Most of the internal circuitries are powered by the internal regulator. The MP2263 has two internal regulators (see Figure 3). The regulator LDO1 takes the VIN input and operates in the full VIN range. When VIN is greater than 5.0V, the output of the regulator is in full regulation, and VCC is 5V. When VIN is lower than 5V, the output degrades.

Another regulator, LDO2, is powered by BIAS. Connect BIAS to an external power source. Keep the BIAS voltage higher than 4.8V. VCC and the internal circuit are powered by BIAS. When V_{BIAS} is greater than 5V, the output of the regulator is in full regulation, and VCC is 5V. When V_{BIAS} is lower than 5V, the output degrades.

LDO2 is enabled when V_{BIAS} > 4.8V. Once LDO2 is enabled, LDO1 is disabled. For a 5V output application, connect BIAS to V_{OUT} for improved efficiency. The diode (D1) between BIAS and the internal circuit is used for current reverse blocking. Since LDO1 has no reverse block function, V_{BIAS} must be less than VIN. Connect BIAS to GND if BIAS is not used.

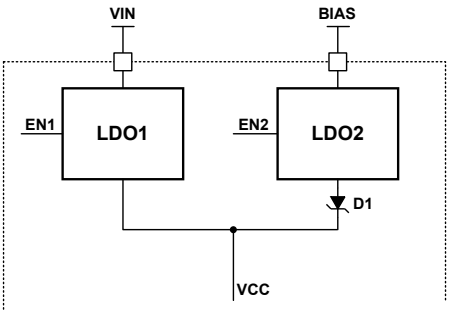


Figure 3: VCC Regulator

Bootstrap Charging

The bootstrap capacitor is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between the BST and SW nodes is lower than its regulation, a PMOS connected from VCC to BST is turned on. The charging current path is from VCC to BST to SW.

When the HS-FET is on, VIN is about equal to SW, so the bootstrap capacitor cannot be charged.

At higher duty cycle operation conditions, the time period available to the bootstrap charging is less, so the bootstrap capacitor may not be charged sufficiently. In case the internal circuit does not have sufficient voltage or time to charge the bootstrap capacitor, extra external circuitry can be used to ensure that the bootstrap voltage is in the normal operation region.

Low-Dropout Operation

To improve dropout, the MP2263 is designed to operate at almost 100% duty cycle for as long as the BST to SW voltage is greater than 2.5V. When the voltage from BST to SW drops below 2.5V, the HS-FET is turned off using an UVLO circuit, which allows the LS-FET to conduct and refresh the charge on the BST capacitor. In DCM or PSM, the LS-FET is forced on to refresh the BST voltage.

Since the supply current sourced from the BST capacitor is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor. Therefore, the effective duty cycle of the switching regulator is high.

The effective duty cycle during dropout of the regulator is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, low-side diode and printed circuit board resistance.

Enable Control (EN)

EN is a digital control pin that turns the regulator on and off.

EN can be enabled by an external logic H/L signal. When EN is pulled below the threshold voltage, the chip enters the lowest shutdown current mode. Forcing EN above the EN threshold voltage turns on the MP2263.

For the programmable VIN under-voltage lockout (UVLO), with a high enough VIN, the MP2263 can be enabled and disabled by EN (see Figure 4). This circuit can generate a programmable VIN UVLO and hysteresis.

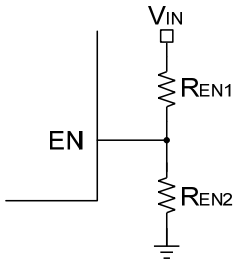


Figure 4: Enable Divider Circuit

Frequency Programmable

The MP2263 oscillating frequency is programmed by an external resistor (R_{freq}) from the FREQ pin to ground.

The approximate value of R_{freq} can be calculated with Equation (1):

$$R_{freq}(k\Omega) = \frac{86500}{f_s(kHz)} - 6.5 \quad (1)$$

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up.

When the soft-start period begins, an internal current source begins charging the external soft-start capacitor. After the soft-start voltage charges higher than the internal offset voltage (typically 600mV), V_{OUT} starts up.

When (SS - V_{offest})/1.125 is lower than the internal reference (REF), the error amplifier uses (SS - V_{offest})/1.125 as the reference. When (SS - V_{offest})/1.125 is higher than REF, REF regains control.

C_{SS} can be calculated with Equation (2):

$$Css(nF) = \frac{Tss(ms) \times Iss(\mu A)}{1.125 \times V_{ref}(V)} \quad (2)$$

The minimum T_{SS} is 800μs, typically.

Pre-Bias Start-Up

The MP2263 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged. The voltage on the soft-start capacitor is also charged. If the BST voltage exceeds its rising threshold voltage, and the soft-start capacitor voltage exceeds 1.125*V_{FB}+V_{offest}, the MP2263 begins working normally.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from running away thermally. When the silicon die temperature is higher than its upper threshold, the power MOSFETs shut down. When the temperature is lower than its lower threshold, thermal shutdown is removed, and the chip is enabled again.

Current Comparator and Current Limit

The power MOSFET current is sensed accurately via a current sense MOSFET. This current is fed to the high-speed current comparator for current-mode control purposes. The current comparator uses this sensed current as one of its inputs. When the HS-FET is turned on, the comparator is first blanked until the end of the turn-on transition to avoid noise. The comparator then compares the power switch current with V_{COMP}. When the sensed current is higher than V_{COMP}, the comparator outputs low to turn off the HS-FET. The maximum current of the internal power MOSFET is limited cycle-by-cycle internally.

Hiccup Protection

When the output is shorted to ground, causing the output voltage to drop below 70% of its nominal output, the IC shuts down momentarily and begins discharging the soft-start capacitor. The IC restarts with a full soft start when the soft-start capacitor is fully discharged. This hiccup process is repeated until the fault is removed.

Start-Up and Shutdown

If both VIN and EN are higher than their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltages and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the rest of the circuitries.

When the internal supply rail is up, an internal timer holds the power MOSFET off for about 50μs to blank the start-up glitches. When the soft-start block is enabled, the SS output is held low to ensure that the rest of the circuitries are ready before slowly ramping up.

Three events can shut down the chip: EN low, VIN low, and thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Power Good Output

The MP2263 has an open-drain pin as the power good indicator (PG). PG can indicate under voltage (UV) and over voltage (OV). Pull PG up to VCC through a 100kΩ resistor. In the UV condition, when V_{FB} exceeds 90% of V_{REF}, PG goes high. If V_{FB} drops below 84% of V_{REF}, an internal MOSFET pulls PG down to ground. In the OV condition, when V_{FB} exceeds 118% of V_{REF}, PG goes low. If V_{FB} goes below 110% of V_{REF}, PG goes high.

APPLICATION INFORMATION

Setting the Output

The external resistor divider is used to set the output voltage (see the Typical Application on page 1). Refer to Table 1 to choose R1. R2 can then be calculated with Equation (3):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1} \quad (3)$$

The feedback network is highly recommended (see Figure 5).

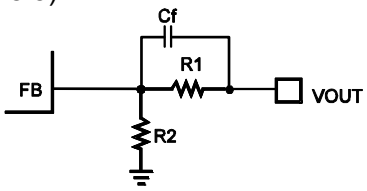


Figure 5: Feedback Network

Table 1 lists the recommended feedback network parameters for common output voltages.

Table 1: Recommended Parameters for Common Output Voltages(7)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_f (pF)
1.05	470	1500	5.6
1.2	750	1500	5.6
1.8	1000	806	5.6
2.5	1000	470	5.6
3.3	1000	324	5.6
5	1000	191	5.6

NOTE:

7) The recommended parameters are based on a 500kHz switching frequency. A different input voltage, output inductor value, or output capacitor value may affect the selection of R1, R2, and C_f. For additional component parameters, please refer to the Typical Application Circuits on pages 16 and 17.

Selecting the Inductor

For most applications, use a 1μH to 22μH inductor with a DC current rating at least 25% higher than the maximum load current. For the highest efficiency, use an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be derived from Equation (4):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (4)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (5):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (5)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current while maintaining the DC input voltage. Use low ESR capacitors for optimum performance. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, use two 10μF capacitors. Since C1 absorbs the input switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated with Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (7):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (7)$$

For simplification, choose an input capacitor that has an RMS current rating greater than half the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality, ceramic capacitor (e.g.: 0.1μF) should be placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output

voltage ripple low. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (9)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor affect the stability of the regulation system. The MP2263 can be optimized for a wide range of capacitance and ESR values.

PCB Layout Guidelines [8]

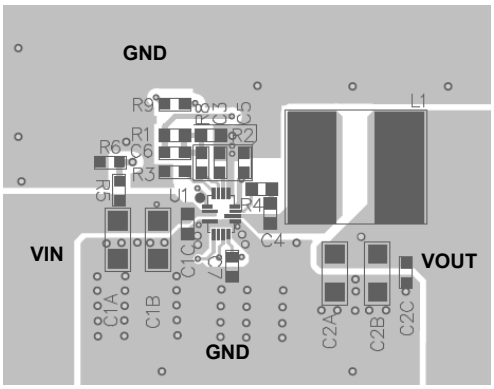
Efficient PCB layout is critical for stable operation. For best results, refer to Figure 6 and follow the guidelines below.

1) Keep the connection of the input ground and GND as short and wide as possible.
2) Keep the connection of the input capacitor and IN as short and wide as possible.
3) Ensure all feedback connections are short and direct.
4) Place the feedback resistors and compensation components as close to the chip as possible.
5) Route SW away from sensitive analog areas, such as FB.

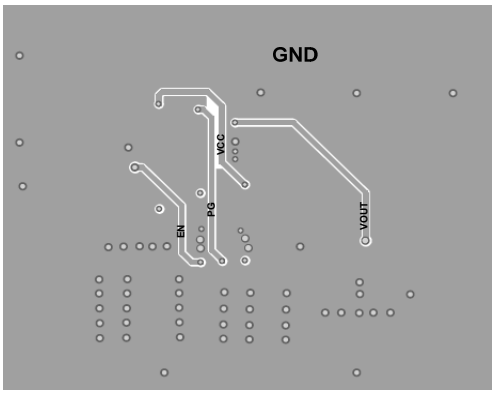
NOTE:

8) The recommended layout is based on Figure 8.

To achieve better performance, use four-layer boards. Figure 6 shows the top and bottom layers (Inner 1 and Inner 2 are both GND).



Top Layer



Bottom Layer

Figure 6: Sample PCB Layout

Design Example

Table 2 shows a design example following the application guidelines for the specifications below:

Table 2: Design Example

V_{IN}	12V
V_{OUT}	3.3V
Io	3A

The detailed application schematic is shown in Figure 8. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For additional device applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUITS(9)

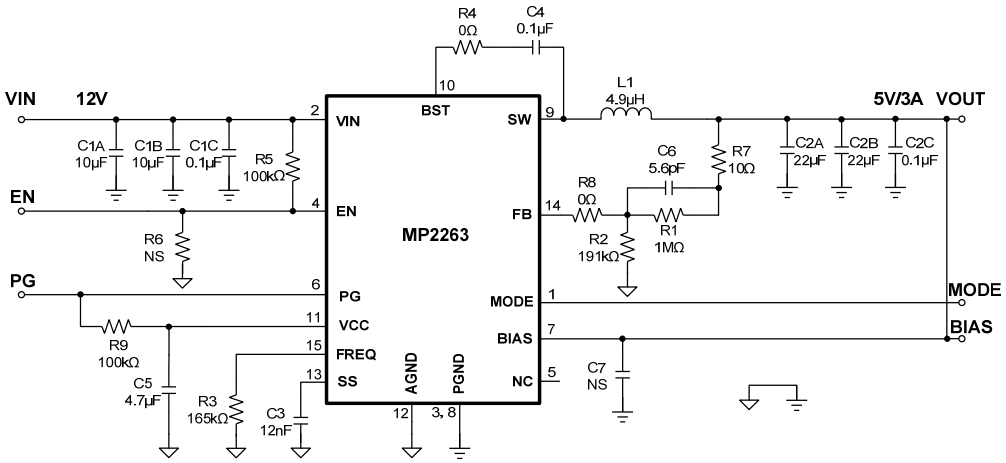


Figure 7: V_{IN} = 12V, V_{OUT} = 5V

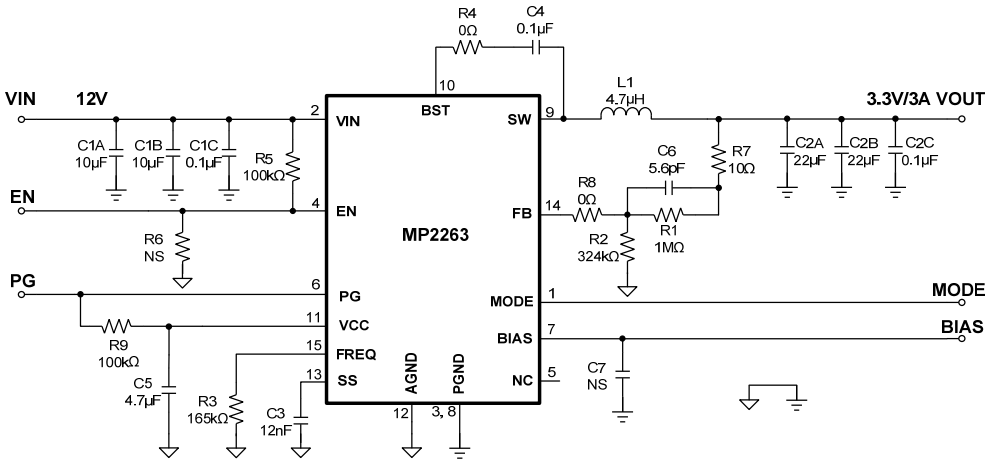


Figure 8: V_{IN} = 12V, V_{OUT} = 3.3V

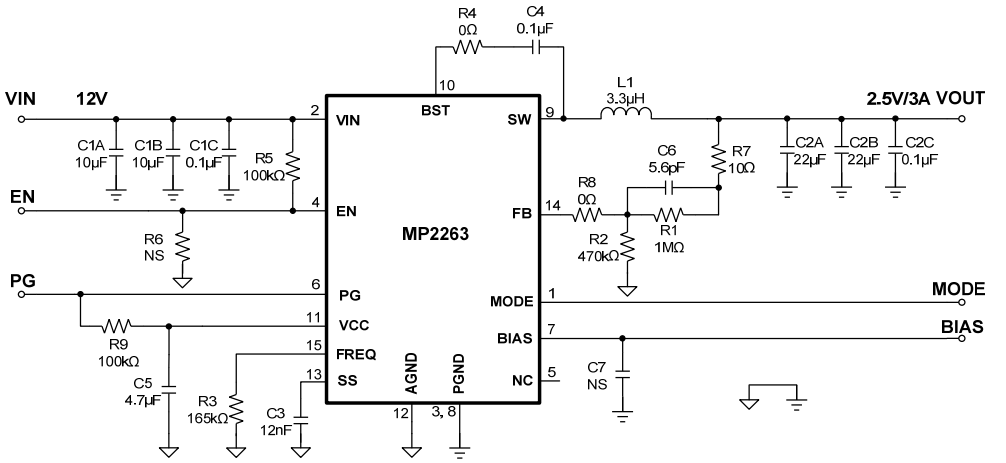


Figure 9: V_{IN} = 12V, V_{OUT} = 2.5V

TYPICAL APPLICATION CIRCUITS *(continued)*

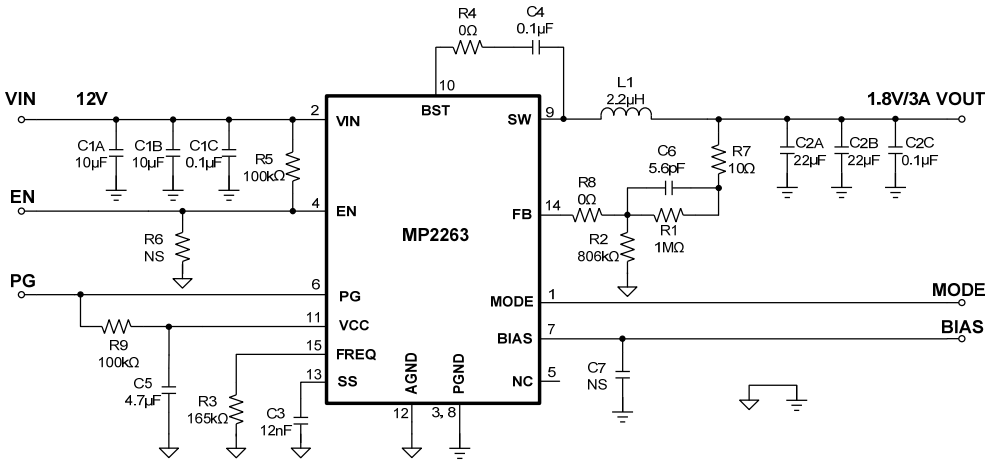


Figure 10: V_{IN} = 12V, V_{OUT} = 1.8V

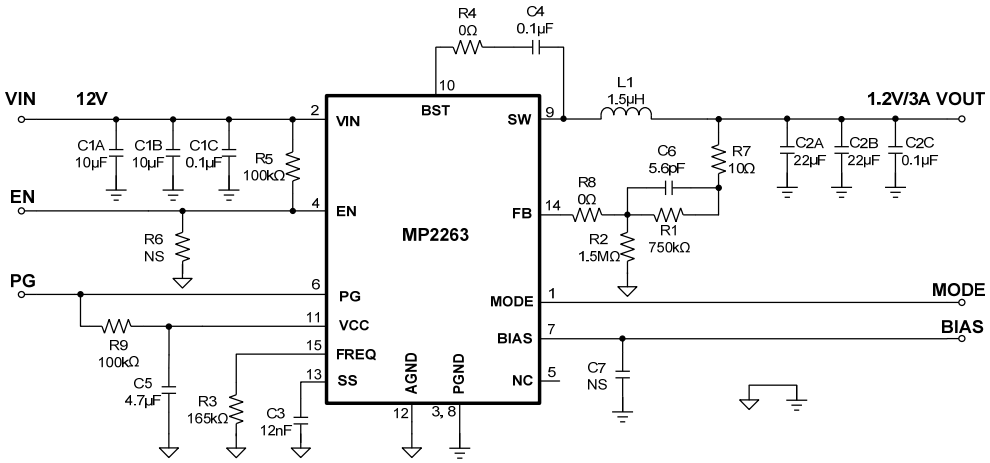


Figure 11: V_{IN} = 12V, V_{OUT} = 1.2V

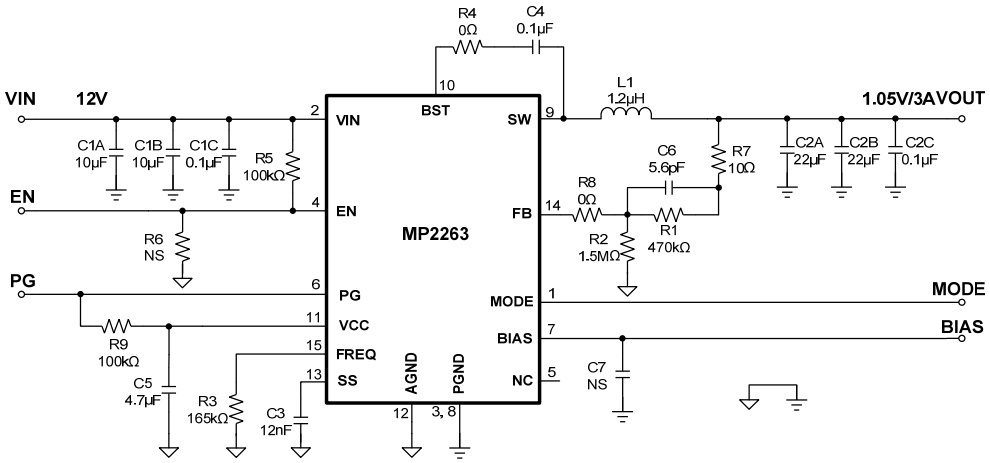


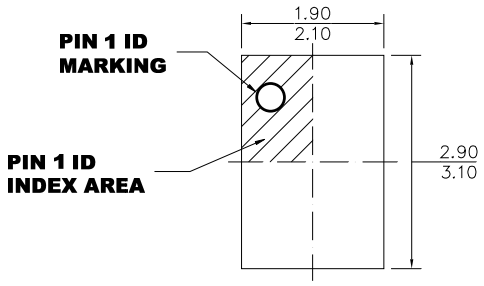
Figure 12: V_{IN} = 12V, V_{OUT} = 1.05V

NOTE:

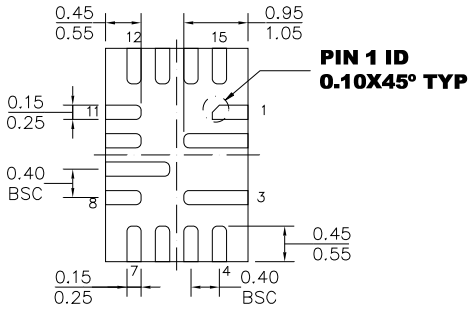
8) To use the bias function, connect BIAS to a power source higher than 4.8V. If the bias function is not used, connect BIAS to GND.

PACKAGE INFORMATION

QFN-15 (2mmx3mm)

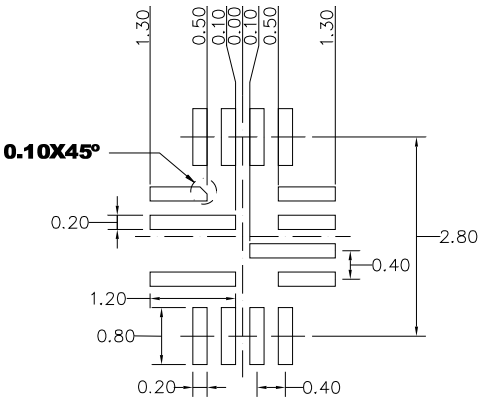


TOP VIEW



BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.