

[v2,00/17] RISC-V: support vector extension

11140355	mbox (/cover/11140355/mbox/)	series (/series/172559/mbox/)
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- Message ID** 1568183141-67641-1-git-send-email-zhiwei_liu@c-sky.com
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Message

LIU Zhiwei (</project/qemu-devel/list/?submitter=187957>)

Sept. 11, 2019, 6:25 a.m. UTC

Features:

- * support specification riscv-v-spec-0.7.1(<https://content.riscv.org/wp-content/uploads/2019/>)
- * support basic vector extension.
- * support Zvlsseg.
- * support Zvamo.
- * not support Zvediv as it is changing.
- * fixed VLEN 128bit.
- * fixed SLEN 128bit.
- * ELEN support 8bit, 16bit, 32bit, 64bit.

Todo:

- * support VLEN configure from qemu command line.
- * move check code from execution-time to translation-time

Changelog:

V2

- * use float16_compare{quiet}
- * only use GETPC() in outer most helper
- * add ctx.ext_v Property

LIU Zhiwei (17):

- RISC-V: add vfp field in CPURISCVState
- RISC-V: turn on vector extension from command line by cfg.ext_v Property
- RISC-V: support vector extension csr
- RISC-V: add vector extension configure instruction
- RISC-V: add vector extension load and store instructions
- RISC-V: add vector extension fault-only-first implementation
- RISC-V: add vector extension atomic instructions
- RISC-V: add vector extension integer instructions part1, add/sub/adc/sbc
- RISC-V: add vector extension integer instructions part2, bit/shift
- RISC-V: add vector extension integer instructions part3, cmp/min/max
- RISC-V: add vector extension integer instructions part4, mul/div/merge
- RISC-V: add vector extension fixed point instructions
- RISC-V: add vector extension float instruction part1, add/sub/mul/div
- RISC-V: add vector extension float instructions part2, sqrt/cmp/cvt/others
- RISC-V: add vector extension reduction instructions
- RISC-V: add vector extension mask instructions
- RISC-V: add vector extension premutation instructions

```
linux-user/riscv/cpu_loop.c      |      7 +
target/riscv/Makefile.objs       |      2 +-
target/riscv/cpu.c               |      6 +-
target/riscv/cpu.h               |     30 +
target/riscv/cpu_bits.h          |     15 +
target/riscv/cpu_helper.c        |      7 +
target/riscv/csr.c               |     65 +-
target/riscv/helper.h            |    358 +
target/riscv/insn32.decode       |    373 +
target/riscv/insn_trans/trans_rvv.inc.c |    490 +
target/riscv/translate.c         |      1 +
target/riscv/vector_helper.c     |  25701 ++++++
12 files changed, 27049 insertions(+), 6 deletions(-)
create mode 100644 target/riscv/insn_trans/trans_rvv.inc.c
create mode 100644 target/riscv/vector_helper.c
```

Comments

Aleksandar Markovic (/project/qemu-devel/list/?submitter=183567)

Sept. 11, 2019, 7 a.m. UTC | #1 (/comment/22875851/)

11.09.2019. 08.35, "liuzhiwei" <zhiwei_liu@c-sky.com> је написао/ла:
 >
 > Features:
 > * support specification riscv-v-spec-0.7.1(
https://content.riscv.org/wp-content/uploads/2019/06/17.40-Vector_RISCV-20190611-Vectors.pdf
 >).

Hi, Zhivei.

The linked document is a presentation, outlining general concepts of the instruction set in question, which is certainly useful and nice to have, but, for review process, we need *specifications* (especially given that they are in draft phase, and therefore "moving target"). Please provide such link.

I also noticed lack of commit messages, and was really disappointed by that. It looks to me you did not honor in entirety our guidelines for submitting patches.

Yours,
 Aleksandar

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> linux-user/riscv/cpu_loop.c          |      7 +
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> target/riscv/cpu.c                   |      6 +-
> target/riscv/cpu.h                   |     30 +
> target/riscv/cpu_bits.h              |     15 +
> target/riscv/cpu_helper.c            |       7 +
> target/riscv/csr.c                   |      65 +-
> target/riscv/float.h                 |     258 +
```

2020/4/20

[v2,00/17] RISC-V: support vector extension - Patchwork

```
> target/riscv/helper.h | 358 +
> target/riscv/insn32.decode | 373 +
> target/riscv/insn_trans/trans_rvv.inc.c | 490 +
> target/riscv/translate.c | 1 +
> target/riscv/vector_helper.c | 25701
++++
> 12 files changed, 27049 insertions(+), 6 deletions(-)
> create mode 100644 target/riscv/insn_trans/trans_rvv.inc.c
> create mode 100644 target/riscv/vector_helper.c
>
> --
> 2.7.4
>
>
```

Palmer Dabbelt (/project/qemu-devel/list/?submitter=177321)

Sept. 14, 2019, 12:59 p.m. UTC | #2 (/comment/22882027/)

On Wed, 11 Sep 2019 00:00:56 PDT (-0700), aleksandar.m.mail@gmail.com wrote:
 > 11.09.2019. 08.35, "liuzhiwei" <zhiwei_liu@c-sky.com> je написао/ла:
 >>
 >> Features:
 >> * support specification riscv-v-spec-0.7.1(
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 > instruction set in question, which is certainly useful and nice to have,
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 > they are in draft phase, and therefore "moving target"). Please provide
 > such link.

Here's the V spec repository

<https://github.com/riscv/riscv-v-spec>

and the exact 0.7.1 specification PDF

<https://github.com/riscv/riscv-v-spec/releases/download/0.7.1/riscv-v-spec-0.7.1.pdf>

In RISC-V land this constitutes an official draft -- there's a whole process for getting a specification ratified, but that isn't done for these draft specifications. The RISC-V QEMU maintainers agree that we'll take implementations of drafts as long as there's a concrete definition we can point at, like this one.

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 > that. It looks to me you did not honor in entirety our guidelines for
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 > Yours,
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>>

```

patchwork (<http://jk.ozlabs.org/projects/patchwork/>) patch tracking system | version | about patchwork (/about/)