Topic 7.4

ASIC Design Flow IV

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Deadlines

Summary of Deadlines for the rest of the semester			
Category	**Items**	**Due date/time**	**Type**
Assignment	Sign up for SoC product review assignment here: https://sjtu.feishu.cn/sheets/shtcnJVd2fKDs4fLrs3NI7XVElP	**Nov. 17th**	Individual
Project	Indicate your intention for the target application (from the application pool) and planned methodology https://sjtu.feishu.cn/sheets/shtcnBP61XqeTugdwWf6zDHQfPb	**Nov. 17th**	Team
Assignment	HW#4	**Nov. 18th**	Individual
Lab	Lab#6	**Nov. 21st**	Team
Project	progress update (oral)	**Dec. 3rd Lab Session**	Team
Assignment	SoC Product Manual Review Slides	**Dec. 9th 13:00**	Individual
Assignment	Literature Search & Review Assignment Slides	**Dec. 9th 13:00**	Individual
Assignment	SoC Product Manual Review & Literature Search Review Presentation	**Dec. 9th in class**	Individual
Project	Project Presentation	**Dec. 10th Lab Session**	Team
Project	Project Submission on Canvas	**Dec. 15th**	Team
Exam	Final Exam	**Dec. 16th in class**	Individual

T7 learning goals

- How to design a Chip (SoC) from concept to silicon?
  - **Full design flow from RTL to Layout**
  - **How to make decisions at each step**

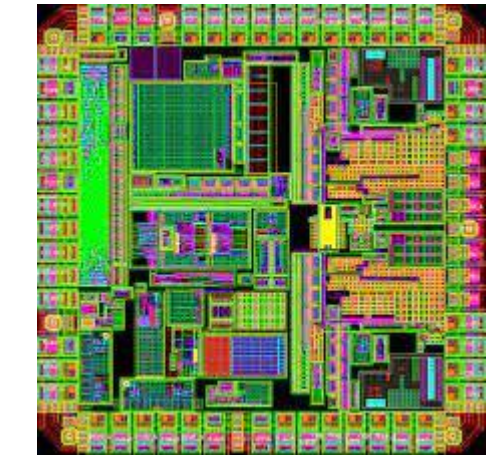
```
module PE (clock, R, S1, S2, S1S2mux, newDist, Accumulate, Rpipe);
input clock;
input [7:0] R, S1, S2;// memory inputs
input S1S2mux, newDist;// control inputs
output [7:0] Accumulate, Rpipe;
reg [7:0] Accumulate, AccumulateIn, Difference, Rpipe;
reg       Carry;

always @(posedge clock) Rpipe <= R;
always @(posedge clock) Accumulate <= AccumulateIn;

always @(R or S1 or S2 or S1S2mux or newDist or Accumulate)
  begin  // capture behavior of logic
   difference = R - S1S2mux ? S1 : S2;
   if (difference < 0) difference = 0 - difference;
// absolute subtraction
    {Carry,AccumulateIn} = Accumulate + difference;
    if (Carry == 1) AccumulateIn = 8'hFF;// saturated
    if (newDist == 1) AccumulateIn = difference;
// starting new Distortion calculation
  end
endmodule
```

Motion Estimator Processing Element (PE).

RTL



Layout

Figure: Synopsys

Routing

Time to connect everything…

Physical Synthesis Flow

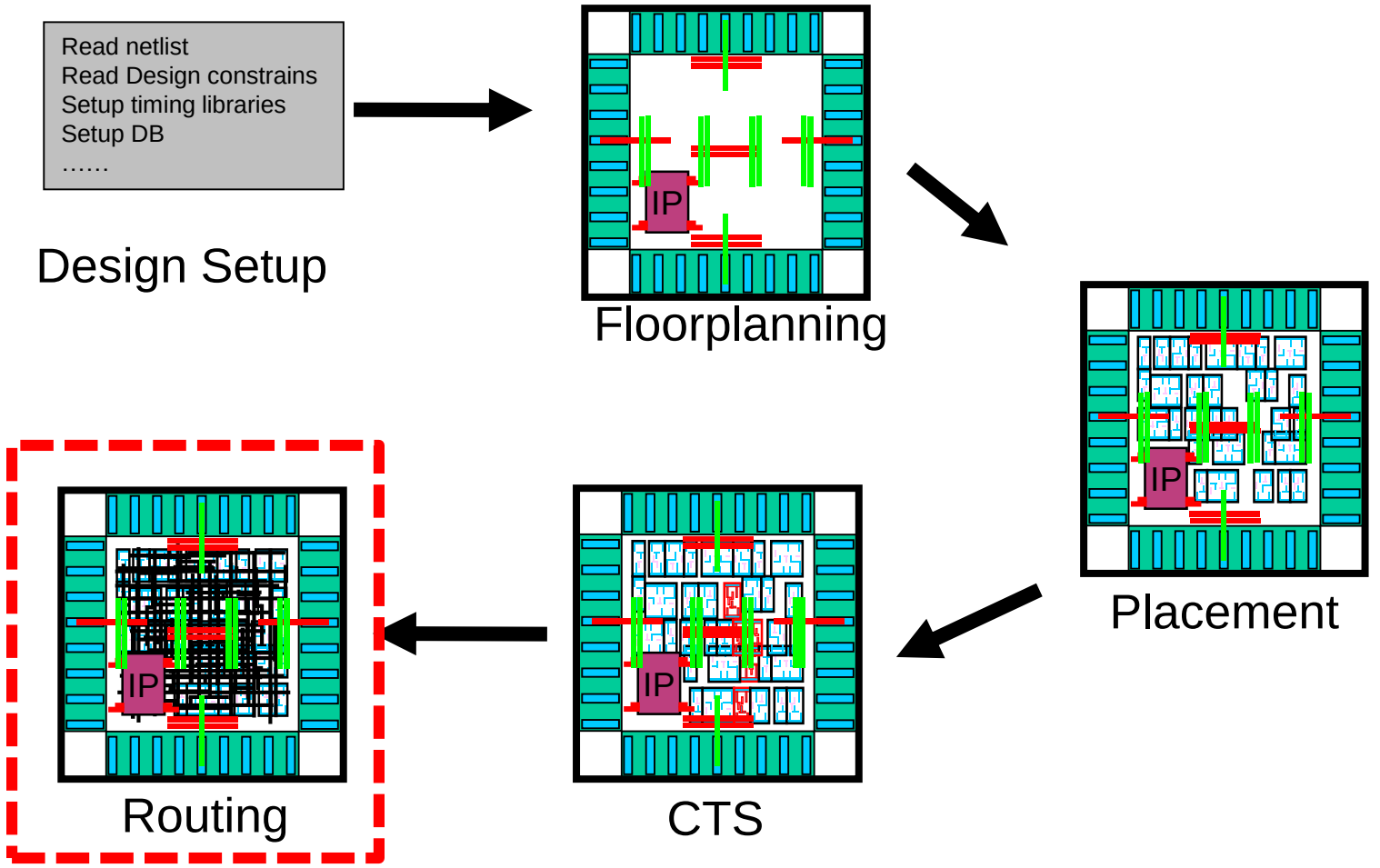
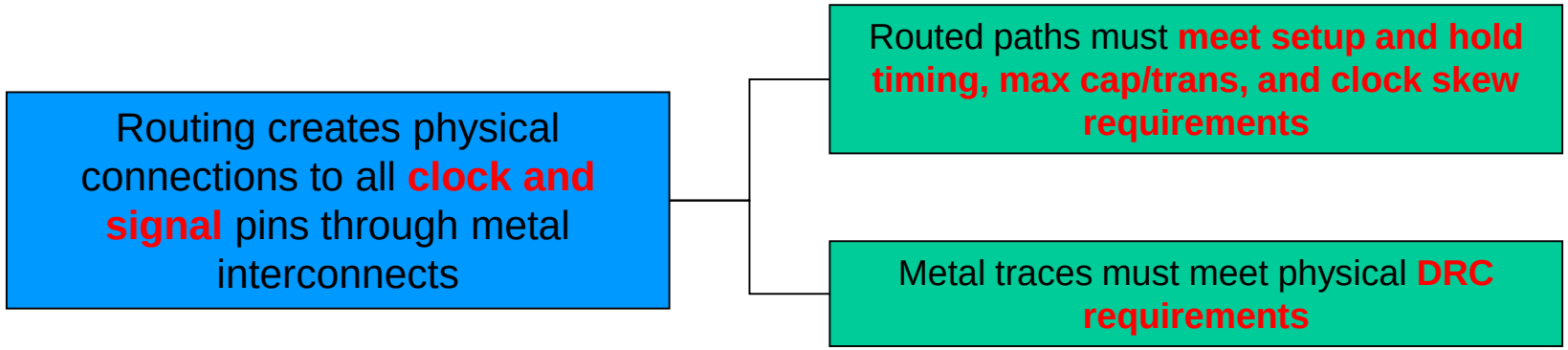


Figure: Synopsys

Routing Fundamentals: Goal

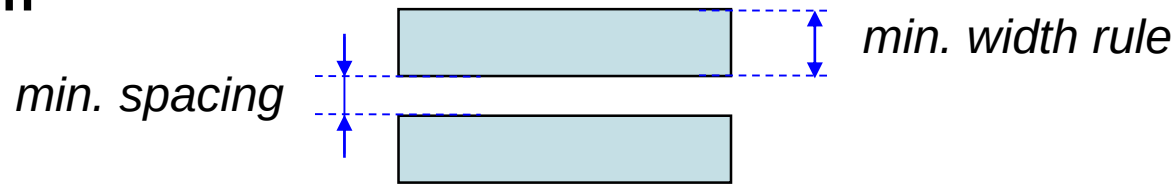


- Routing is the physical realization of all those interconnects between pins which are connected by an electrical circuit.
- Those interconnects provide both signal and clock/power circuit realization and meet physical (DRC) and electrical (timing, capacitance/transmission, clock, etc) requirements.
- Globally interconnects must provide minimal distortions from circuit operation by ideal connection lines to pass the operation through physical interconnects.

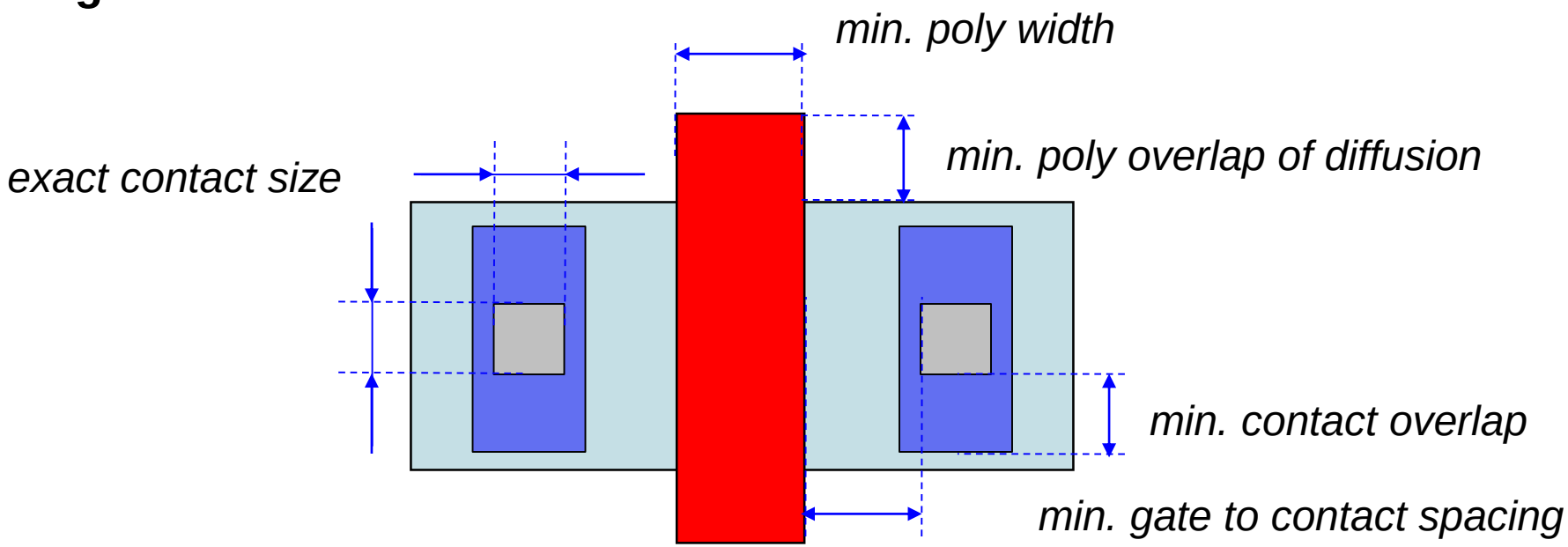
source: Synopsys

Design Rules Example

Resolution

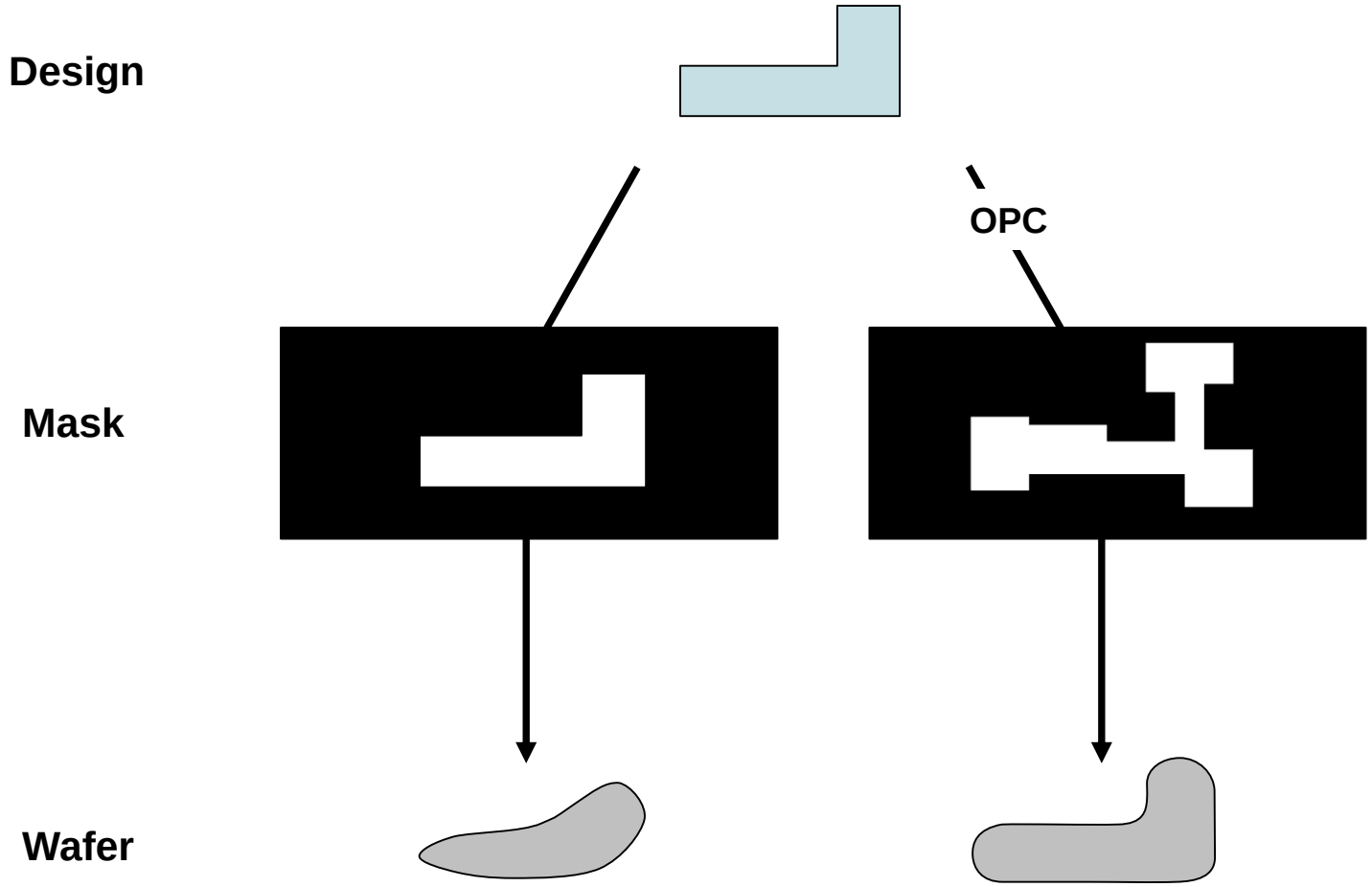


Alignment



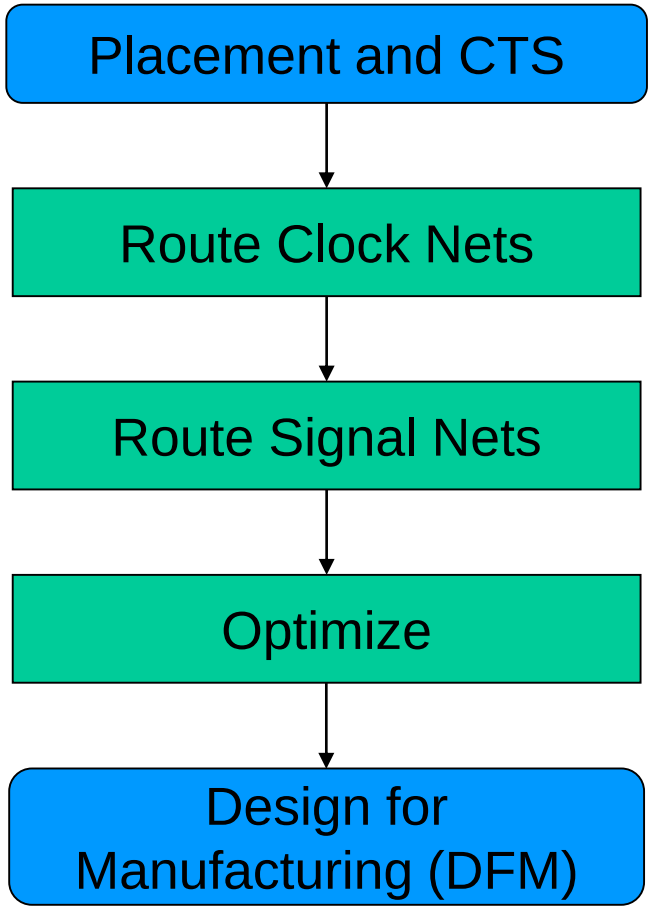
source: Synopsys

Optical Proximity Correction (OPC)



source: Synopsys

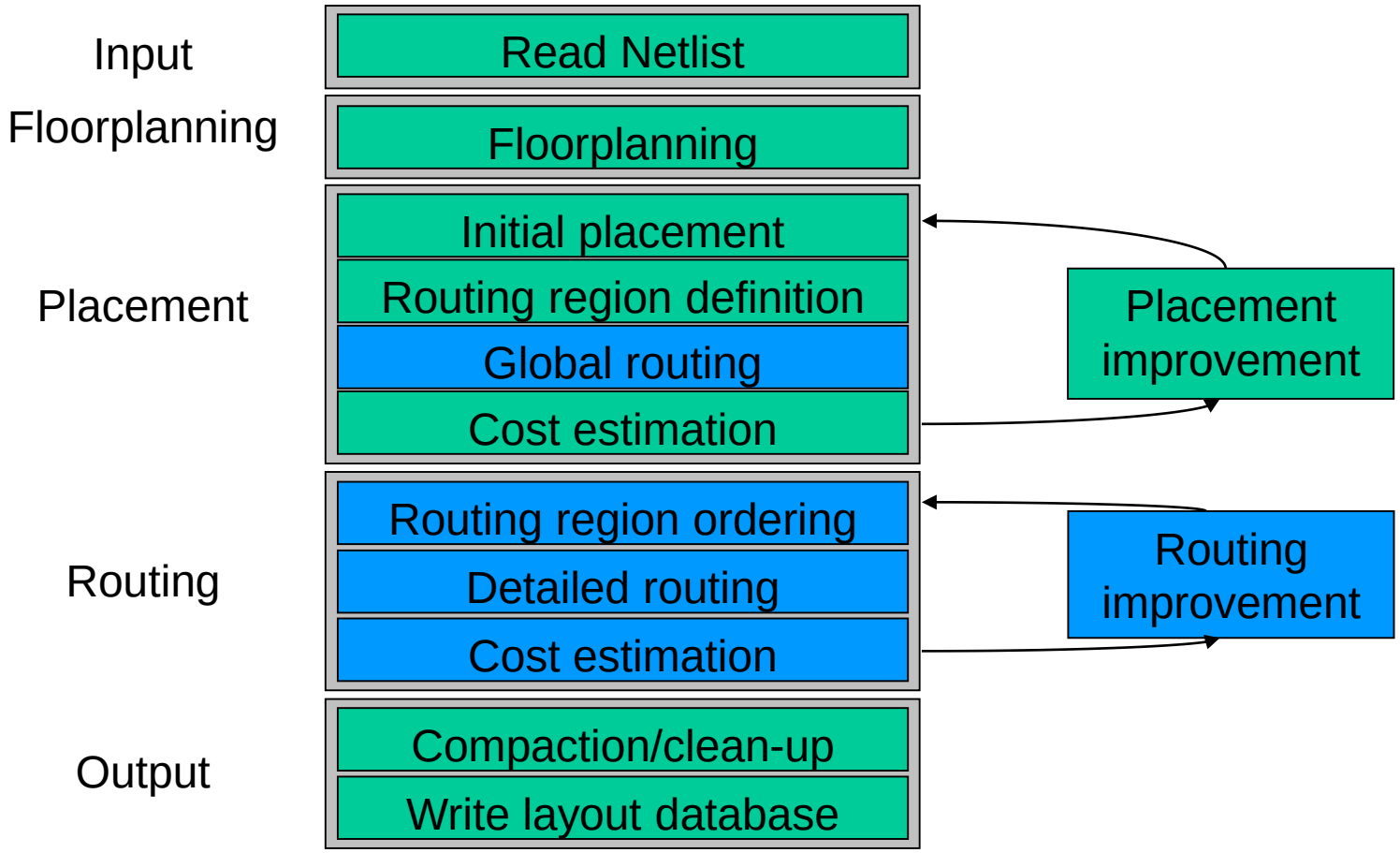
General Flow of Routing



- In all the design stages, preceding routing (floorplan, placement and CTS), provision of better conditions has been the most important for further routing. This is also called routability.
- Generally IC electrical circuits in the sense of functionality are divided into 3 groups – signal nets, clock nets and power nets.
- In the stage of routing, the physical design of clock nets and power nets are performed (illustrated in figure).

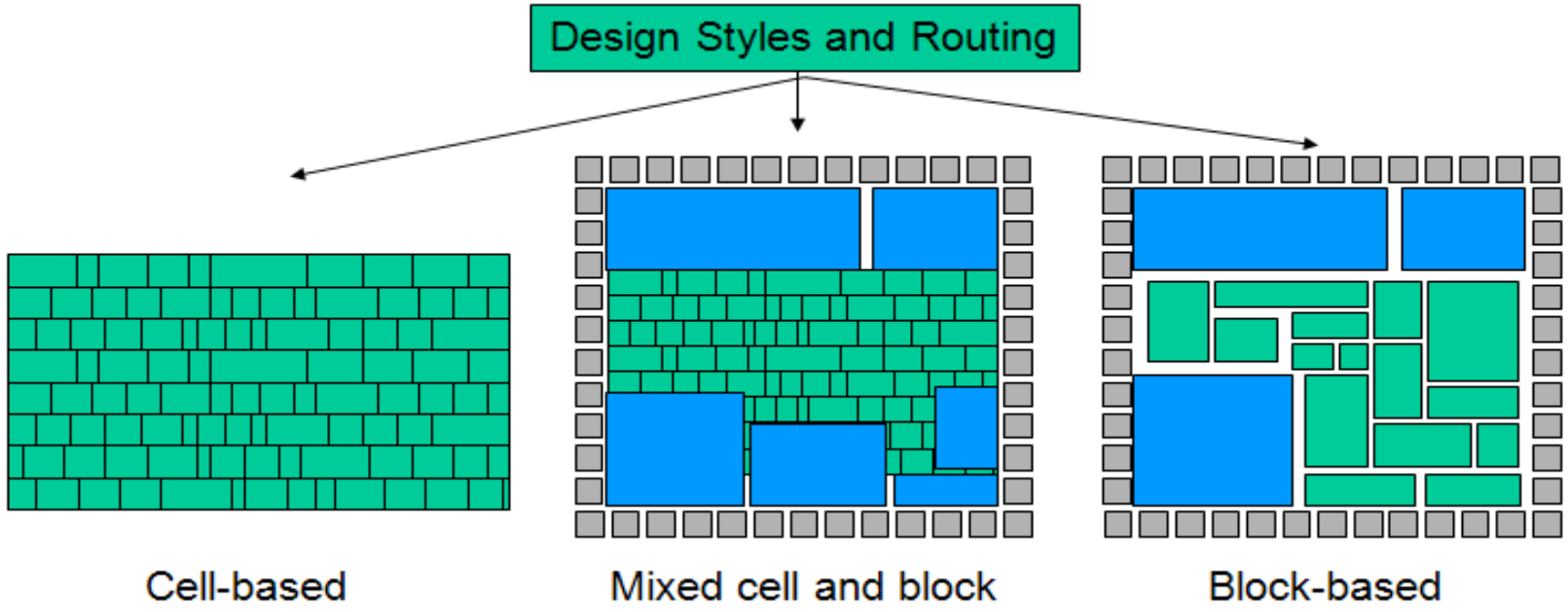
source: Synopsys

Routing Steps in Physical Synthesis



source: Synopsys

Design Styles and Routing



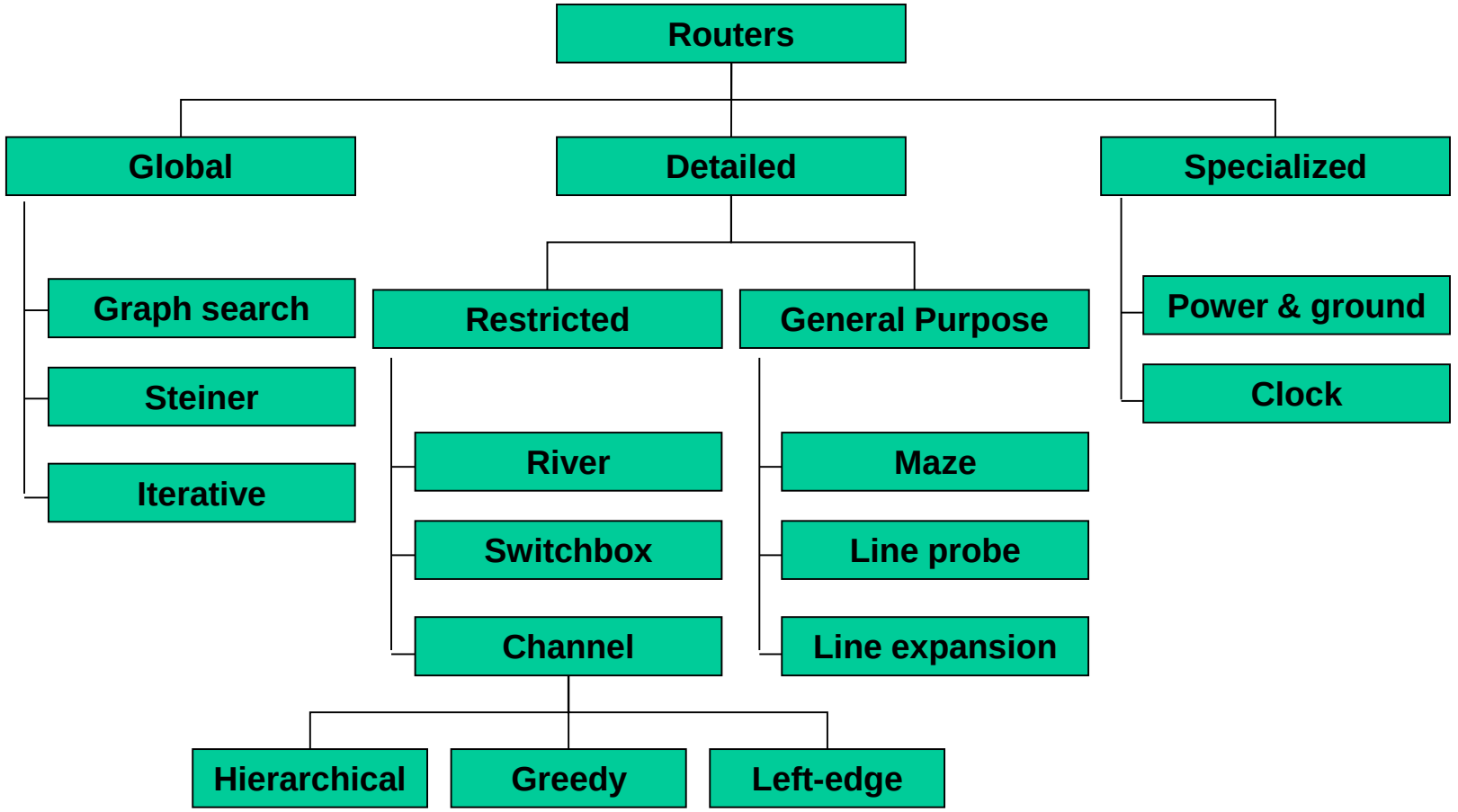
Routing provides interconnects between standard cells

Routing provides interconnects between IP blocks and standard cells

Routing provides interconnects between blocks

source: Synopsys

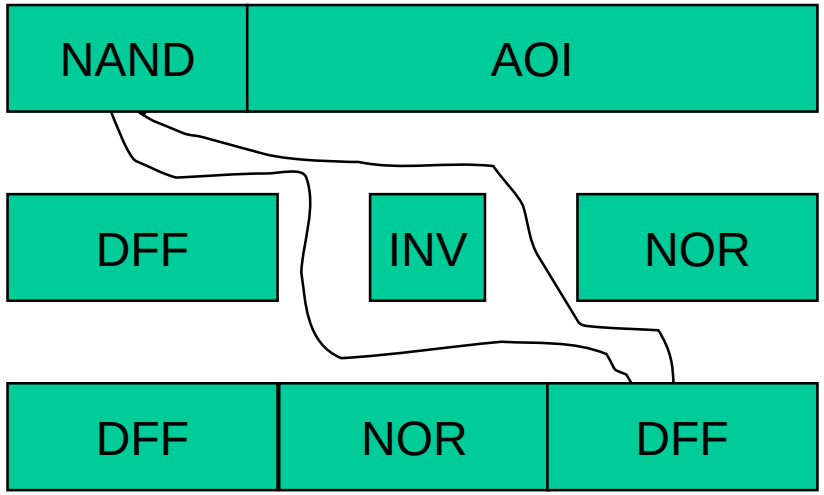
Classification of Routing Methods

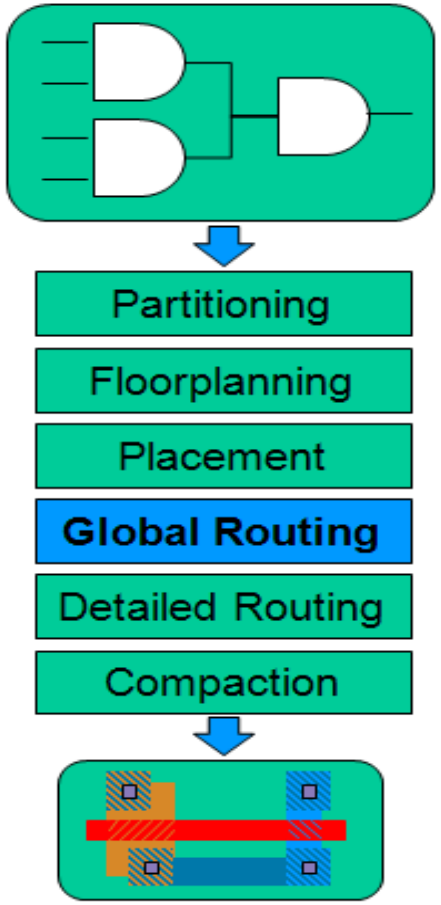


source: Synopsys

Global Routing

- Determining overall path of all routes
  - Picking channels to route through
- Seeking to reduce delay, channel widths

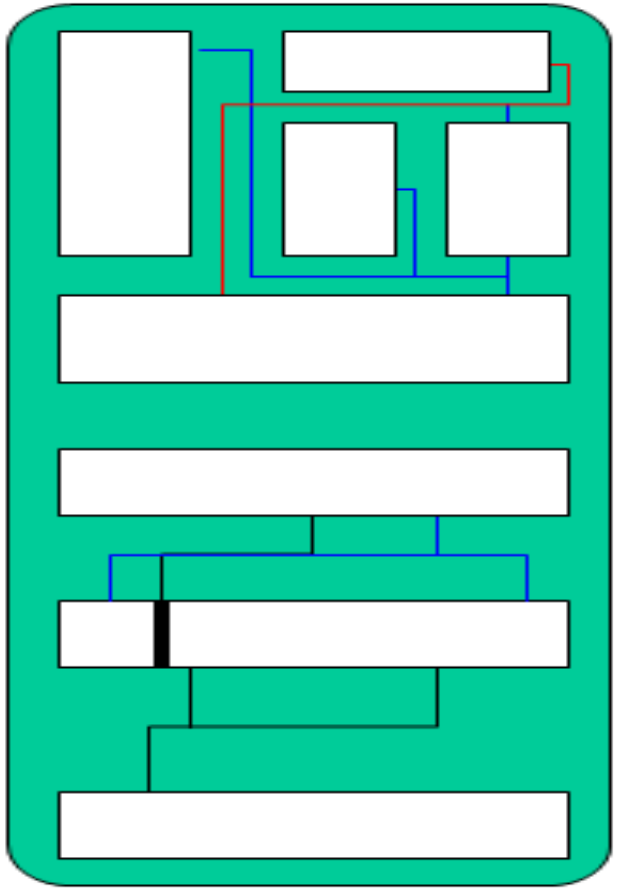




source: Synopsys

Global Routing : Inputs and Outputs

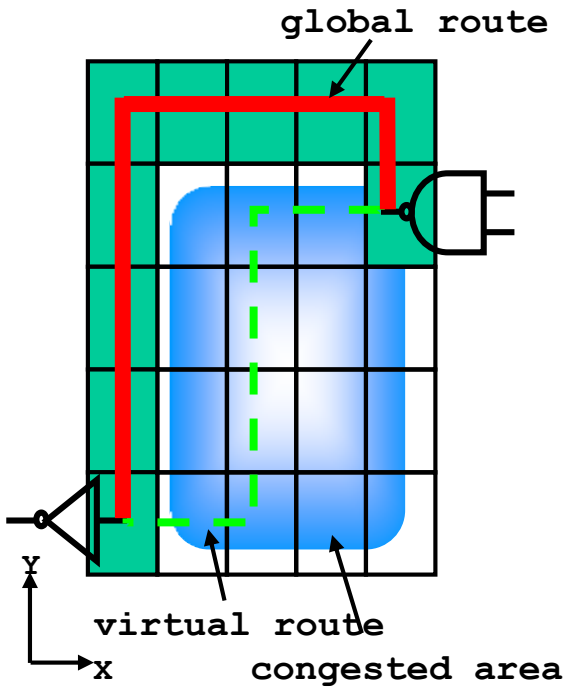
- Given
  - Placement of blocks/cells
  - Channel capacities
- Determine
  - Routing topology of each net
- Optimize
  - Maximum number of nets round
  - Minimum routing area
  - Minimum total wirelength



source: Synopsys

Route Operations: Global Route

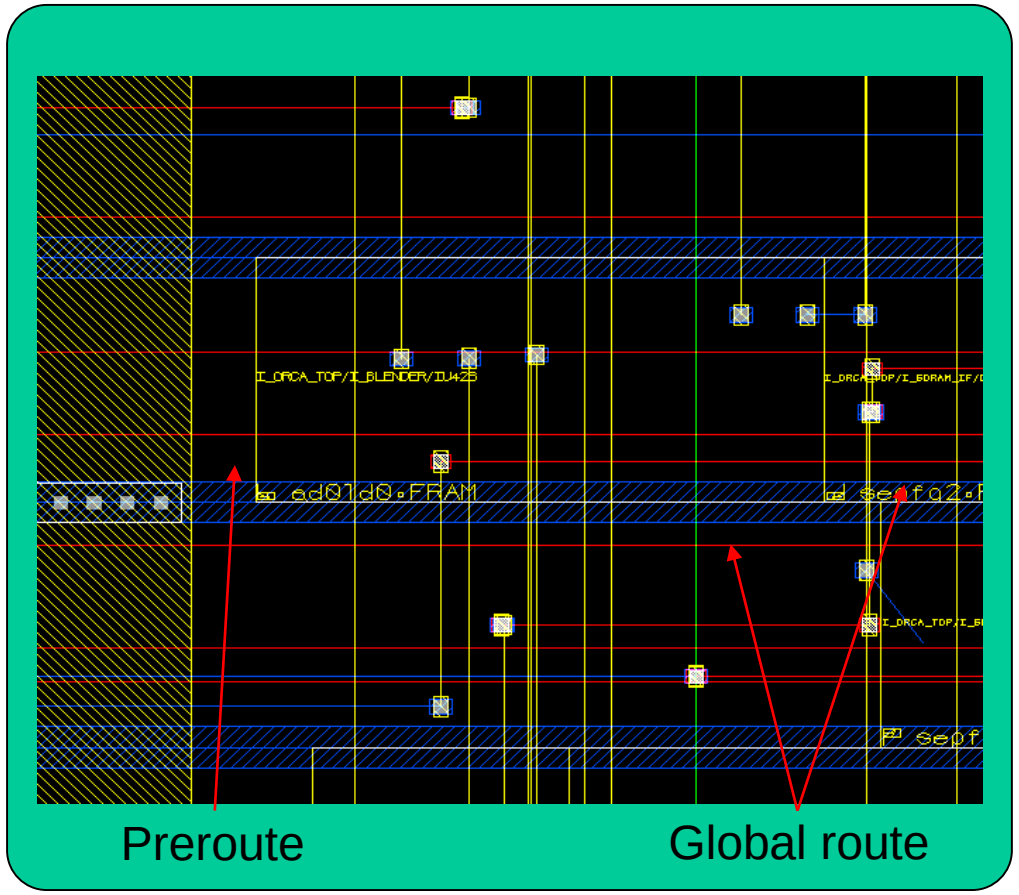
- GR assigns nets to specific metal layers and global routing cells (Gcells)
- GR tries to avoid congested Gcells while minimizing detours
  - Congestion exists when more tracks are needed than available
  - Detours increase wire length (delay)
- GR also avoids
  - P/G (rings/straps/rails)
  - Routing blockages



Metal traces exist after Global Route

source: Synopsys

Global Routing : Summary

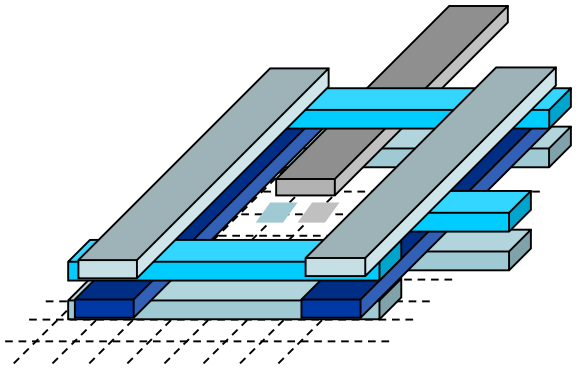


- Global routing is the first stage of routing, and provides global structure for organizing interconnects.
- The importance of global routing increases with the complexity of IC (using IP blocks, and SoC structures).
- Global routing should create good conditions for detailed routing.

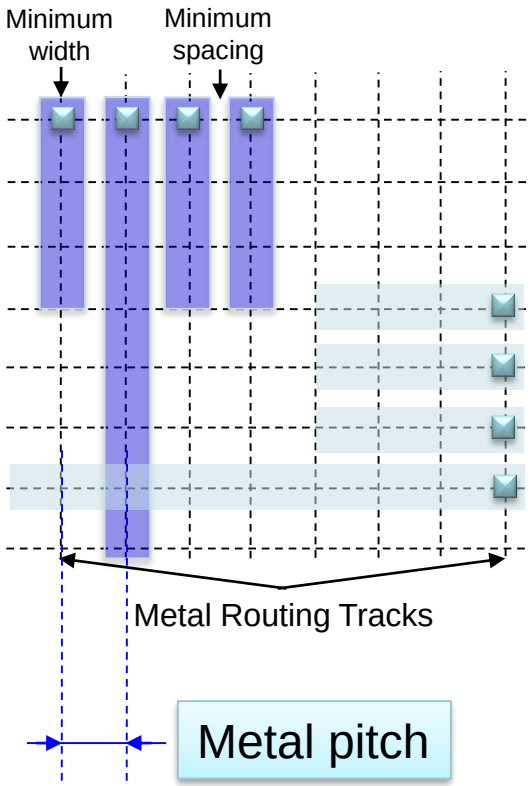
source: Synopsys

Routing Tracks (Wire Tracks)

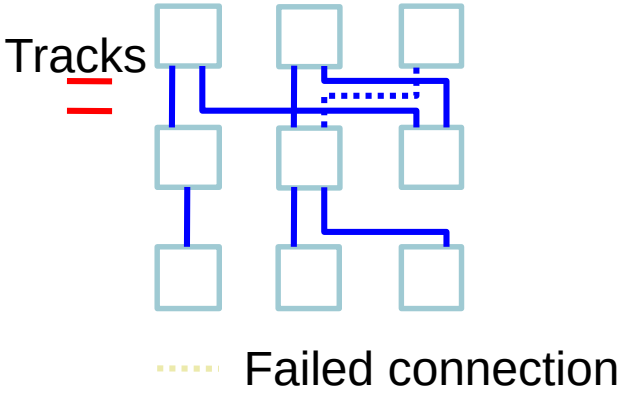
Layers have perpendicular directions



Routing is done on tracks



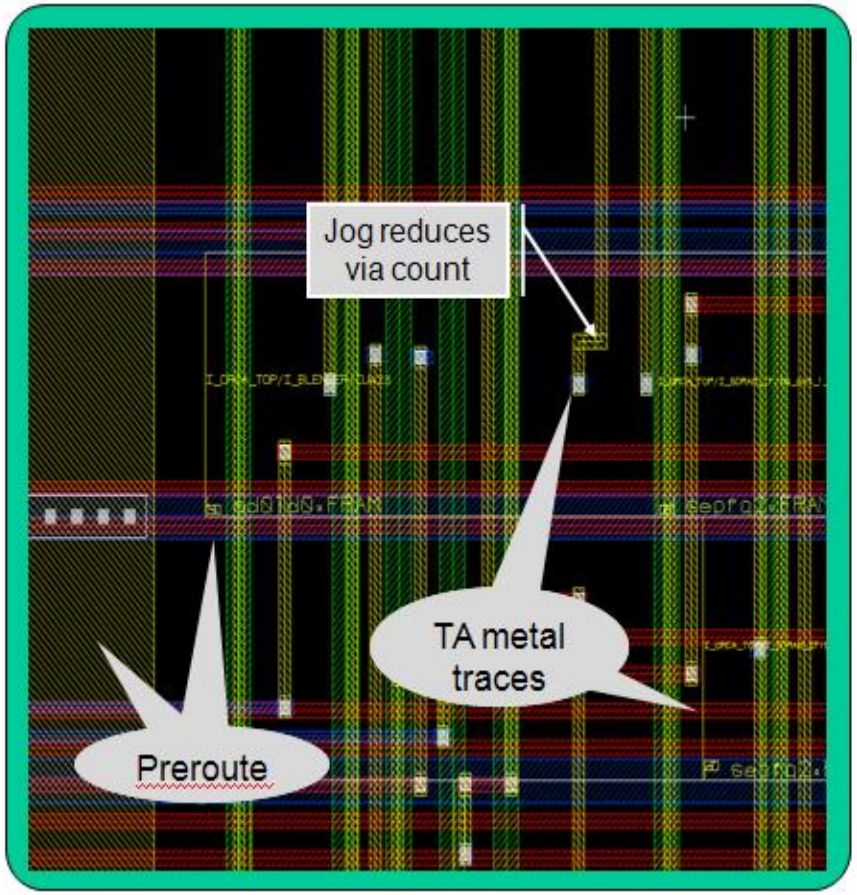
Insufficient number of tracks bring congestion



source: Synopsys

Route Operations : Track Assignment

- Track Assignment (TA):
  - Assigns each net to a specific track and lays down the actual metal traces
- It also attempts to:
  - Make long, straight traces
  - Reduce the number of vias
- TA does not check or follow physical DRC rules

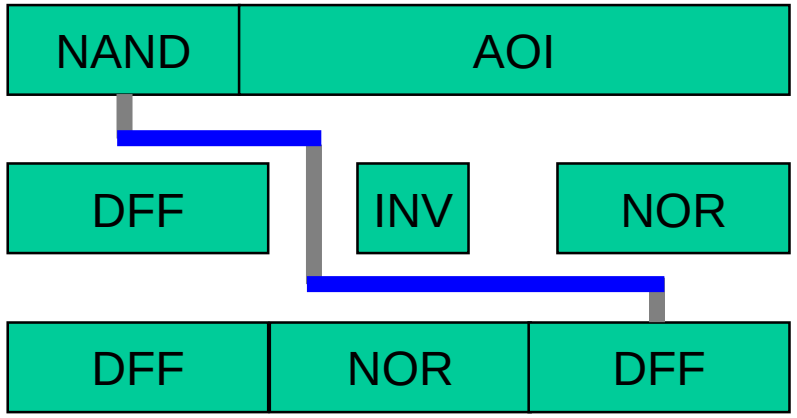


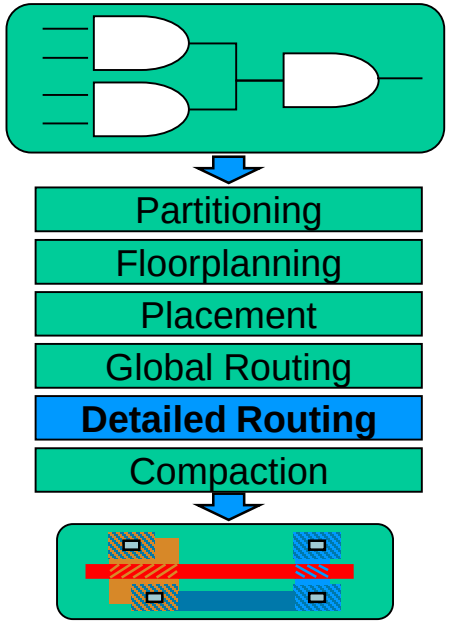
source: Synopsys

Detailed Routing

Detailed routing realizes the interconnection between each connected pair of pins in the region, which has been defined with the result of global routing.

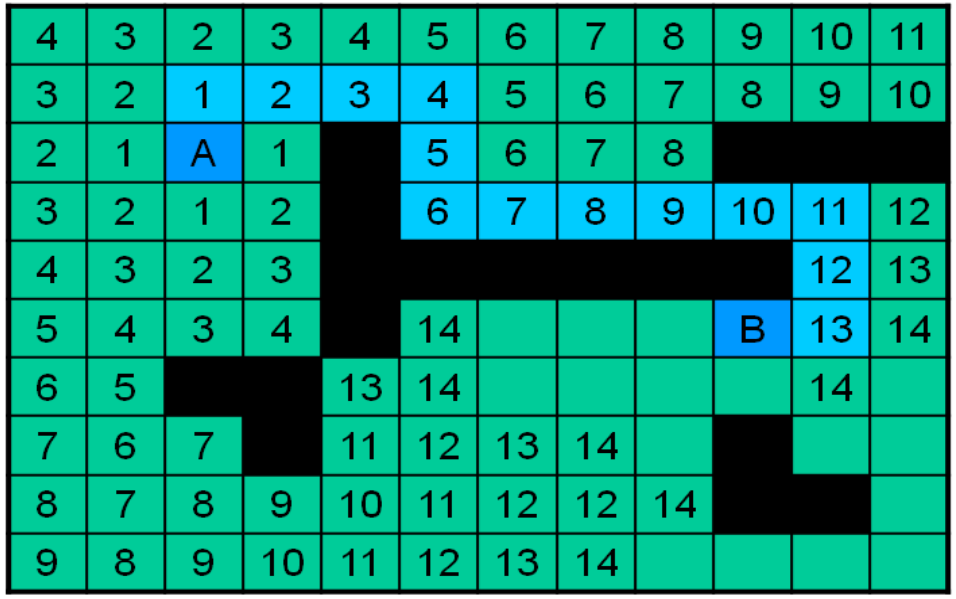
- Determining exactly how each signal is routed through each region
- Seeking to reduce routing area





source: Synopsys

Detailed Routing: Maze

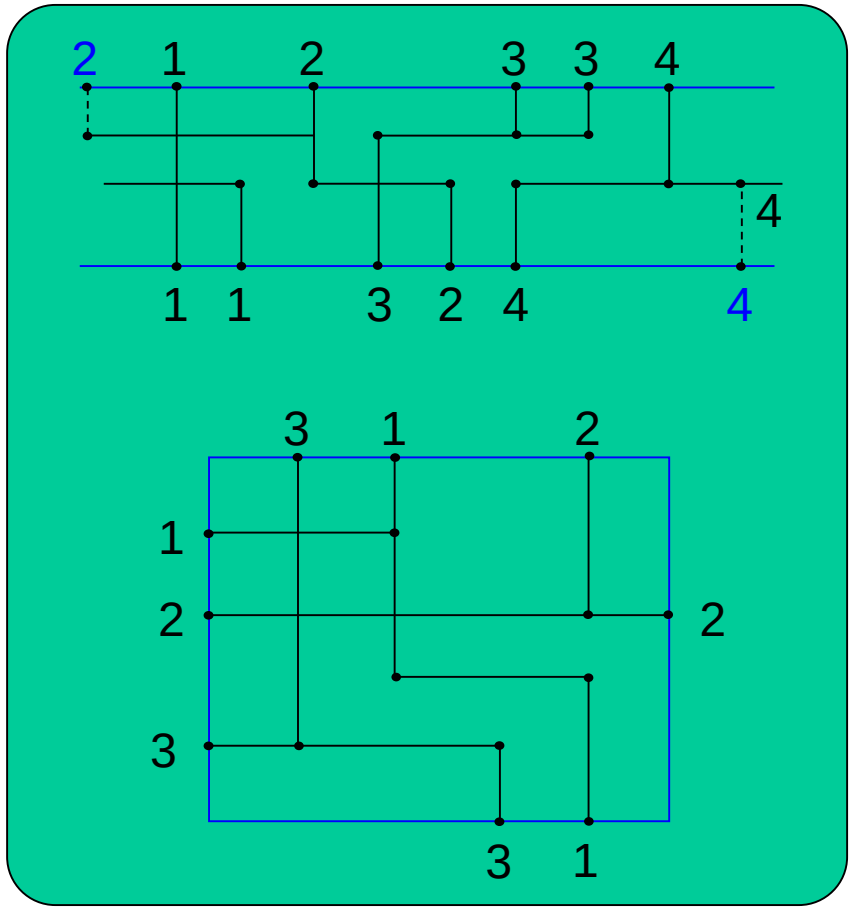


Maze routing finds a path between source (s) and target (t) in a planar graph

- The basic method of detailed routing is maze routing. The main advantage of maze routing is that it always finds the path with minimal length among all possible paths that connects the two pins.
- The disadvantage is the high machine time demand.

source: Synopsys

Detailed Routing: Channel Vs. Switchbox

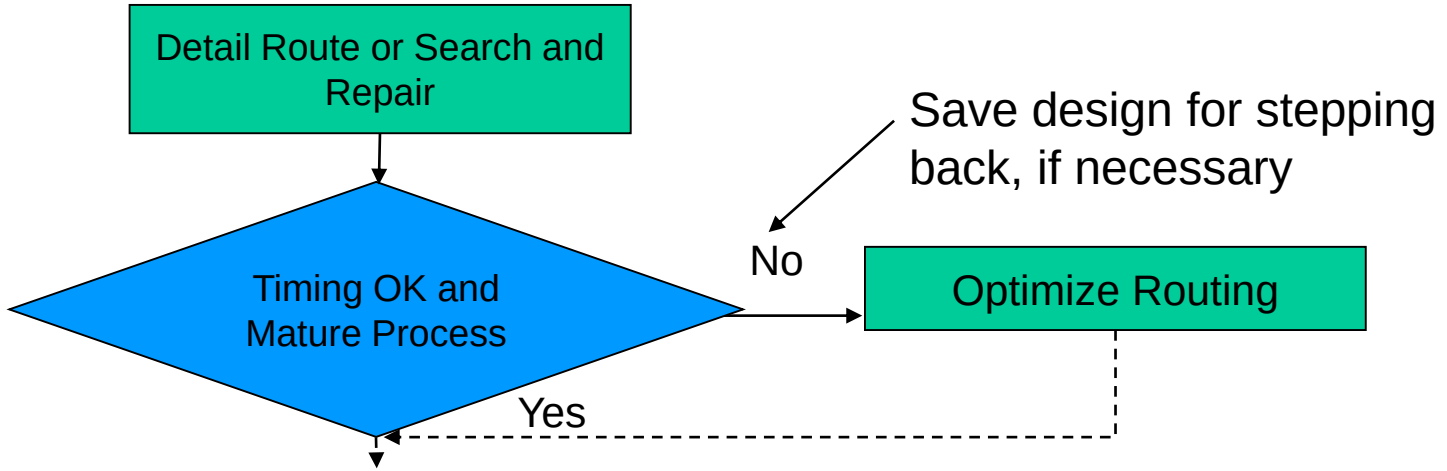


If the channel routing is a one dimensional problem (interconnects pass only in one direction), then the switchbox routing is a two dimensional problem due to which its solution is more difficult.

source: Synopsys

Route Optimization

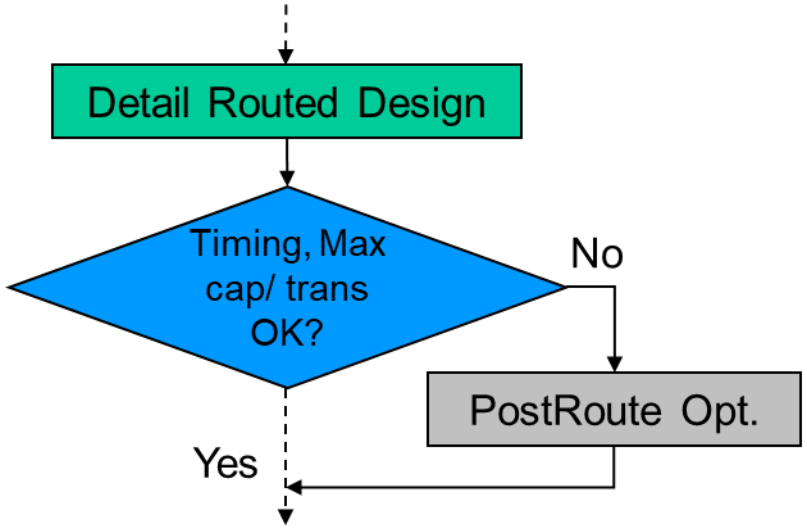
- Route optimization can be done by reducing wire length and number of vias, and also by removing unnecessary jogs
- If the process is new or unproven then the reduction in via counts and the increase in long straight routes may improve yield



source: Synopsys

PostRoute Optimization

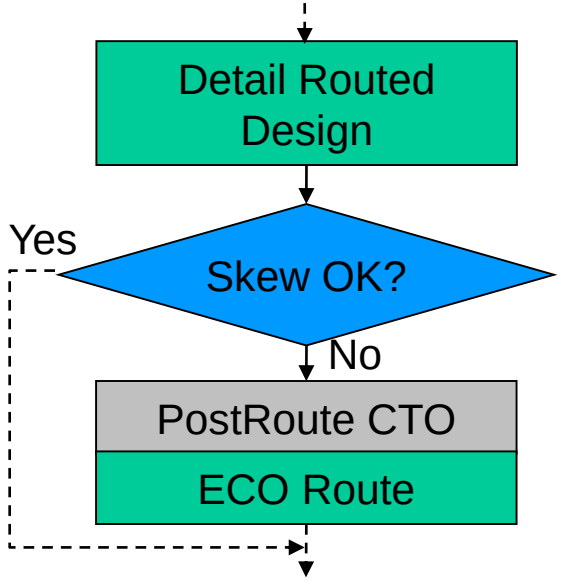
- Performing cell sizing, buffer and inverter insertion
- Powerful hold time fixing
- Topology based optimization



source: Synopsys

PostRoute Clock Tree Optimization (CTO)

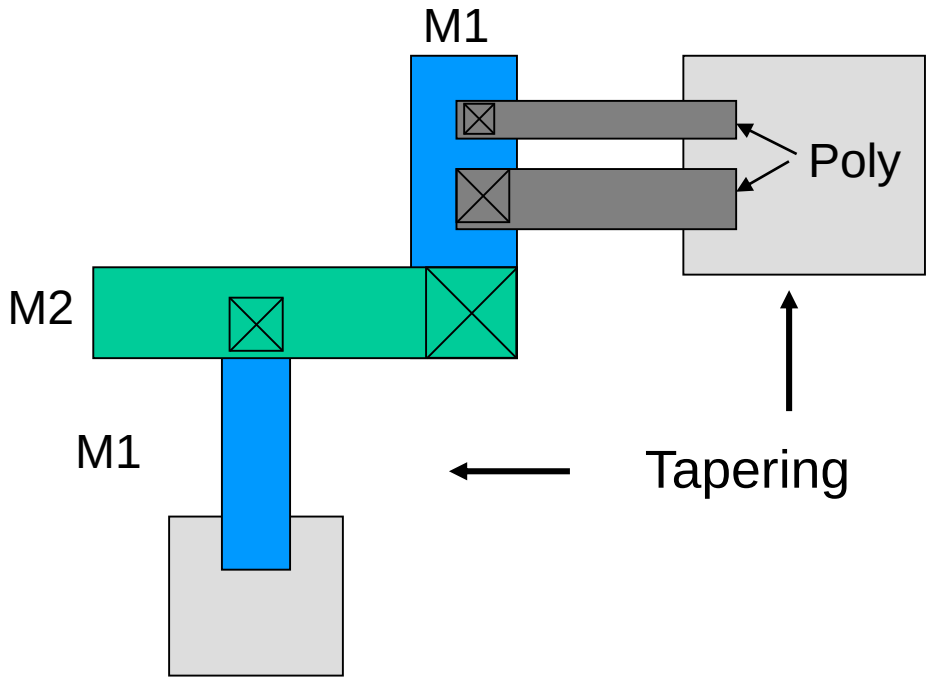
- Clock skew may have been disturbed by previous routing and route optimization activity
- The CTO step can be used to improve the skew on clock nets



source: Synopsys

Detailed Routing Objectives (1)

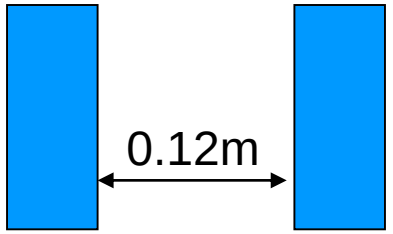
- Routing completion
- Width and spacing rule
  - Minimum width and spacing
  - Variable width and spacing
    - Connection
    - Net
    - Class of nets
  - Tapering



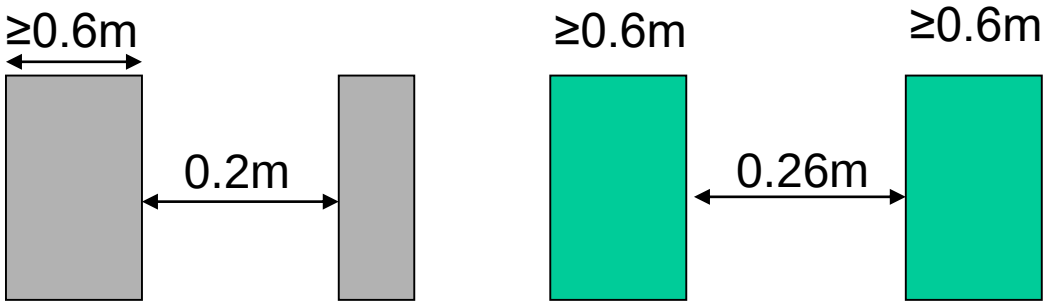
source: Synopsys

Detailed Routing Objectives (2)

Width and spacing rule



Minimum spacing



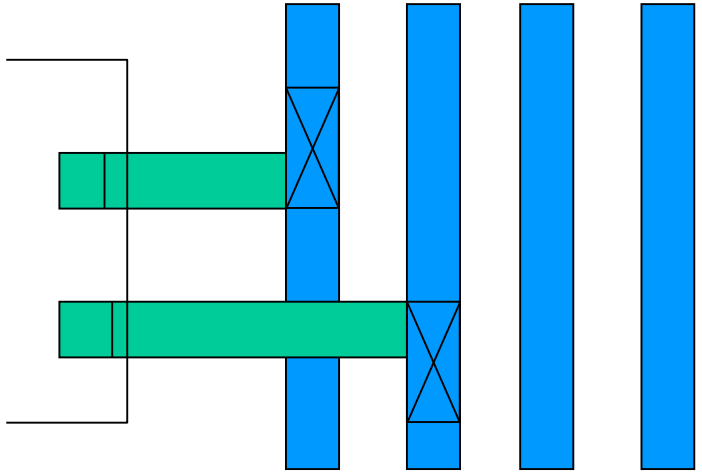
Width-based spacing

source: Synopsys

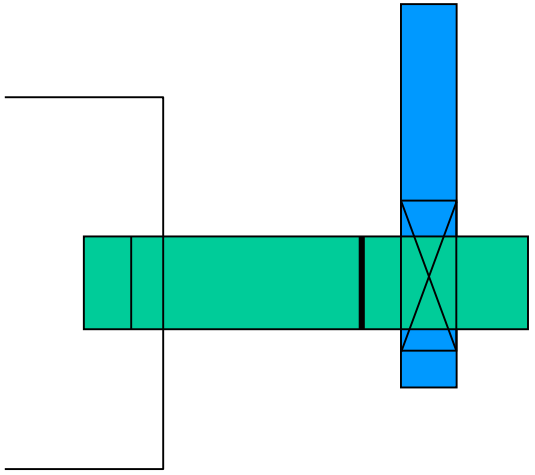
Detailed Routing Objectives (3)

- Via selection
  - Via array based on wire size or resistance
  - Rectangular via rotation and offset

Rotate and offset horizontal vias



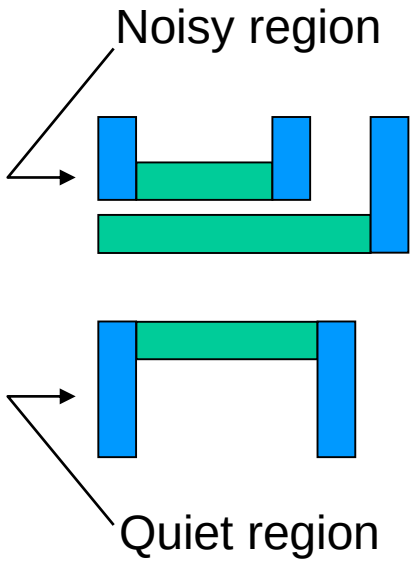
No rotation for a “cross” via



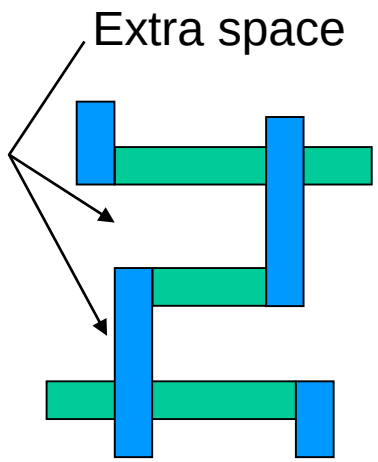
source: Synopsys

Detailed Routing Objectives (4)

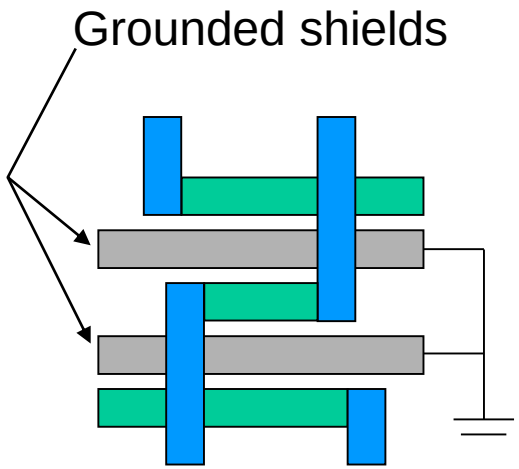
Noise-driven



Segregation



Spacing



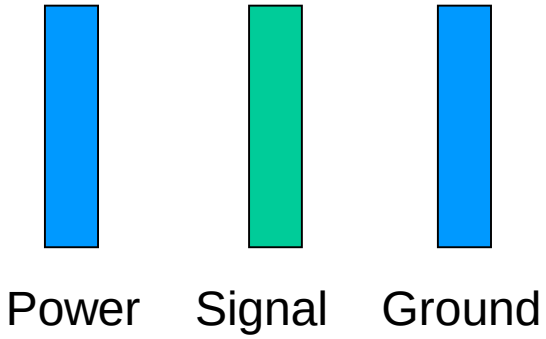
Shielding

source: Synopsys

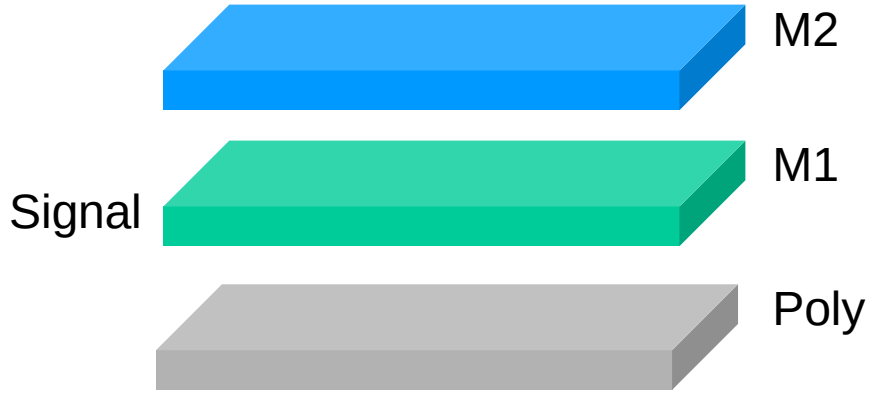
Detailed Routing Objectives (5)

- Shielding
  - Same-layer shielding
  - Adjacent-layer shielding

Same-layer shielding



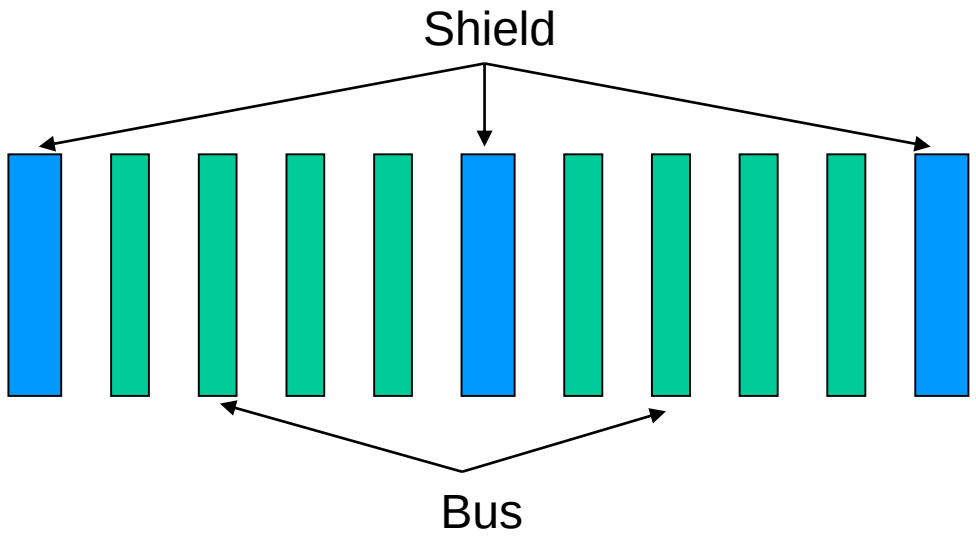
Adjacent-layer shielding



source: Synopsys

Detailed Routing Objectives (6)

- Shielding
  - Bus shielding
  - Bus interleaving



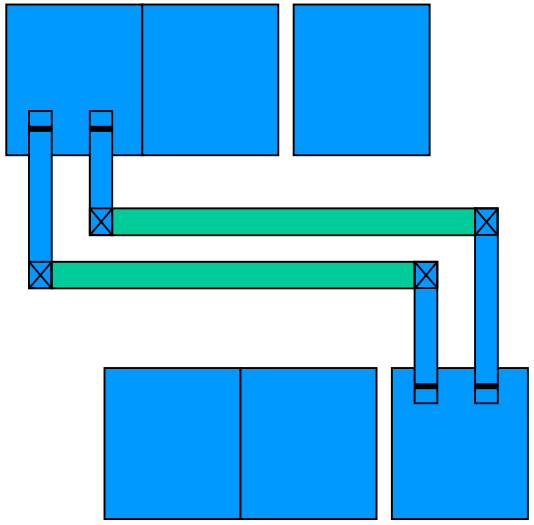
Bus shielding

source: Synopsys

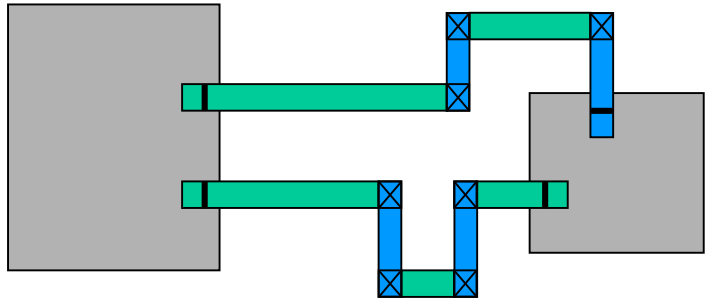
Detailed Routing Objectives (7)

- Differential pair routing
- Balanced length or capacitance

Differential



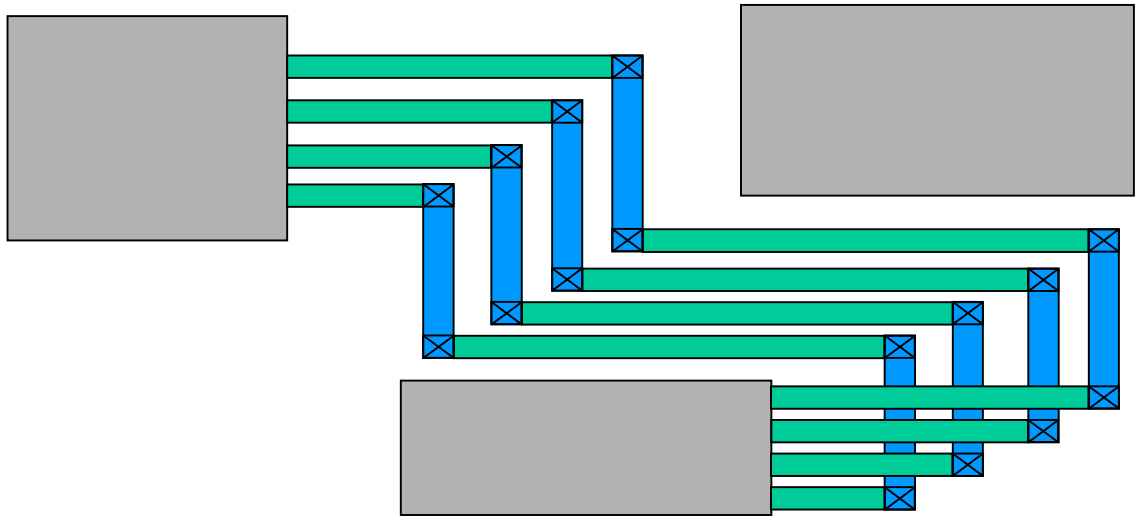
Balanced length



source: Synopsys

Detailed Routing Objectives (8)

Bus routing

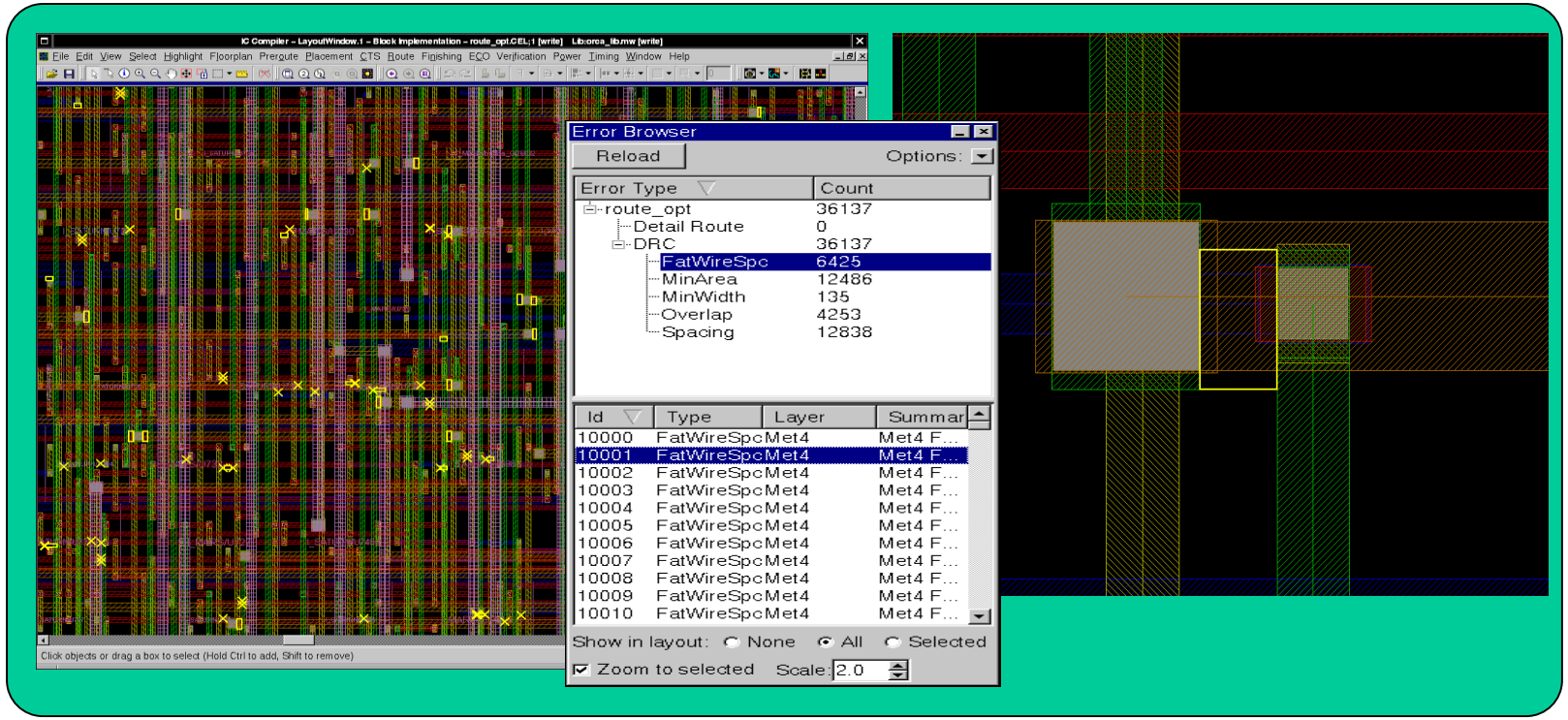


The essence is that by changing the metal layer several times (e.g., 4 times) it is possible to route congested parallel buses using 2 metal layers if there are blocks that close the direct path (e.g., the right block above).

source: Synopsys

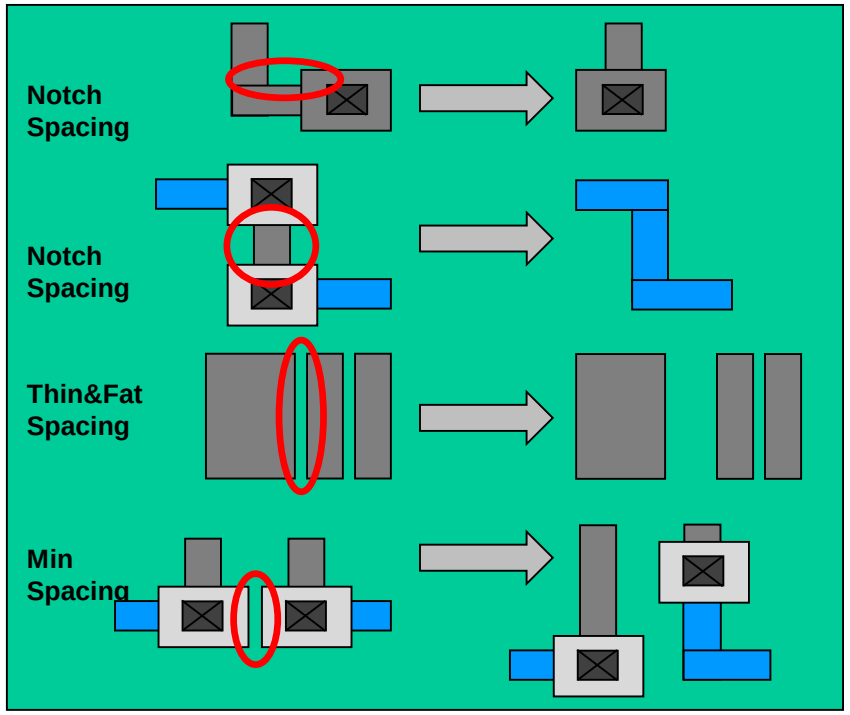
Analysis of the Routing DRC Errors

`verify_route`	**Uses router DRC engine**
`verify_drc`	**Uses Hercules for DRC**



source: Synopsys

Fixing DRC Violations



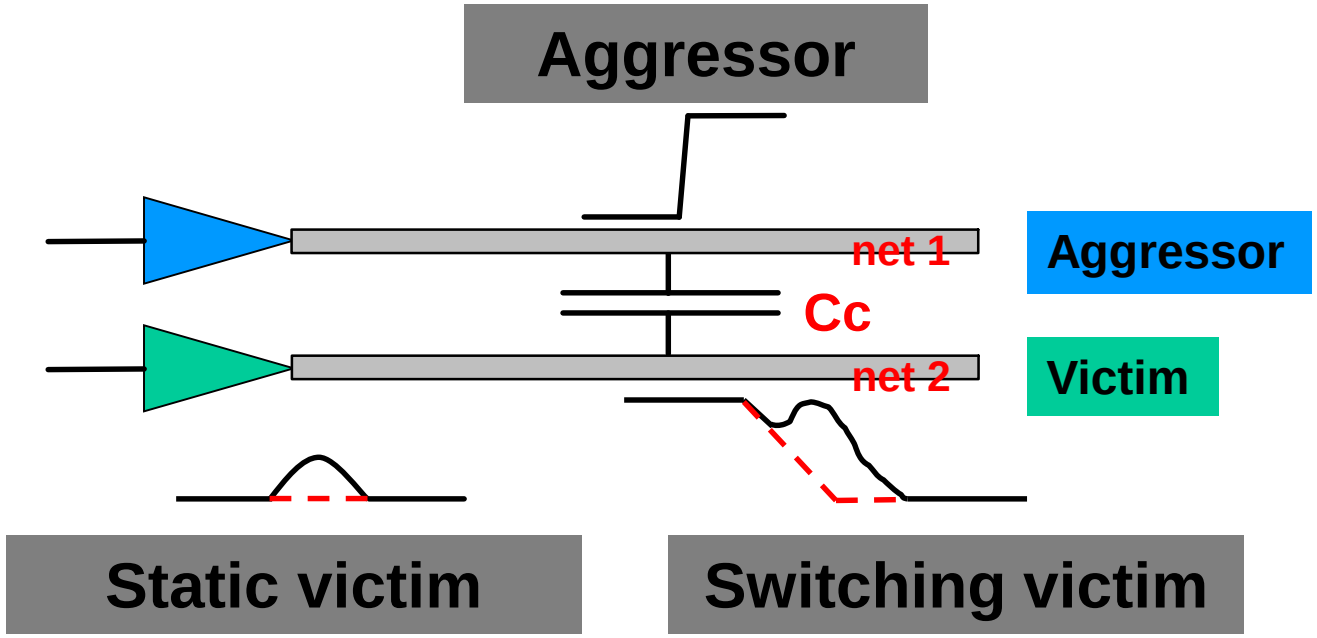
Use route_opt (fixes timing as well):

```
route_opt -incremental
```

source: Synopsys

Crosstalk (Xtalk)

Crosstalk is the transfer of a voltage transition from one switching net (aggressor) to another static or switching net (victim) through a coupling capacitance (Cc)

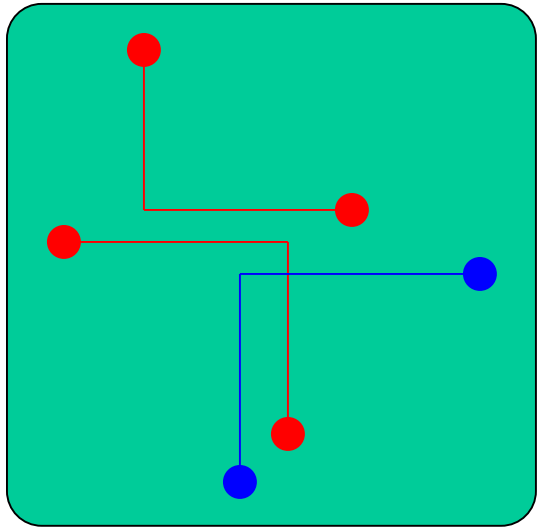


source: Synopsys

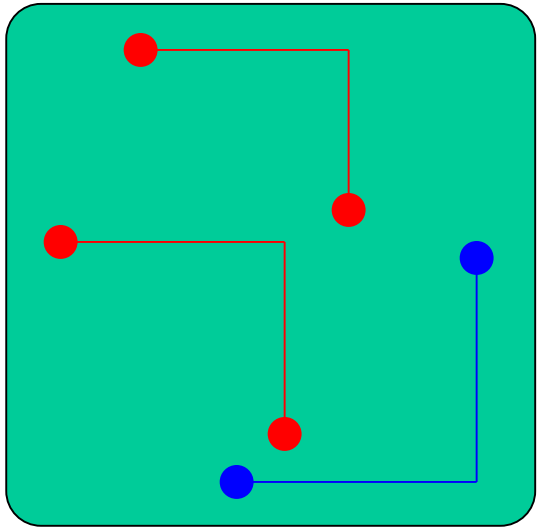
Coupling-Free Routing (CFR)

- Coupling-free Routing means there is a single bend layout for every net such that no two routes couple

Coupled layout

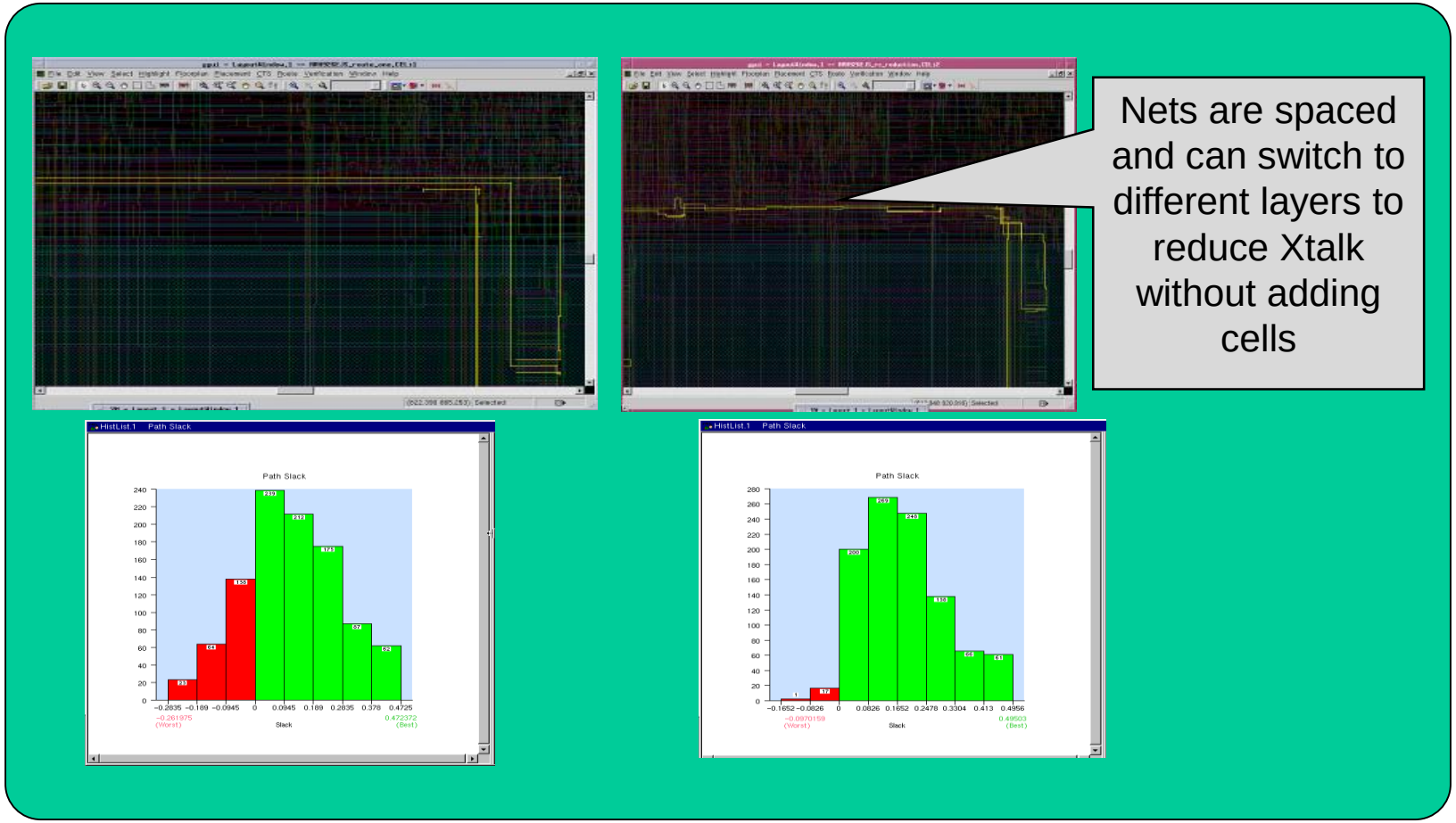


Coupling-free layout



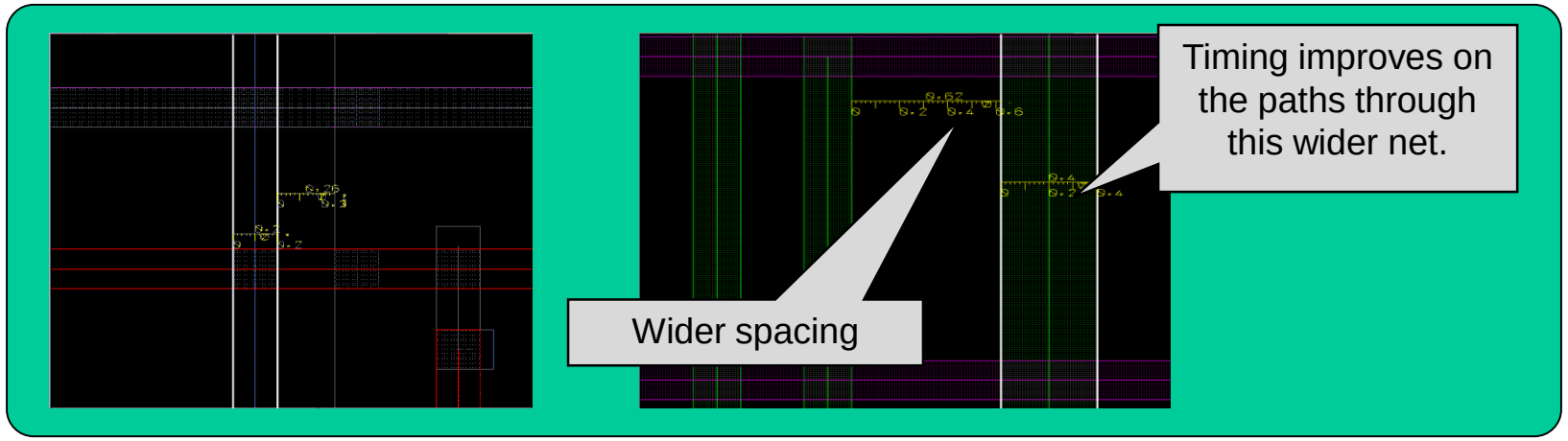
source: Synopsys

Xtalk-Reduction at Work



source: Synopsys

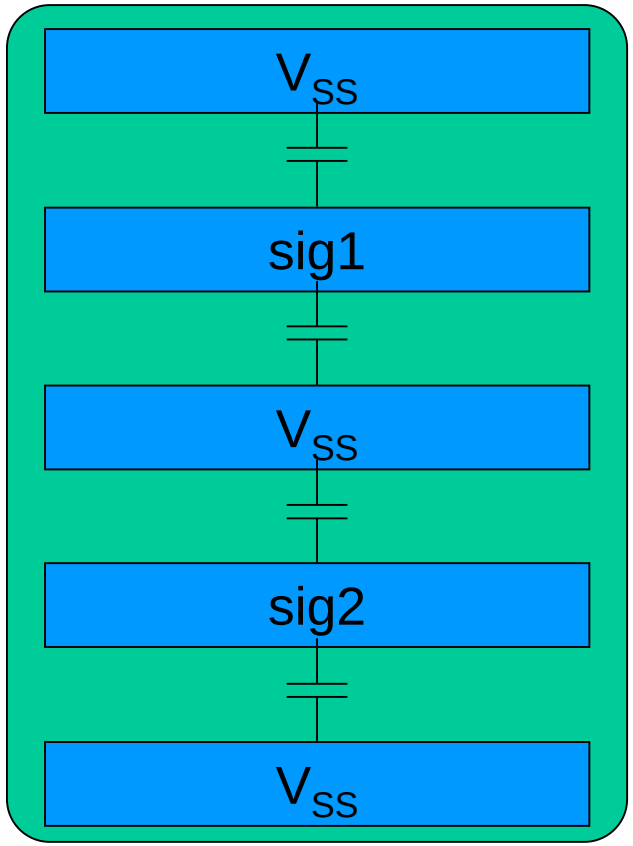
Wire Sizing at Work



- Critical wire has been made wider to solve a timing violation. Since R is reduced, it can benefit the timing. The wider spacing helps crosstalk.
- Use carefully since too many NDRs can make the design unroutable.

source: Synopsys

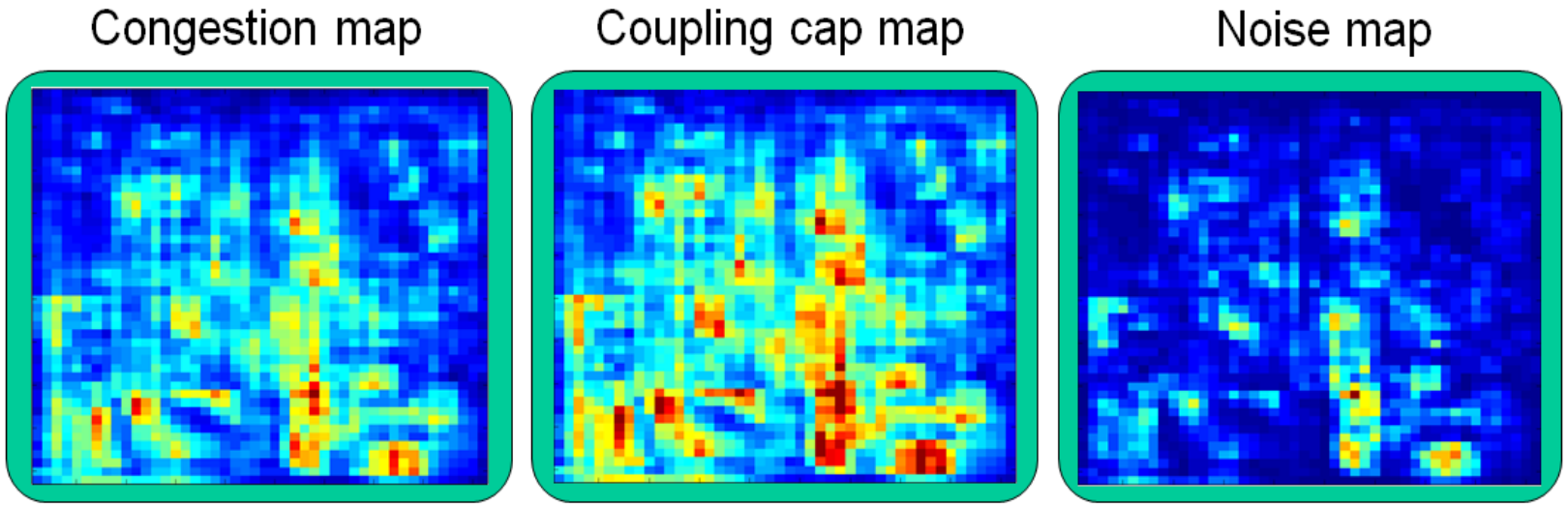
Crosstalk and Physical Synthesis: Ground Wires



- In order to isolate signal nets passing through different layers and to reduce crosstalk, ground wires are added (shown in figure) between signal wires.
- VSS can be used to distribute power as long as the power line is relatively stable.

source: Synopsys

Congestion, Coupling and Noise Maps



Congestion map not necessarily matches to coupling capacitance map → Coupling is more pervasive than congestion

Coupling cap map is different from noise map → Noise also depends on electrical properties (Rd for victim net)

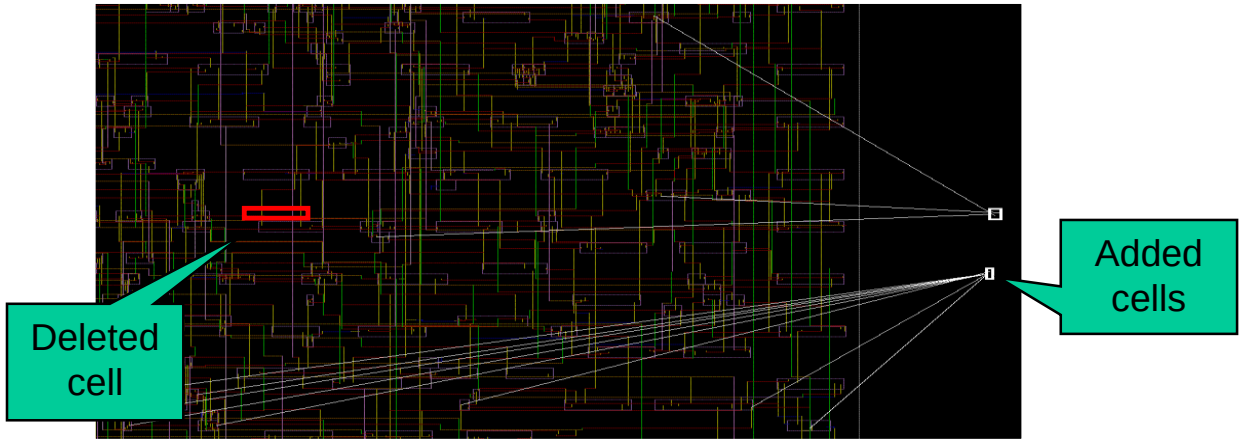
source: Synopsys

ECO: Engineering Change Order

Fix things in the last minute…

ECOs: Making Changes Late in the Flow

- "ECO" is an old term which stands for "Engineering Change Order".
- In the early days of circuit design, if a change has to be made in the design which was already defined or specified, then an "Engineering Change Order" form has to be filled out and signed before making the change.



Functional changes occur late in the design cycle

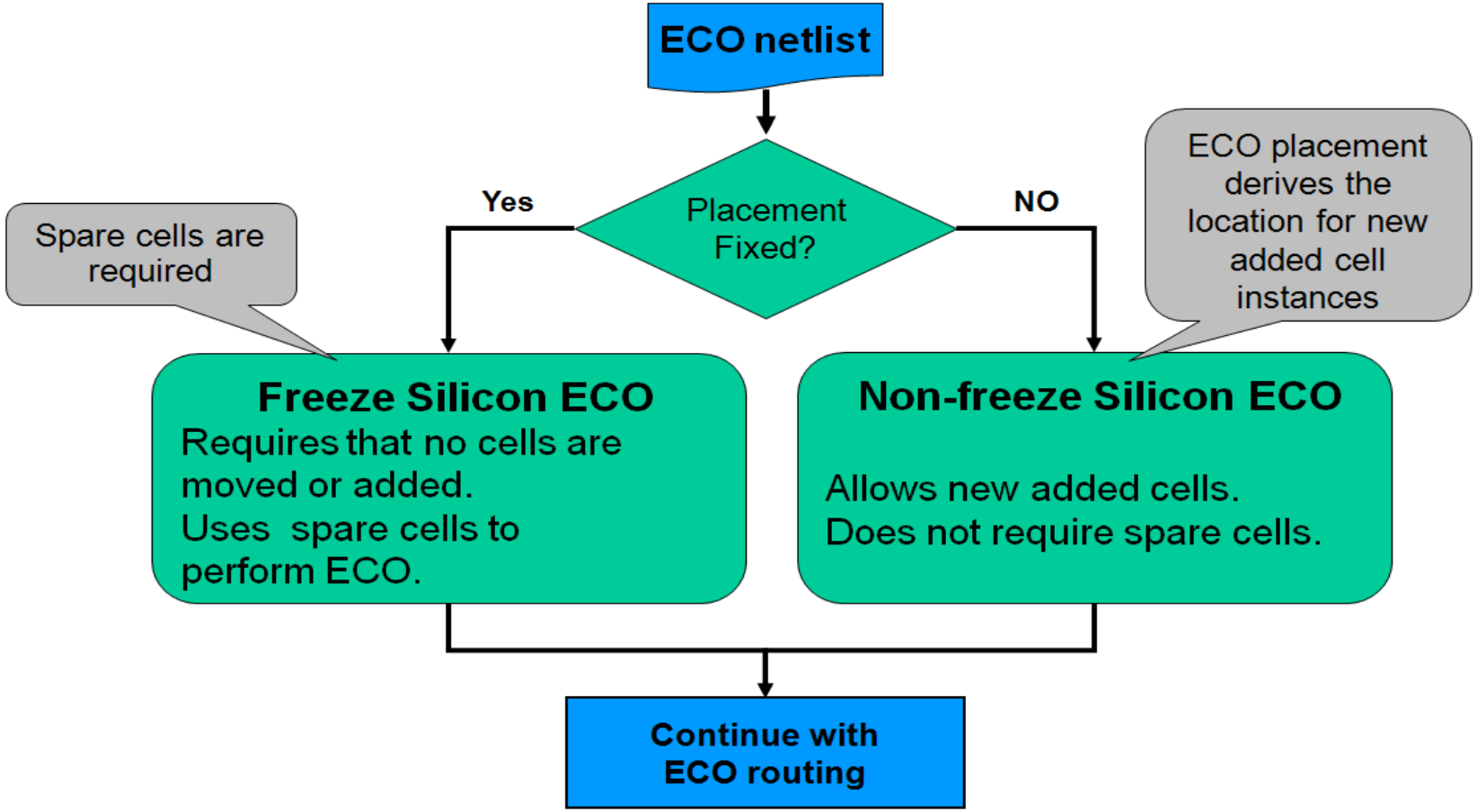
source: Synopsys

Types of ECO

- Functional ECO
  - Functional bug that was discovered in the last minute
- Timing ECO
  - ECOs that are required to fix timing violations
  - E.g. Swap cells, move to a different location
- Power ECO
  - ECOs that are required to fixing power violations
- ECO cells
  - Special cells that designed so it can later be configured to perform certain functions

source: Synopsys

Two Types of ECO Flows



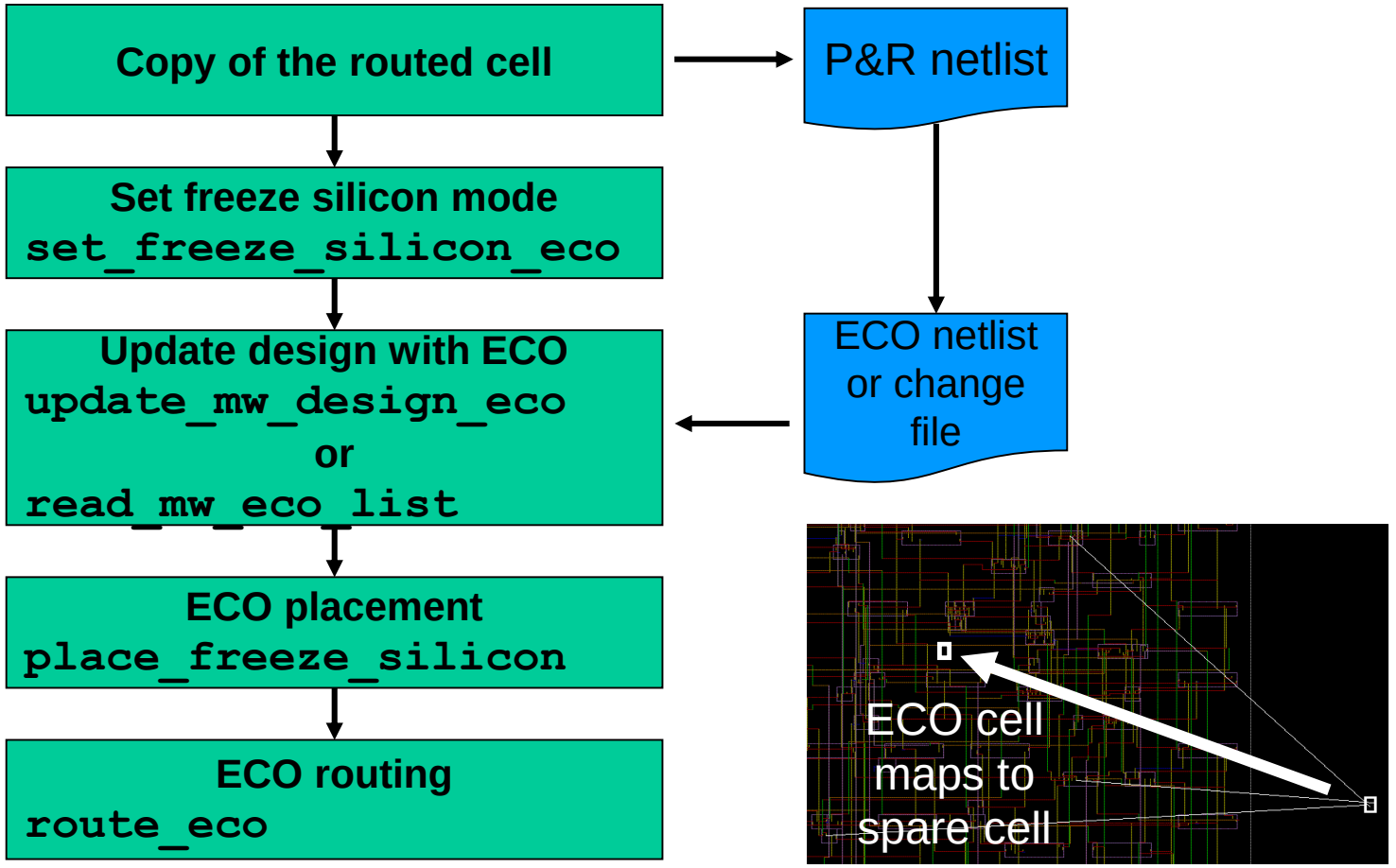
source: Synopsys

ECO Flows

- Non-Freeze silicon ECO
  - Pre-tapeout - no restriction on placement or routing
  - Minimal disturbances to the existing layout
  - ECO cells are placed close to their optimal locations
- Freeze silicon ECO
  - Post-tapeout - metal masks change only using previously inserted spare cells
  - Cell placement remains unchanged
  - ECO cells are mapped to spare cells that are closest to the optimal location
  - Deleted cells become spare cells

source: Synopsys

Freeze Silicon ECO: Metal Change Only

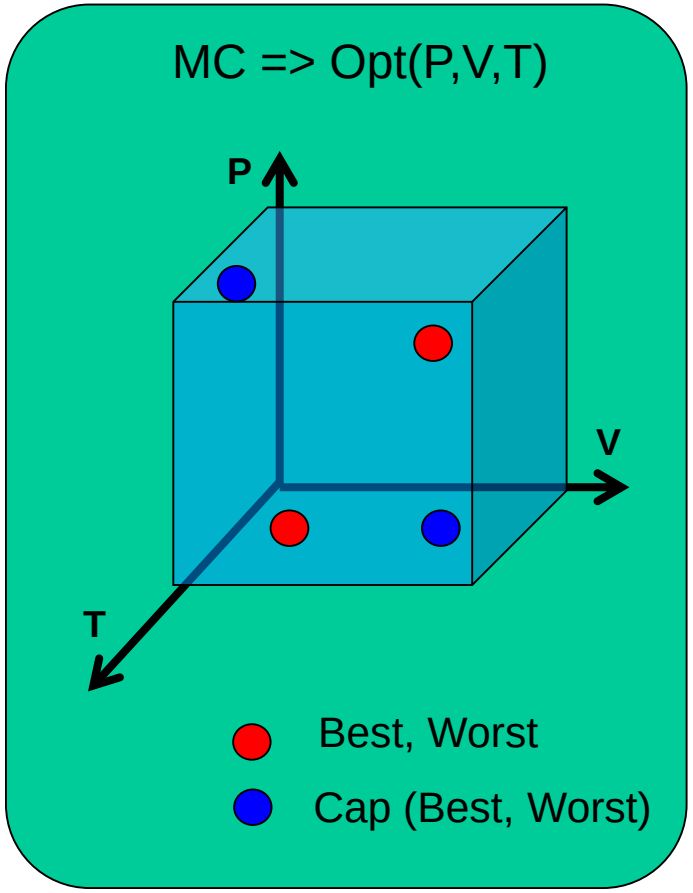


source: Synopsys

Multi Scenario Optimization

How to ensure that the chip works under multiple corners…

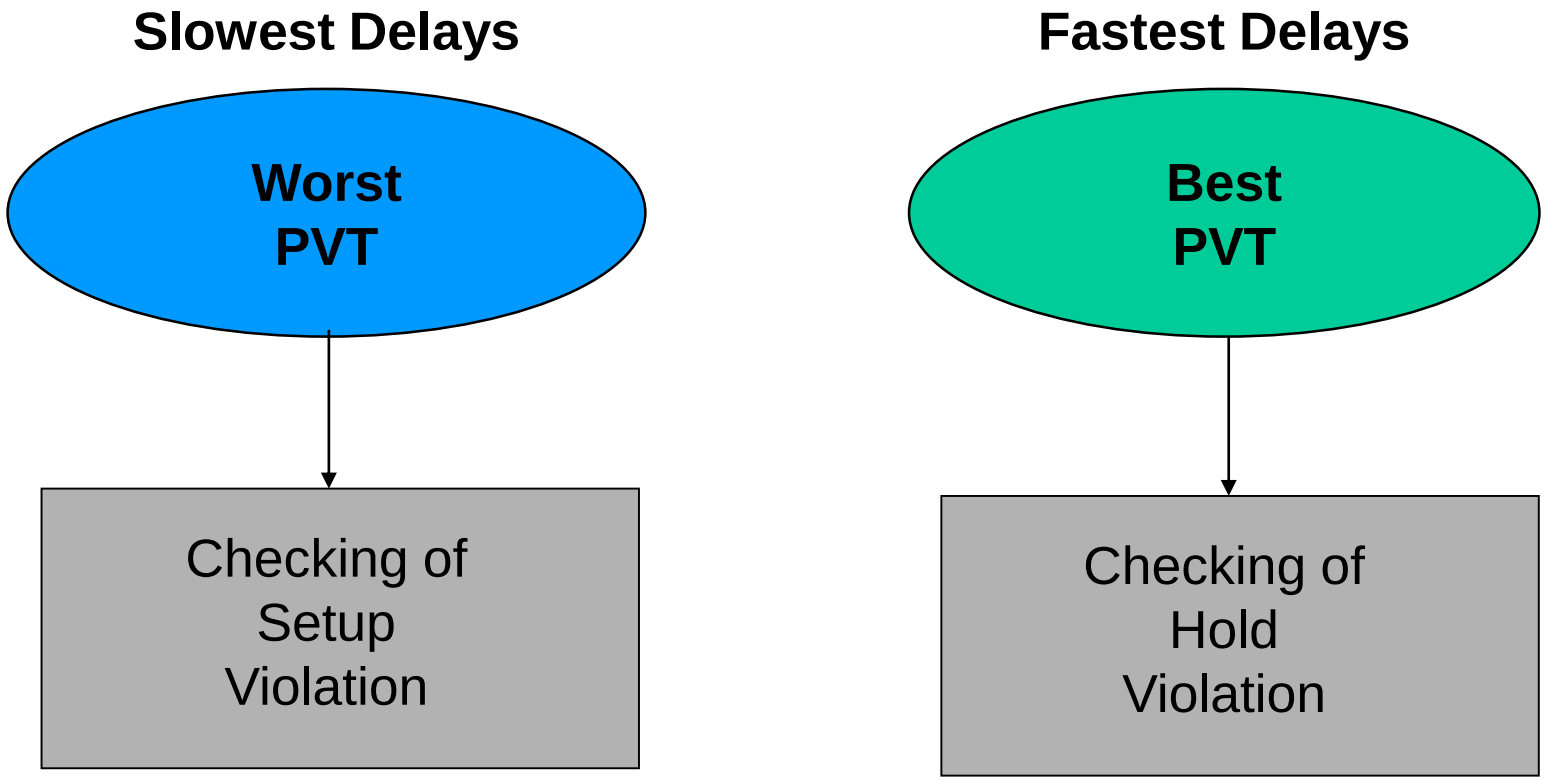
Multi-Corner Problem



A corner is defined as a PVT and it is provided to the tool as logic libraries per PVT and as parasitics data.

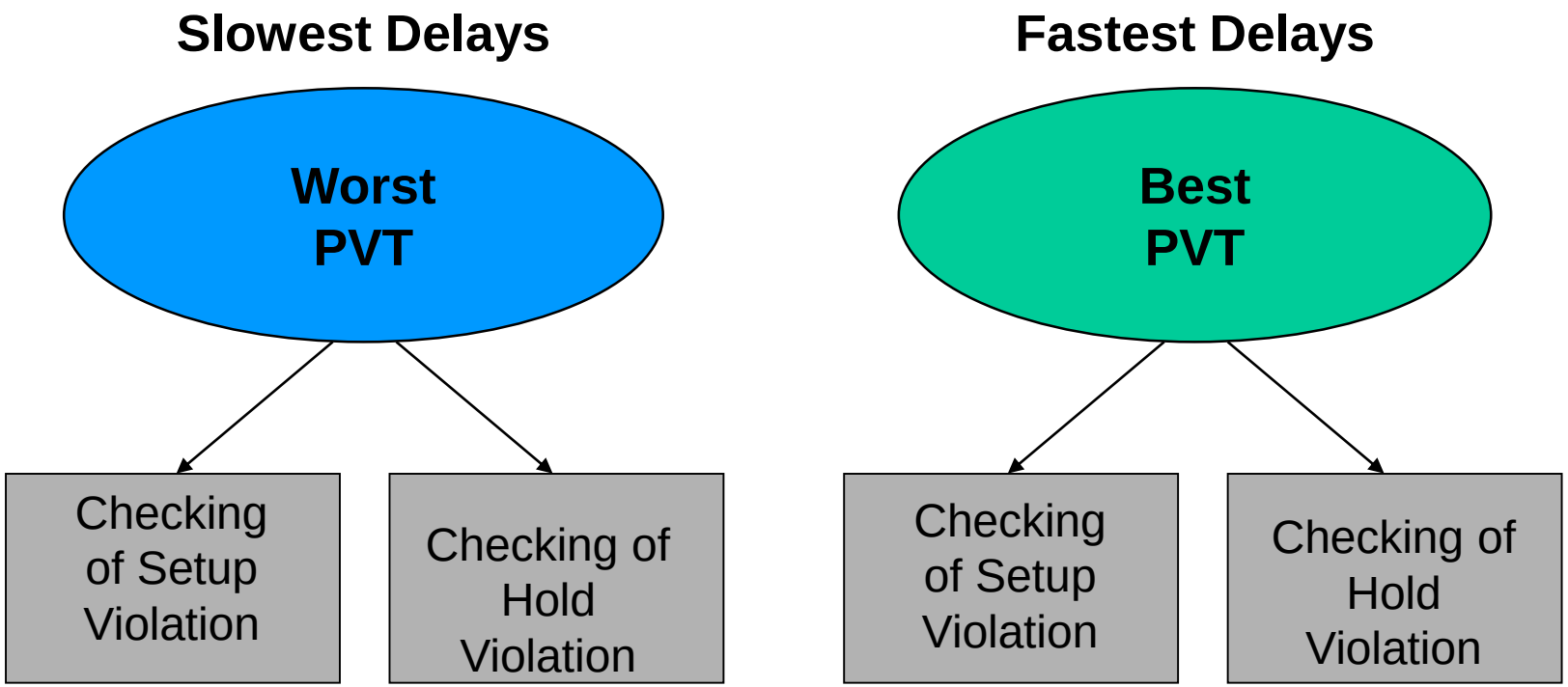
source: Synopsys

Best/Worst Analysis Essence



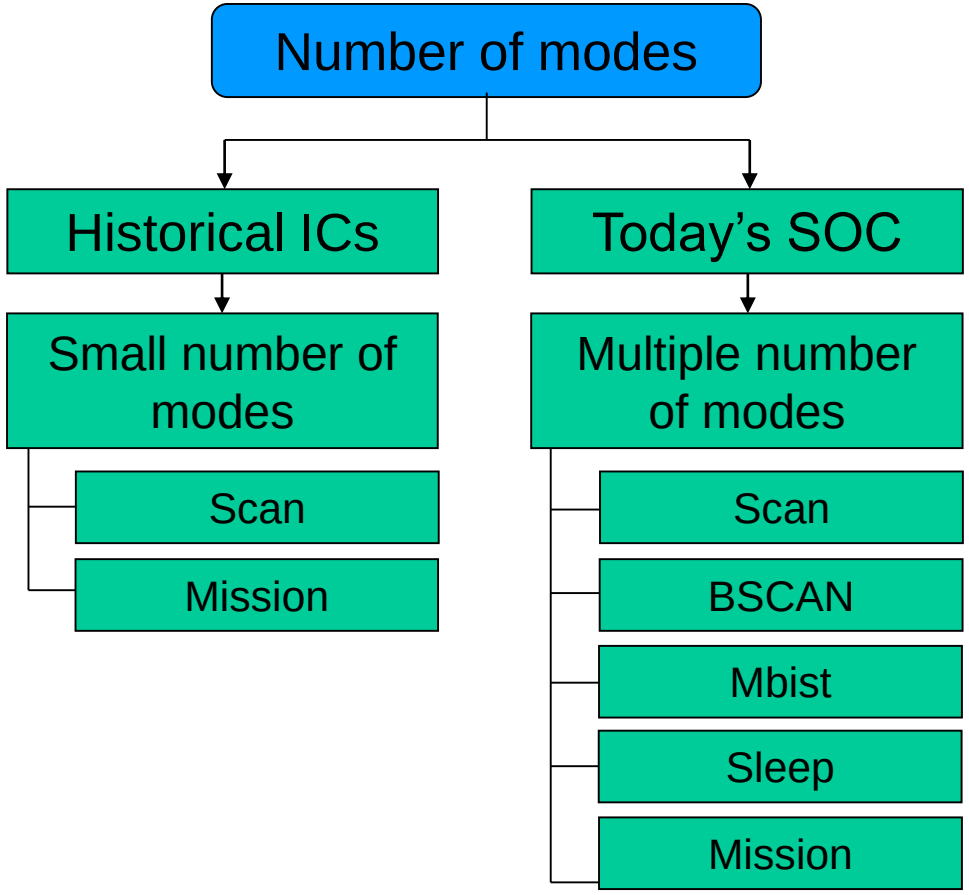
source: Synopsys

Necessity of Multi Corner Analysis

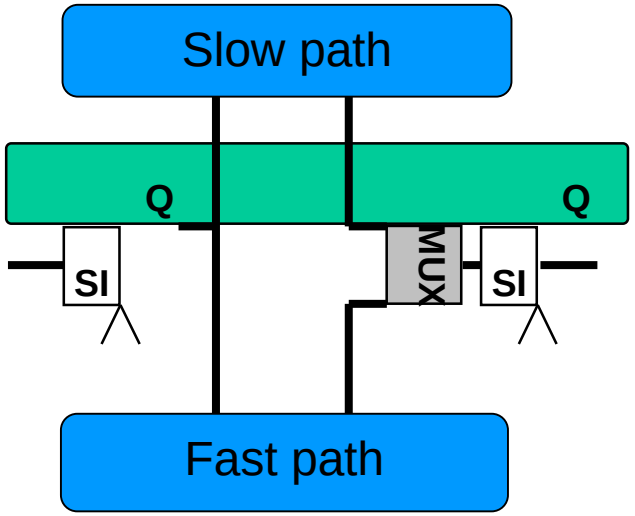


source: Synopsys

Multi Mode Problem in SoC

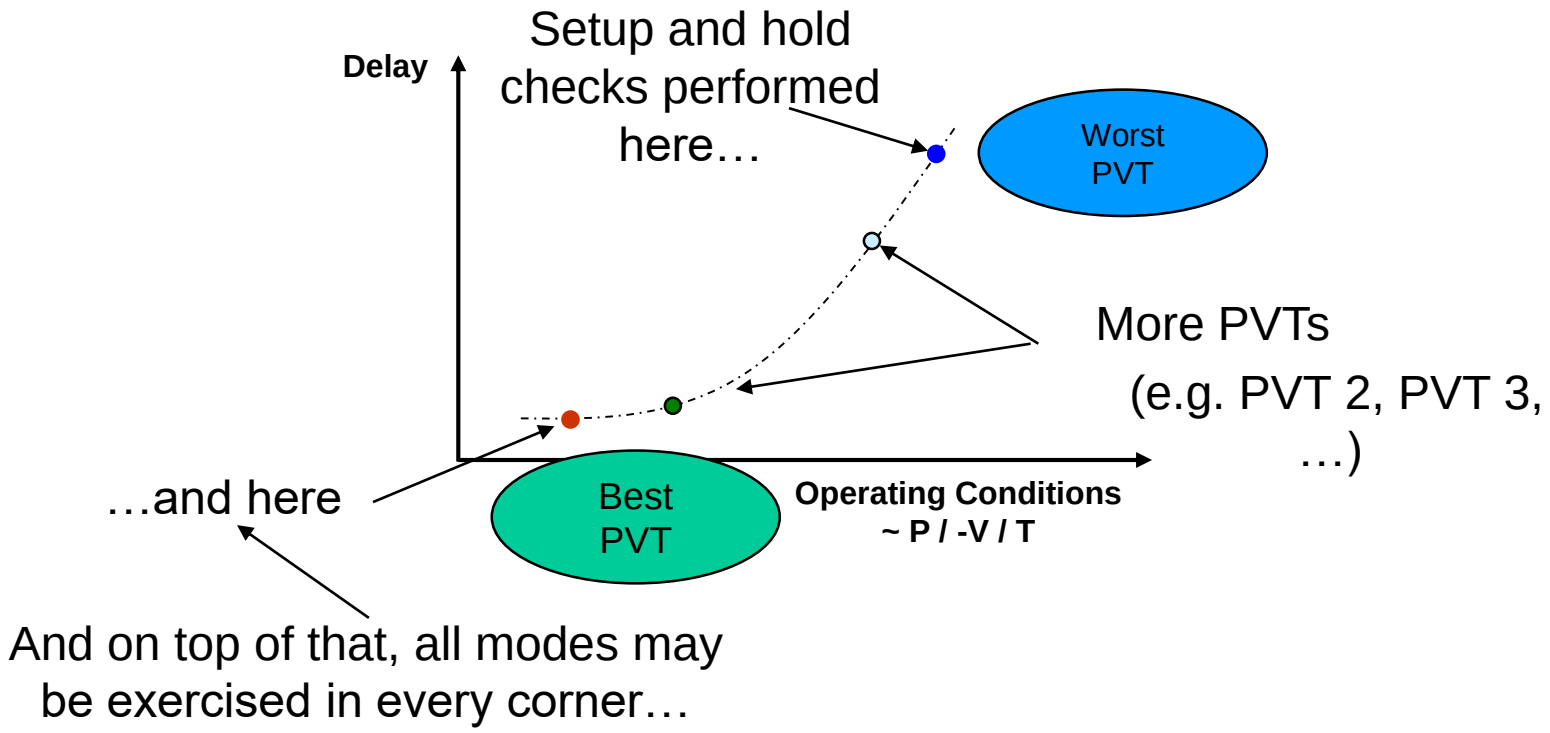


MM => Opt(mode)



source: Synopsys

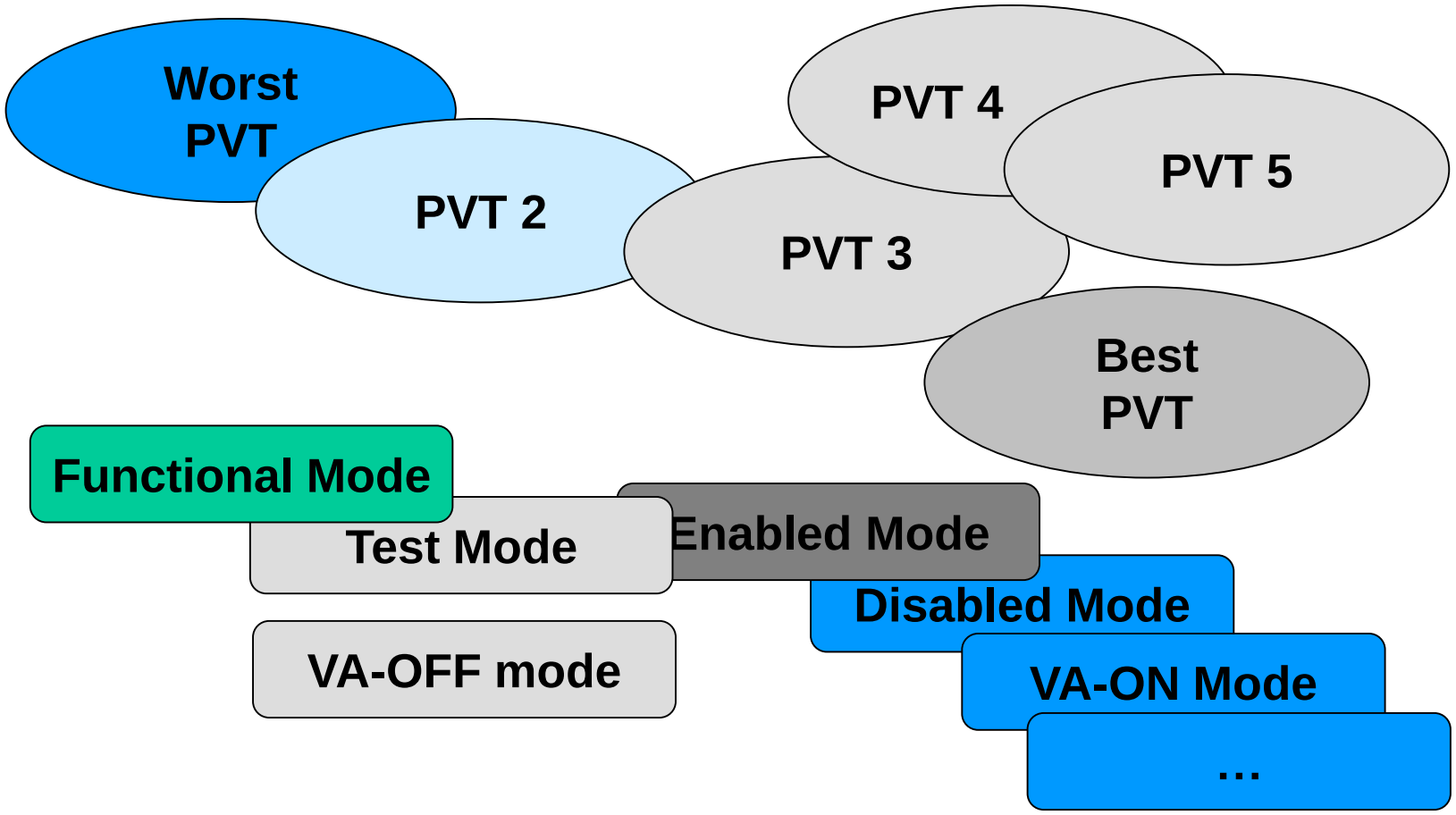
Combination of Corners and Modes



Number of runs = number of Modes x number of PVT corners

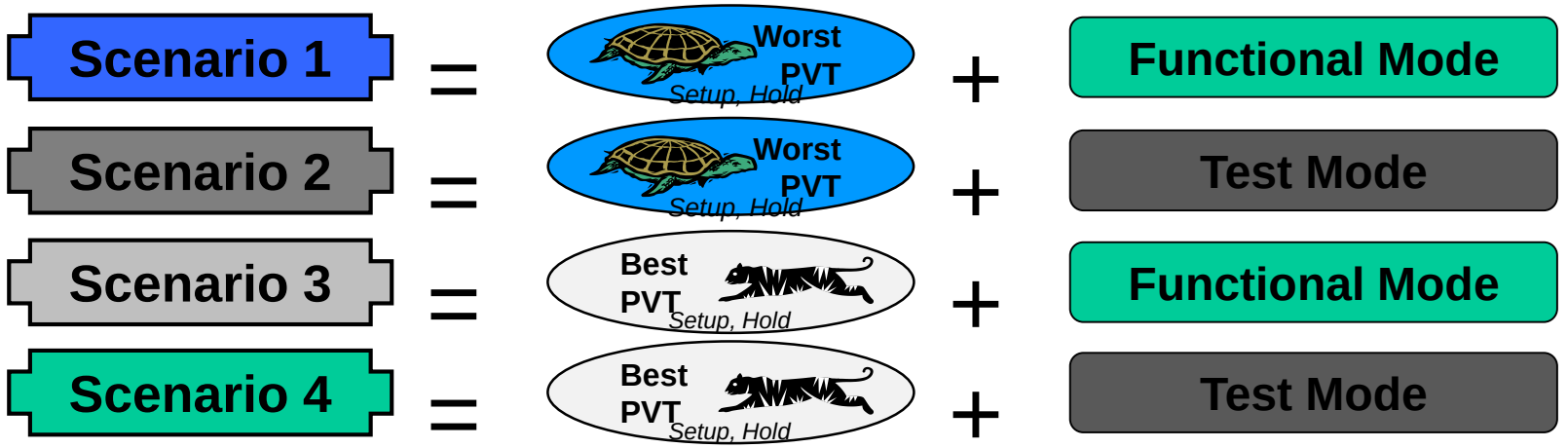
source: Synopsys

Multiple Corners – Multiple Modes



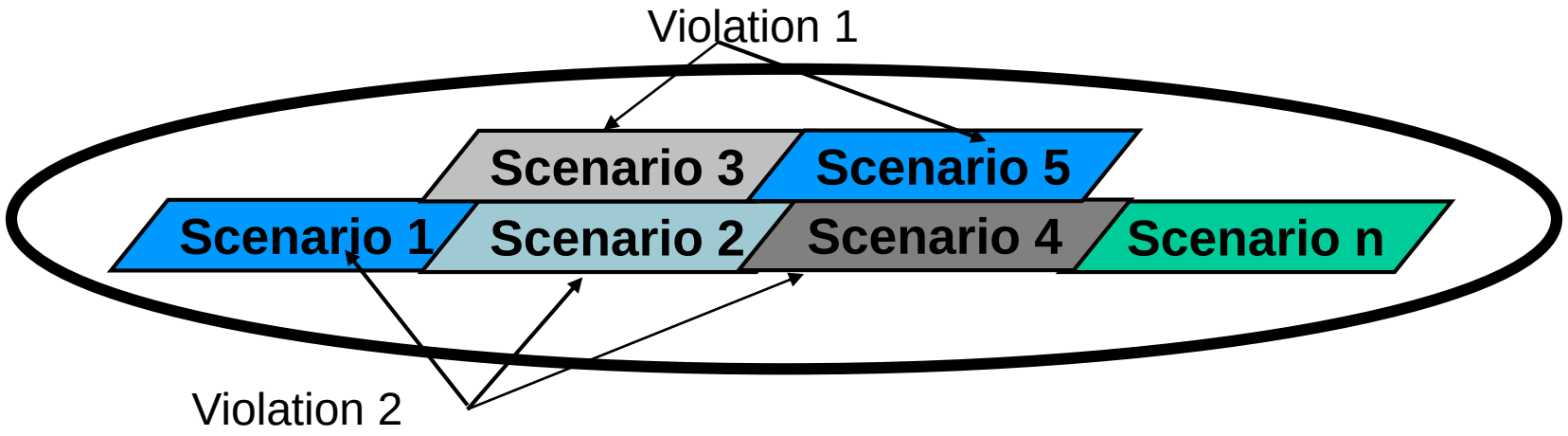
source: Synopsys

Scenarios



source: Synopsys

Fixing of Violations



- Concurrent MM/MC optimization works on all violations and on all scenarios thereby eliminating the convergence problems observed in sequential approaches.
- Optimization is performed for timing, power (leakage), noise, DRC, area, etc.
- MM/MC optimization utilizes a concurrent costing engine which ensures that every transformation is acceptable for all scenarios' costs.

source: Synopsys

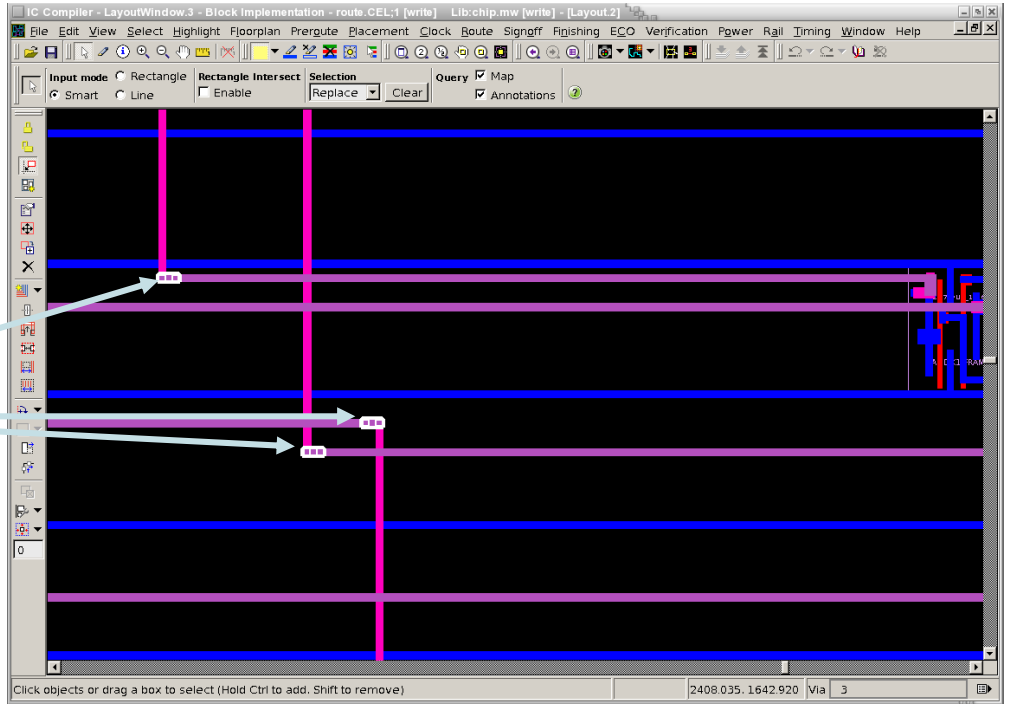
Chip Finishing

Still a few more steps to finish the implementation…

Redundant Vias

- Redundant via insertion is a widely recommended technique to enhance the via yield and reliability

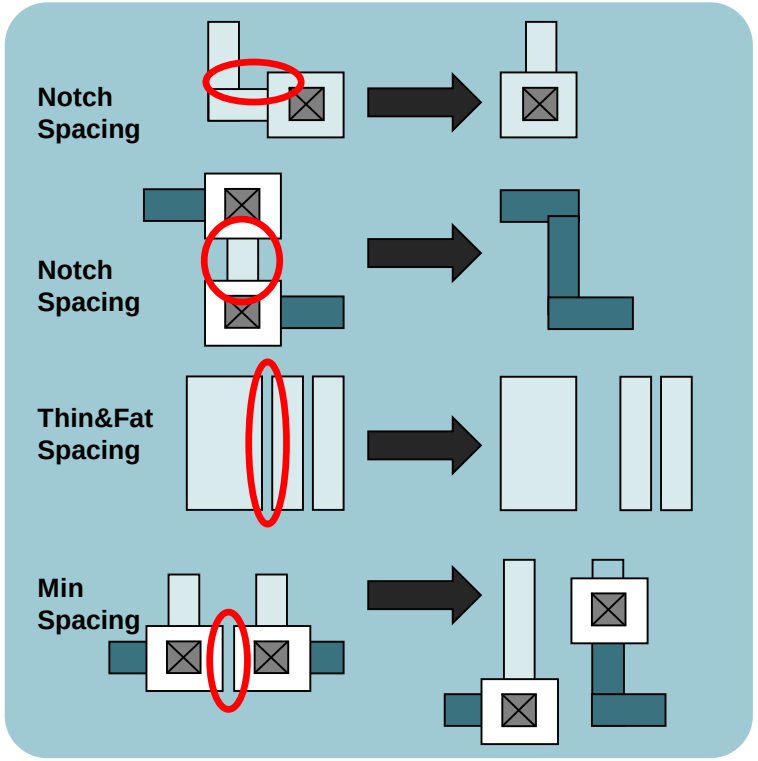
Redundant via doubles the number via
If one of them will not be made chip will still work

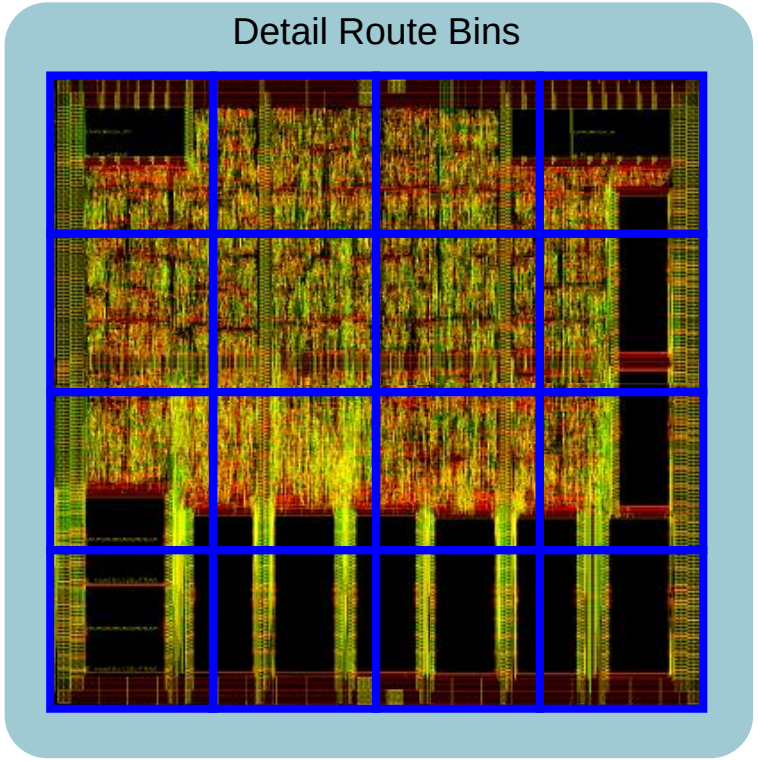


source: Synopsys

Search and Repair

Detail route attempts to clear DRC violations using a fixed size bin

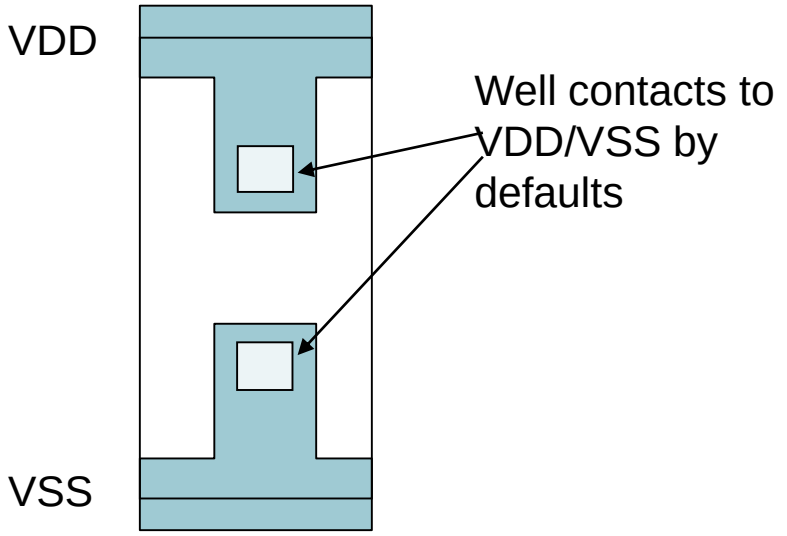




source: Synopsys

Filler Cells

Filler cells are inserted to fill empty places among standard cells



source: Synopsys

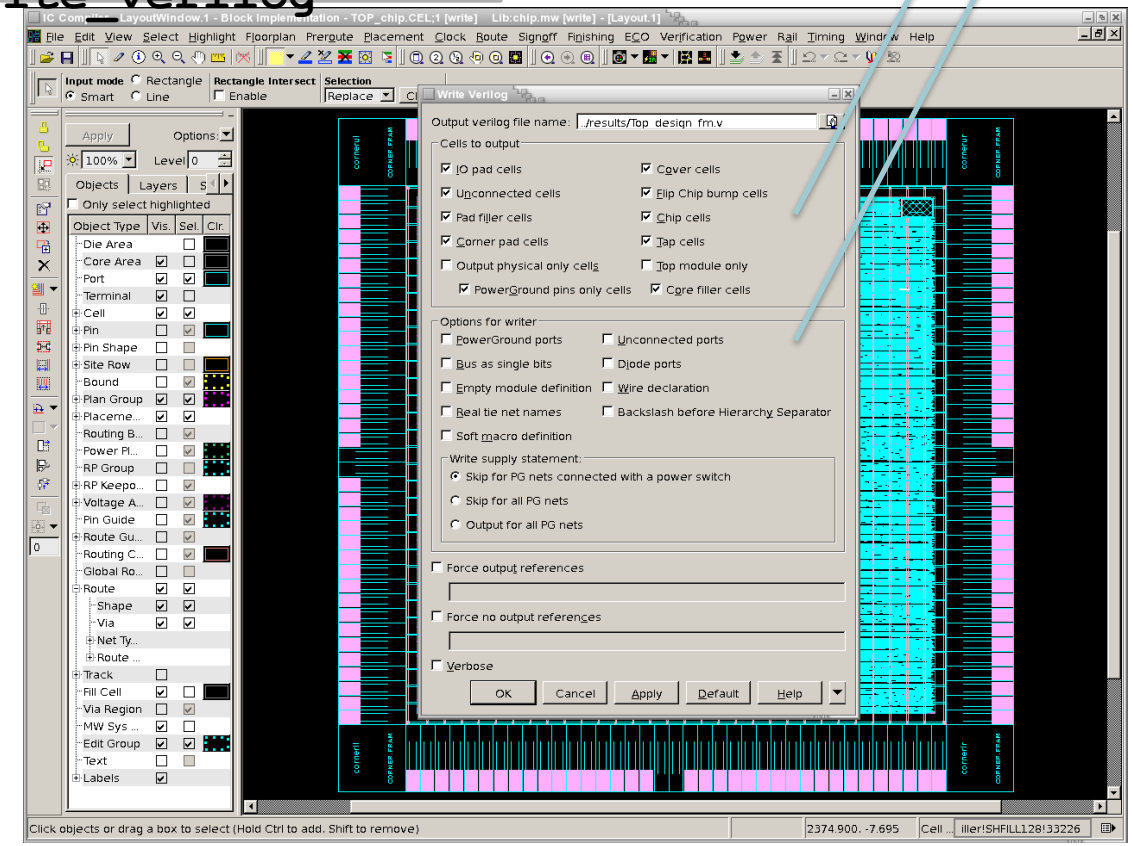
Writing out the netlist

File → Write Verilog

```
icc_shell>
write_verilog
```

Cells to Output

Options for Write

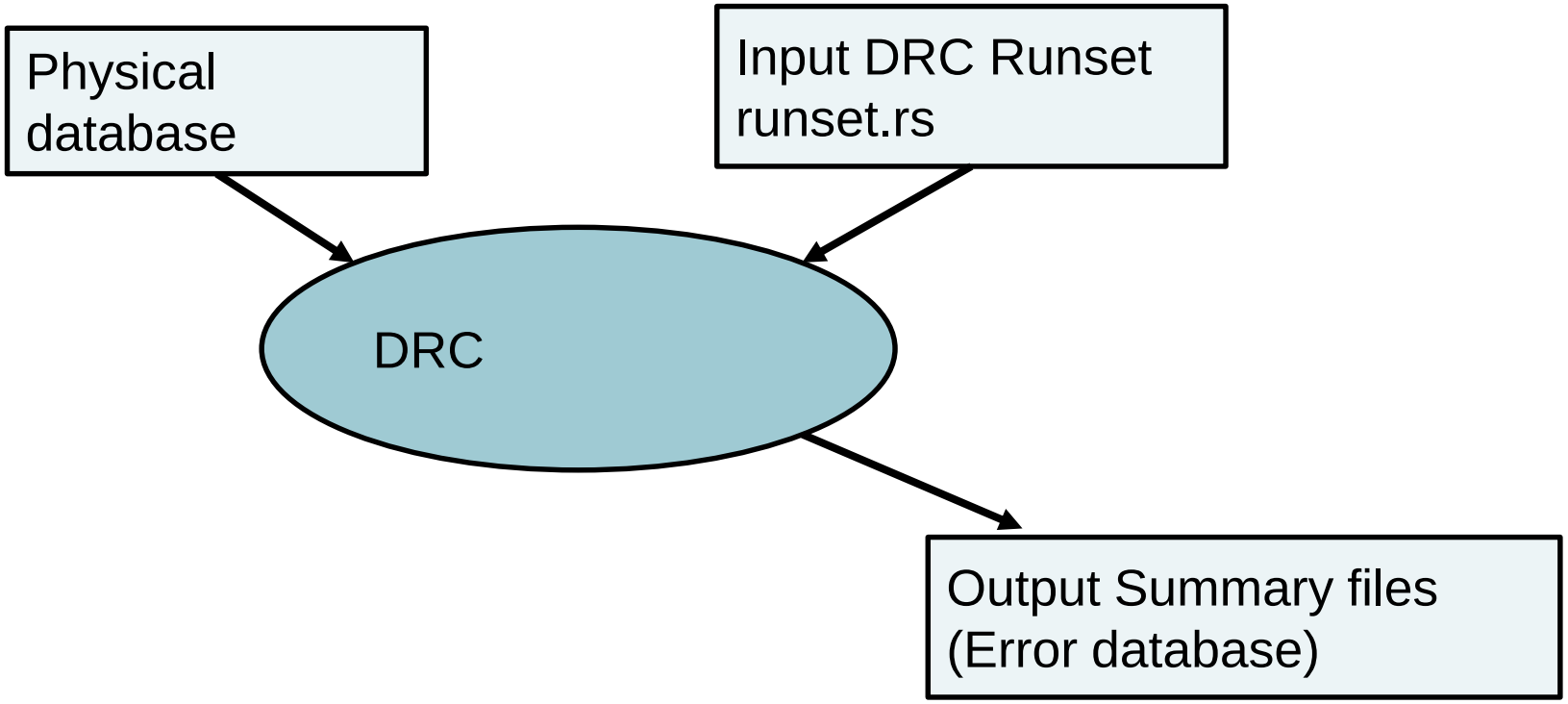


source: Synopsys

Signoff

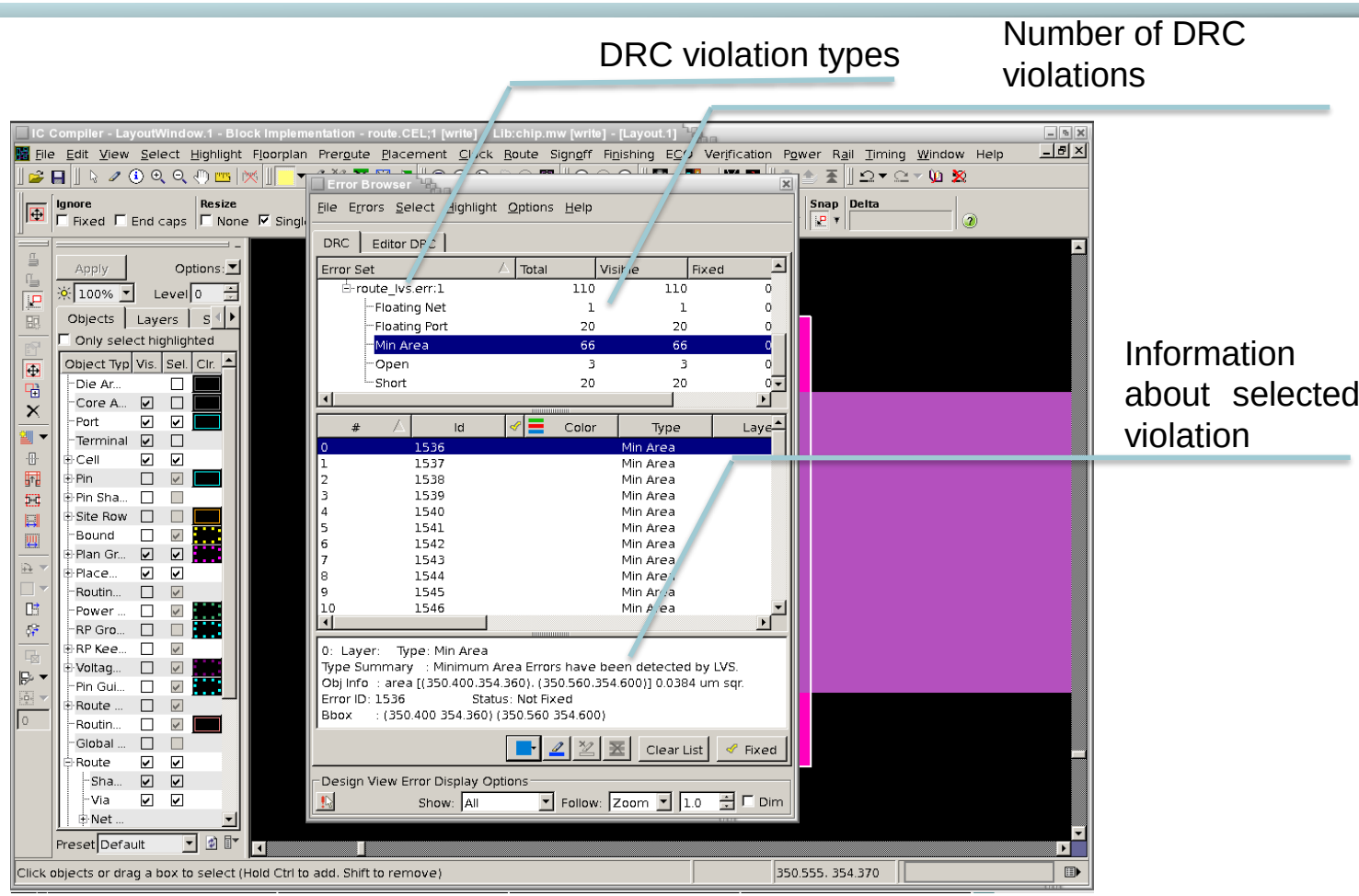
Ready to tape out? Wait…

DRC Flow



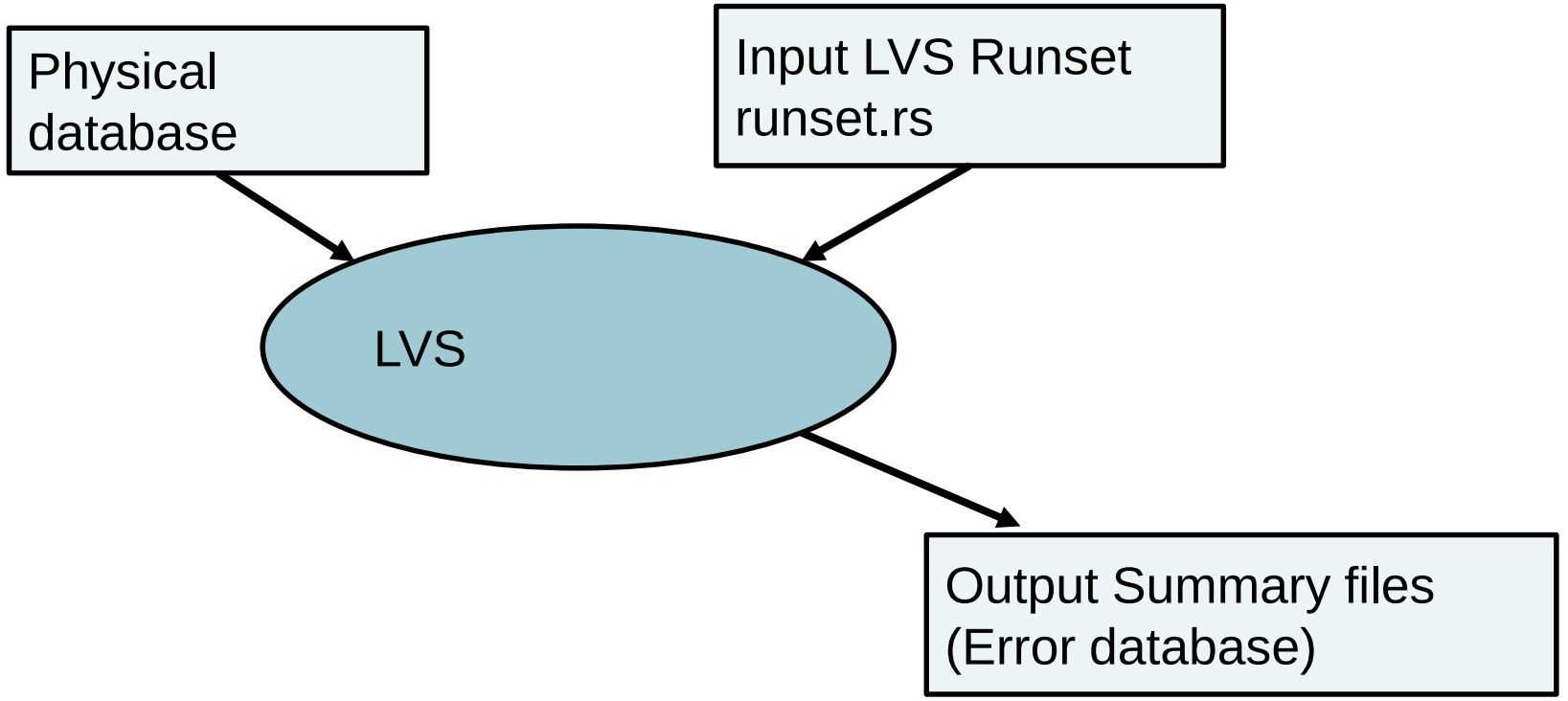
source: Synopsys

DRC Errors Windows



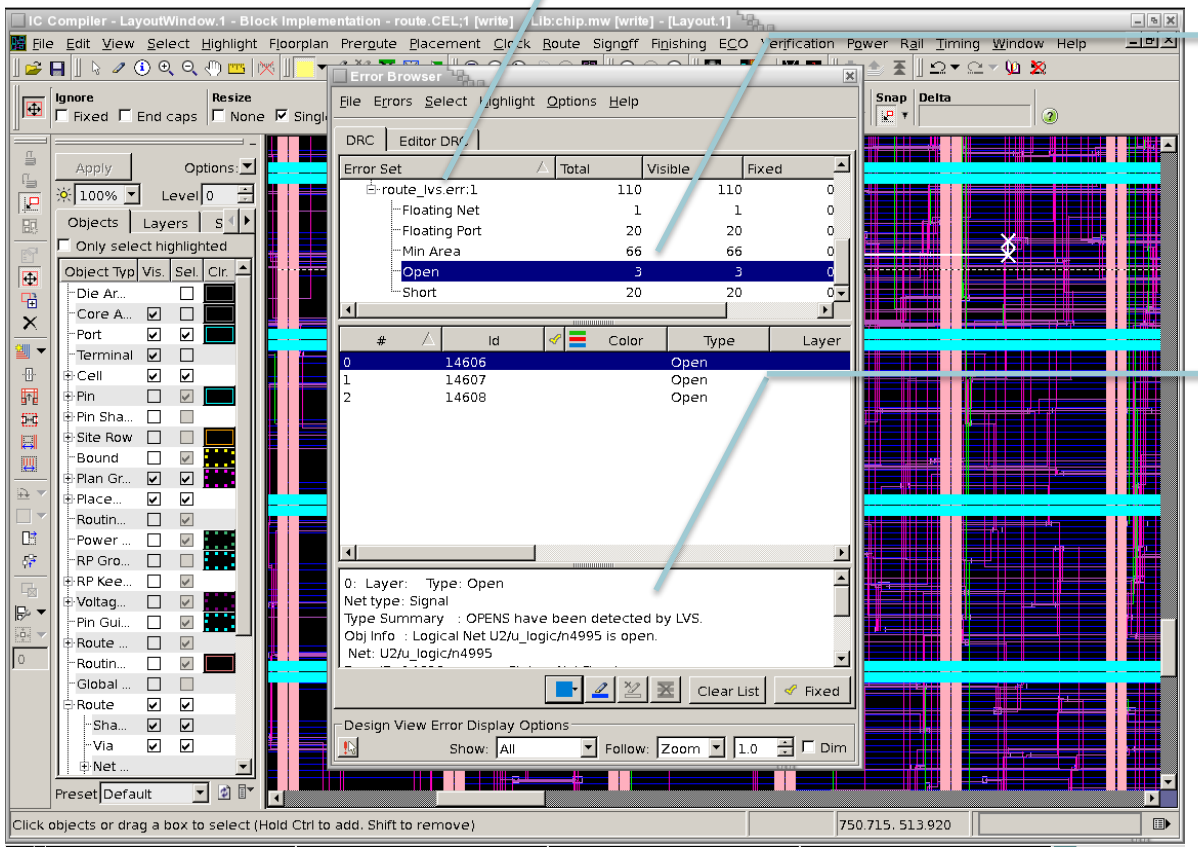
source: Synopsys

Layout Versus Schematic (LVS)



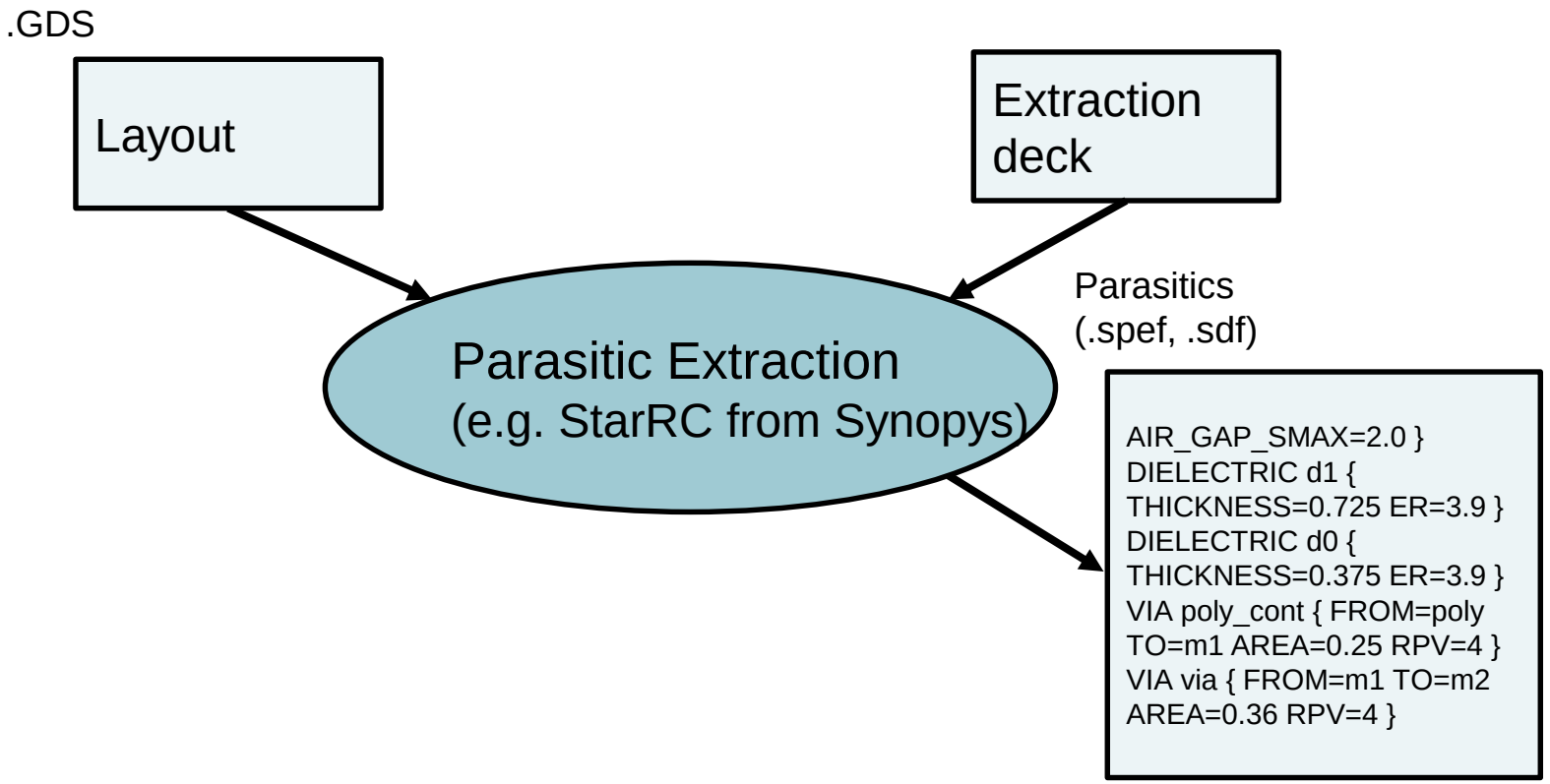
source: Synopsys

LVS Errors Windows



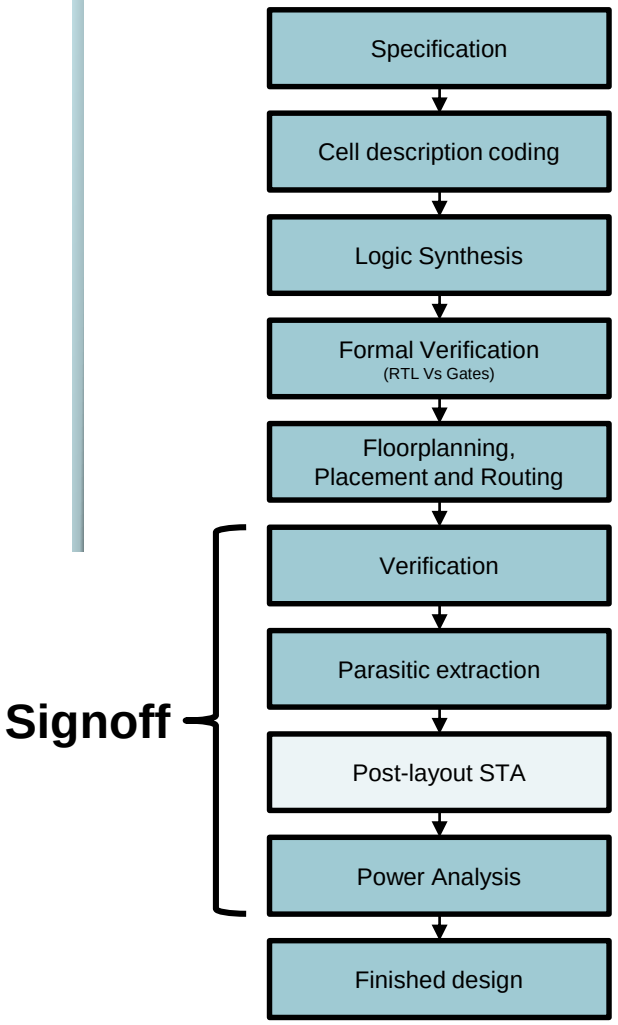
source: Synopsys

Parasitic Extraction



source: Synopsys

Back to the flow

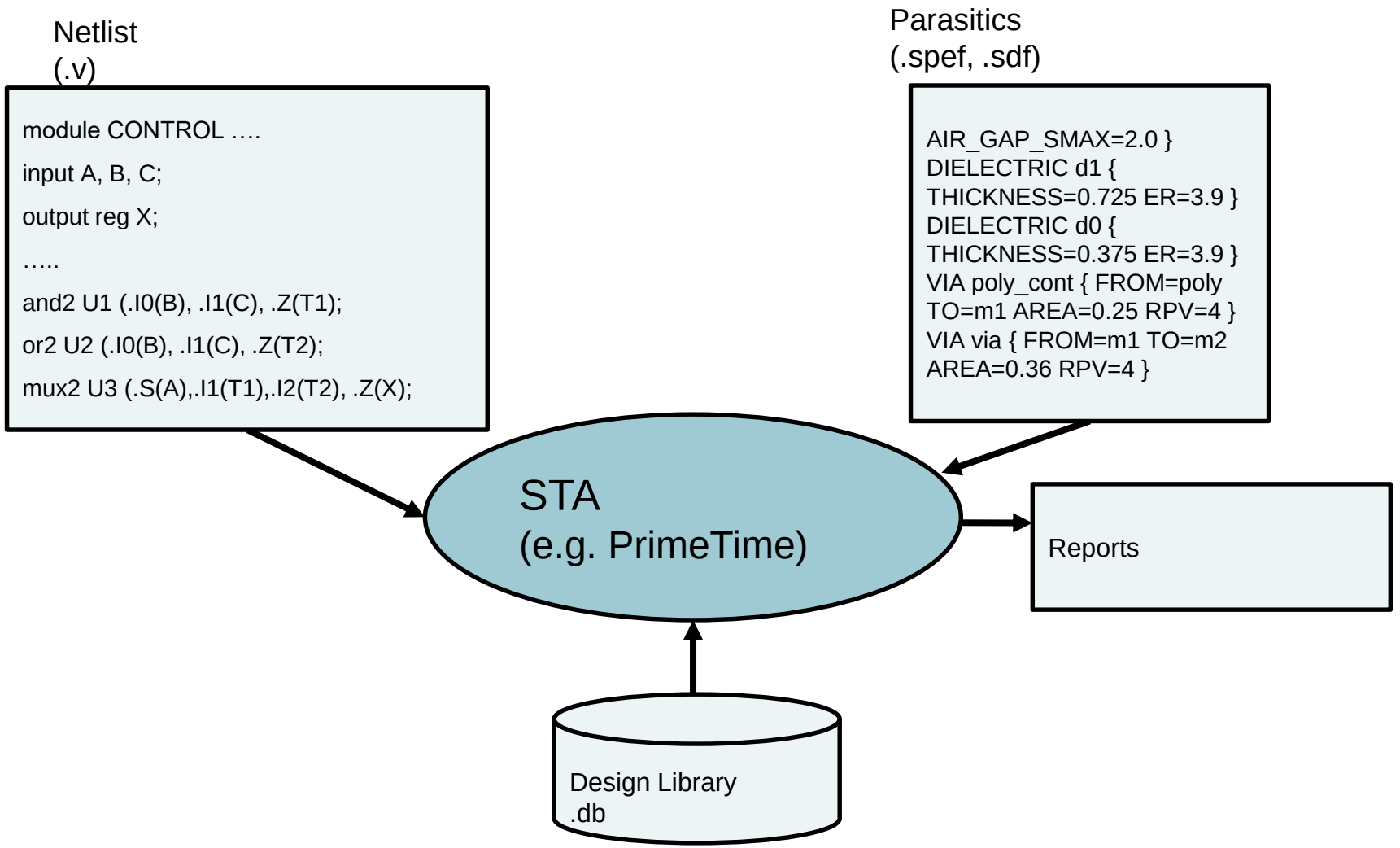


PrimeTime (Synopsys tool) and STA

- PrimeTime is a full-chip, gate-level static timing analysis tool that is an essential part of the design and analysis flow for today's large chip designs
- PrimeTime validates the timing performance of a design by checking all possible paths for timing violations, without using logic simulation or test vectors

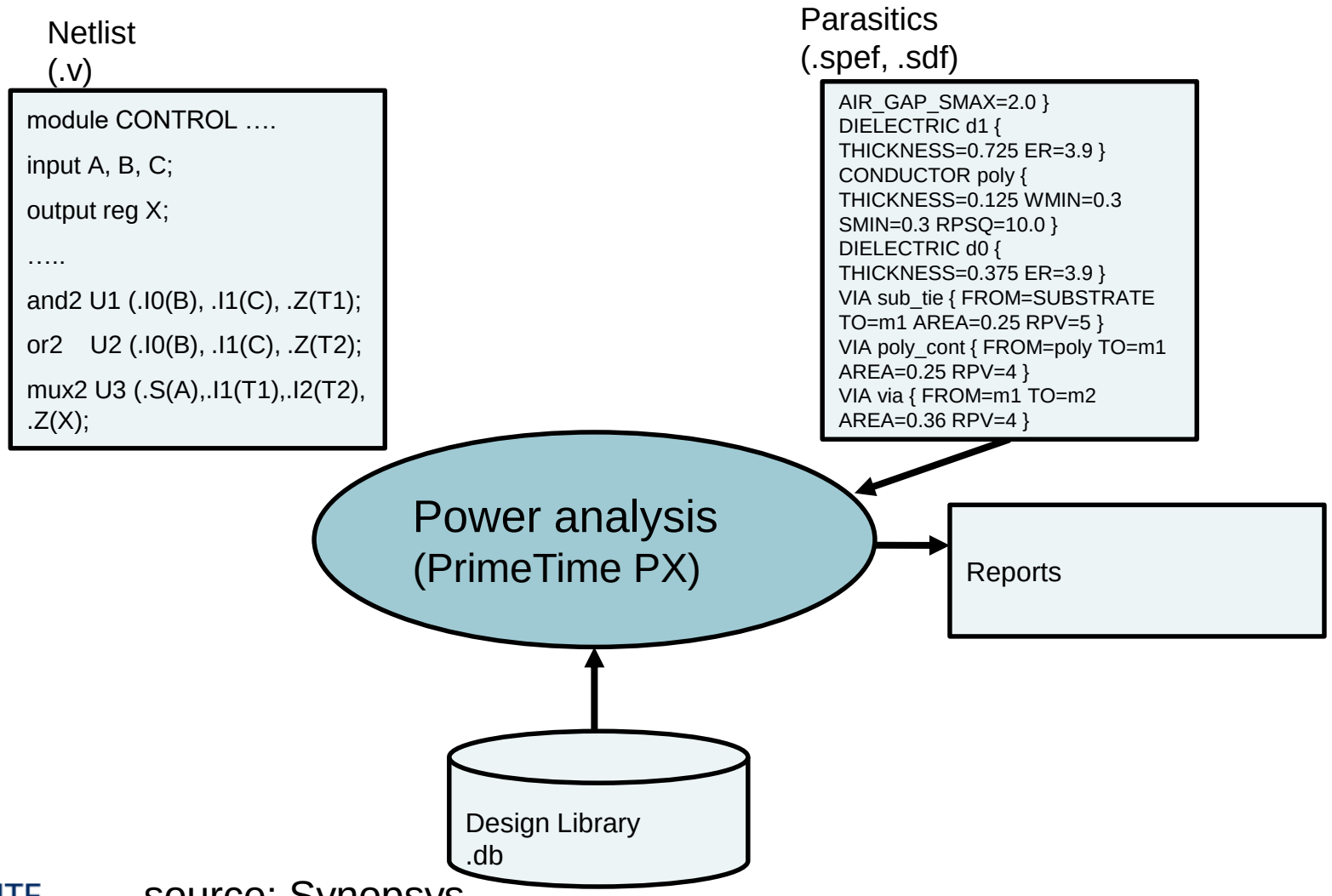
source: Synopsys

STA Flow



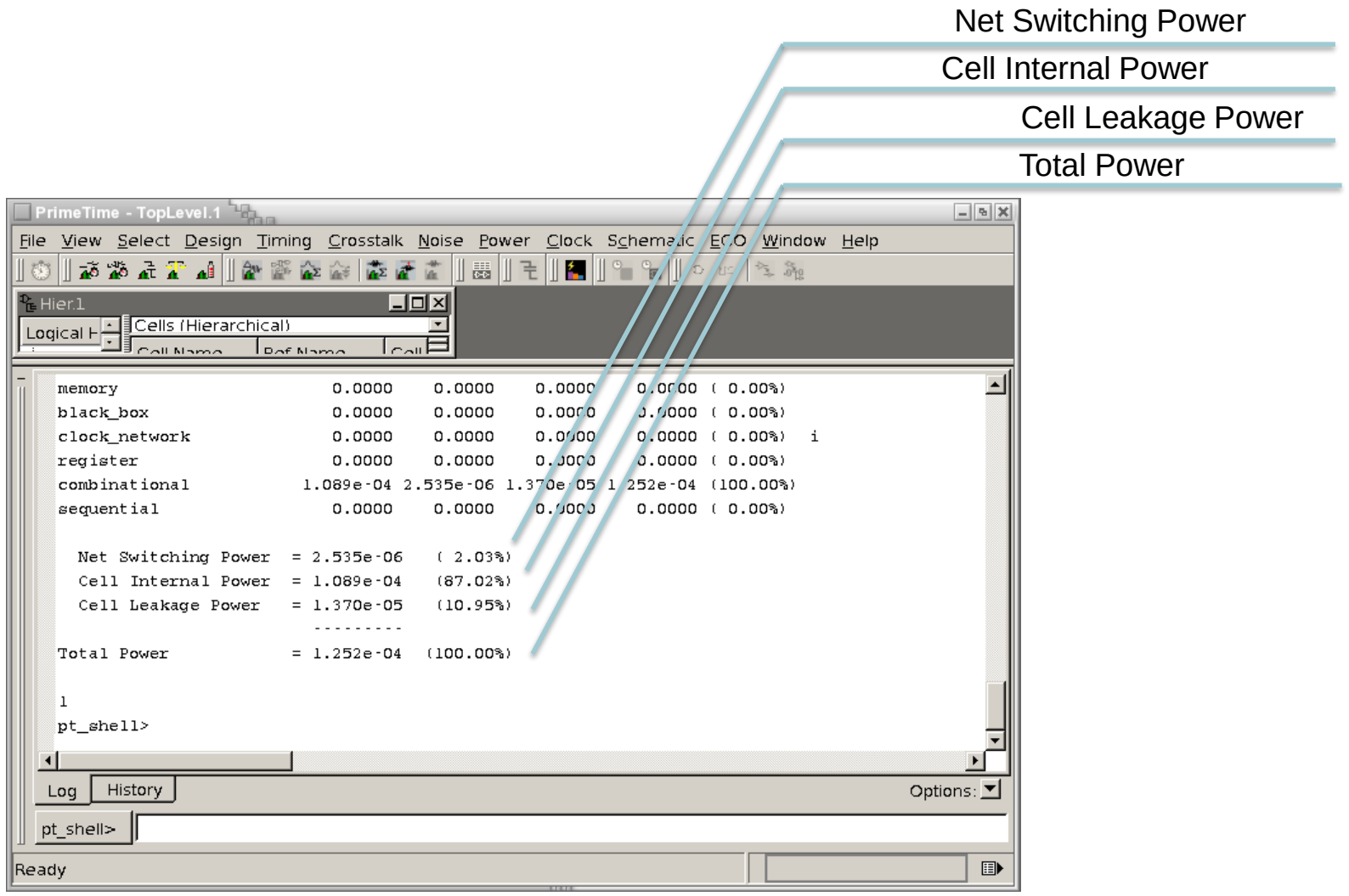
source: Synopsys

Power analysis



source: Synopsys

Report power

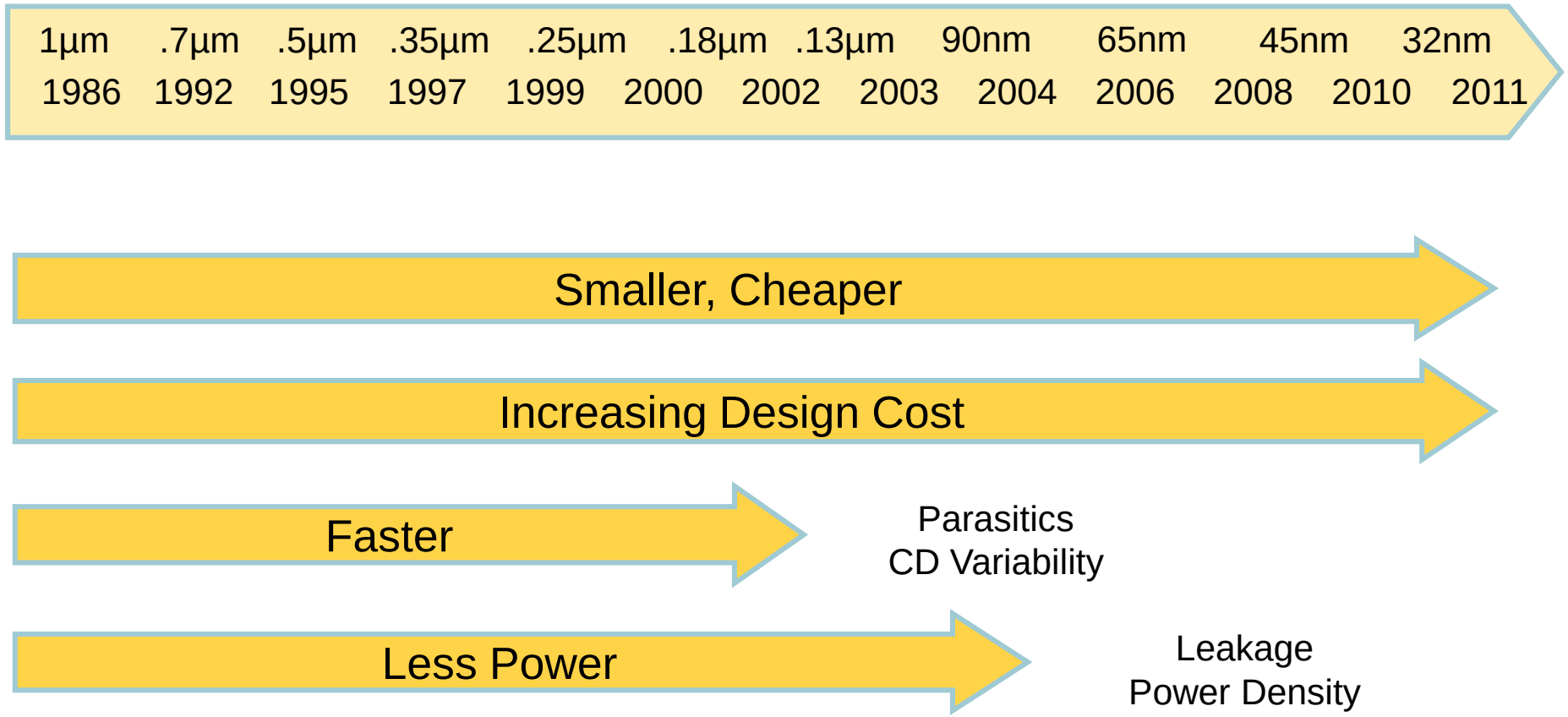


source: Synopsys

Summary

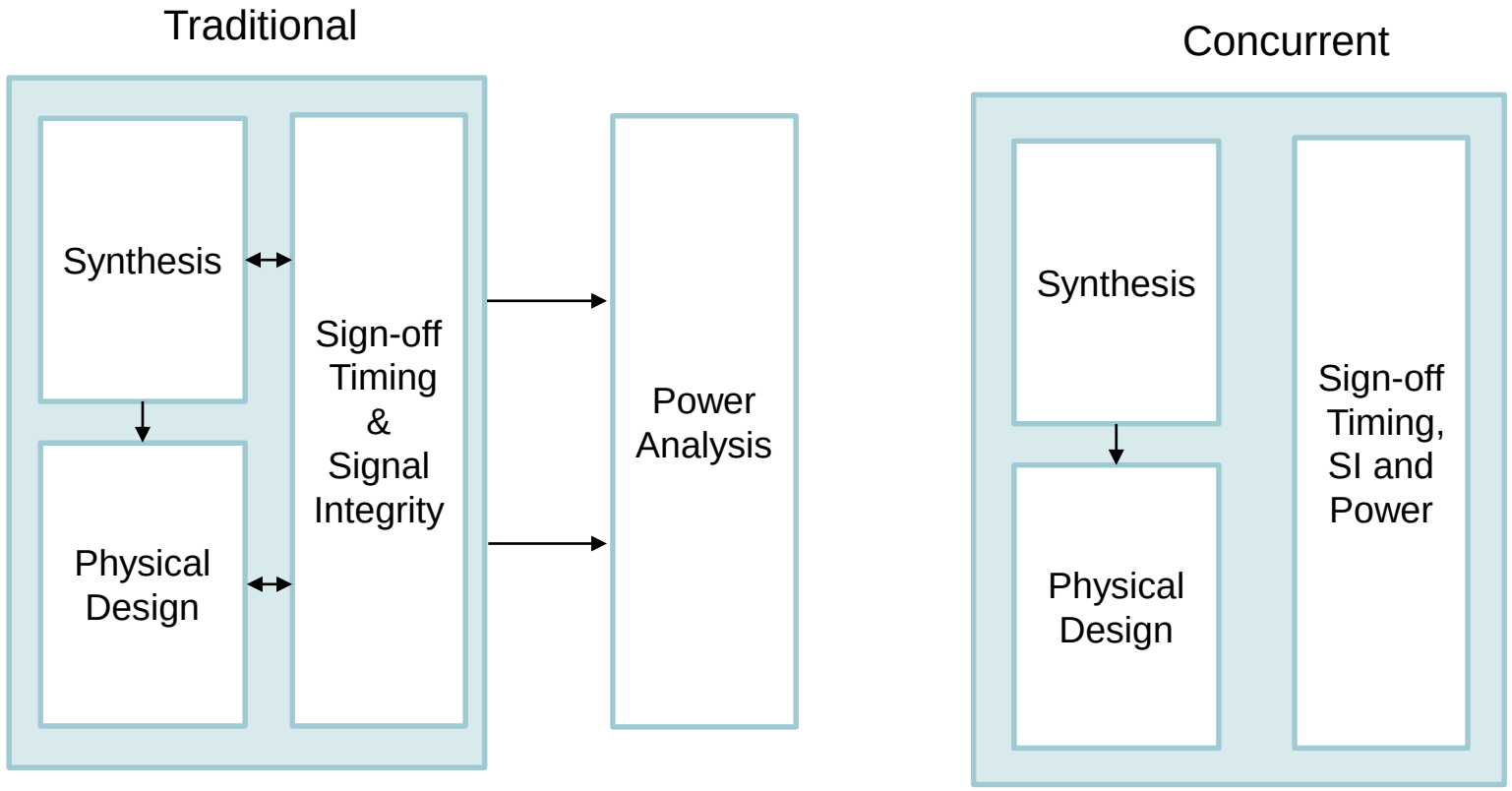
- A full view of how chip design process is done, and what are the considerations of each step
- Chip design flow is VERY complex, everything needs to be scripted up…
- EDA tools are not as intelligent as what you would think
- A lot of design efforts, Human-EDA interfacing
- What are not covered in this lecture
  - Design for test
  - Chip testing
  - Verification
  - Many more…

Challenges start from technology scaling



source: Synopsys

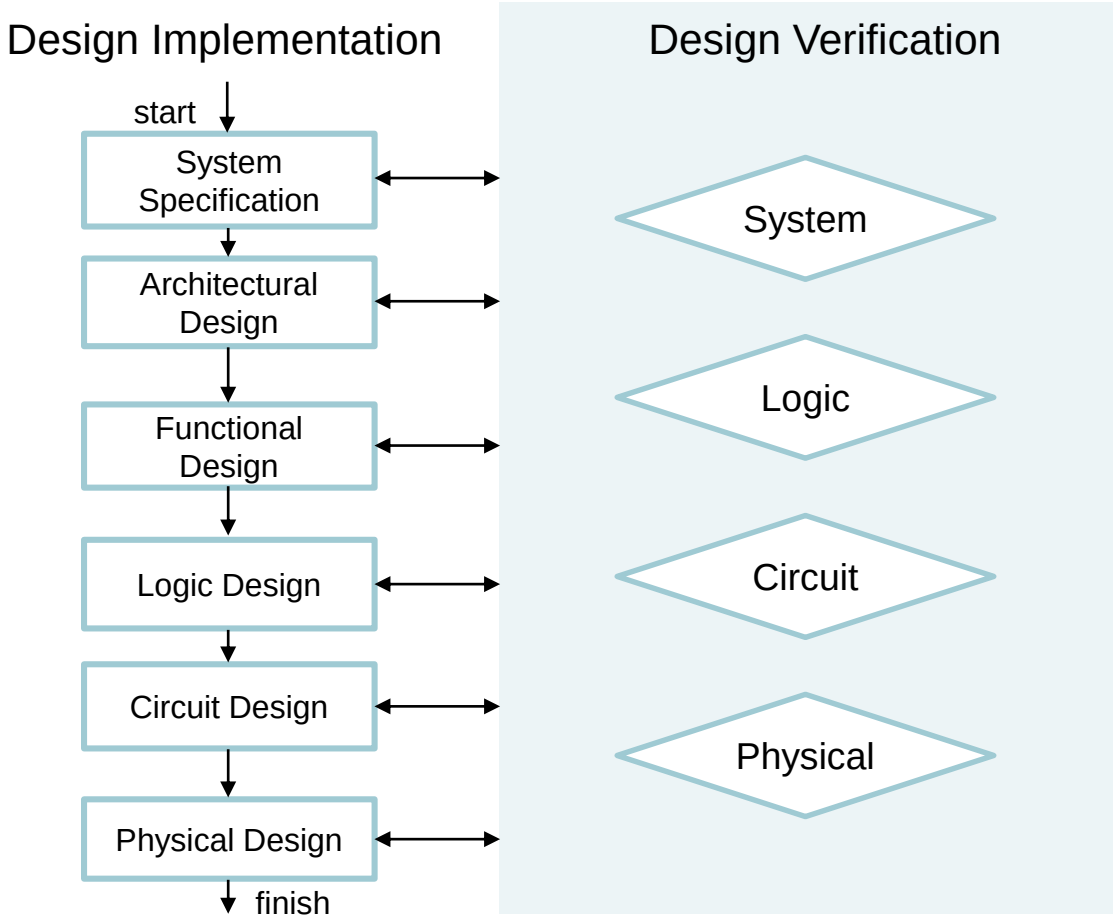
Concurrent Design Methodology



source: Synopsys

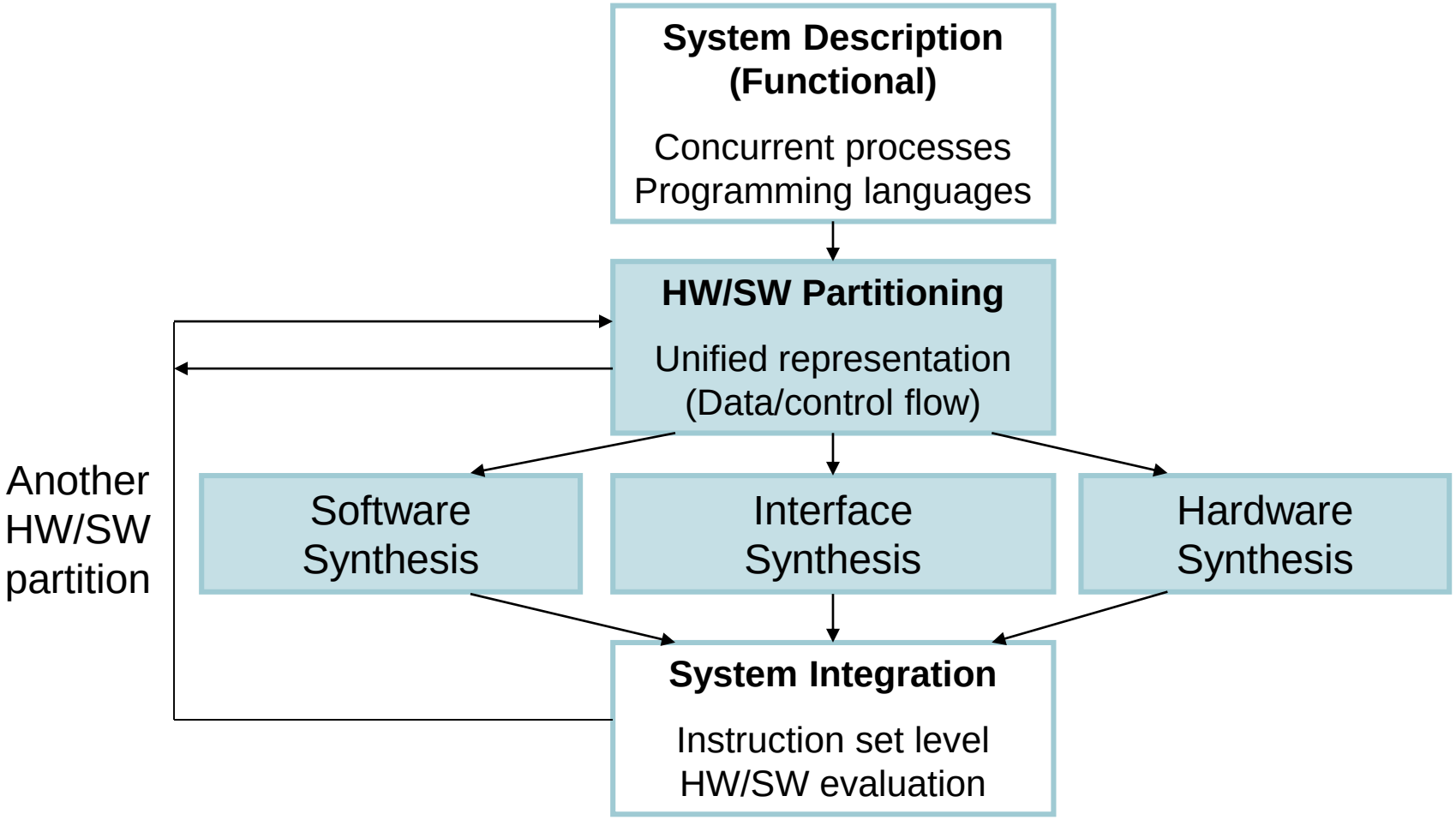
New Challenges in the Design Flow

- Design Challenges
  - IP
  - Timing closure
  - Signal integrity
  - Leakage power
  - Dynamic power
  - Test
  - Yield
  - Printability



source: Synopsys

HW/SW Co-design Flow



source: Synopsys

Where are we Heading?

- Advanced Topics

Action Items

- Final projects – Start ASAP
- Two review assignments

Acknowledgement

Slides in this topic are inspired in part by material developed and copyright by:

- Synopsys Courseware