

SP5140

384 X 128 16 Grayscale Dot Matrix OLED/PLED Driver with Controller

Features

- Support maximum 384 X 128 dot matrix panel with 16 grayscale
- Embedded 384 X 128 X 4bits SRAM
- Operating voltage:
 - I/O and Logic voltage supply: V_{DD} = 1.65V - 3.5V
 - OLED Operating voltage supply: V_{PP} = 8.0V -18V
- Maximum segment output current: 600μA
- Maximum common sink current: 115mA
- 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface, 3 wire/4 wire serial peripheral interface, 400KHZ fast I²C bus interface
- All interfaces support reading ID
- Interface noise process
- Programmable frame frequency and multiplexing ratio
- Horizontal and Vertical scrolling
- Internal or external I_{REF} selection
- Row re-mapping and column re-mapping
- Breathing/ Dimming Display Effect
- Data RAM support mono interface mode
- On-chip oscillator
- 256-step contrast control on monochrome passive OLED panel
- Wide range of operating temperatures: -40 to +85°C
- Available in COG form, thickness: 250μm

General Description

SP5140 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. SP5140 consists of 384 segments, 128 commons with 16 grayscale that can support a maximum display resolution of 384 X 128. It is designed for Common Cathode type OLED panel.

SP5140 embeds with contrast control, display RAM oscillator. SP5140 is suitable for a wide range of household appliances, such as refrigerators, washing machines, microwave ovens and so on.

Block Diagram

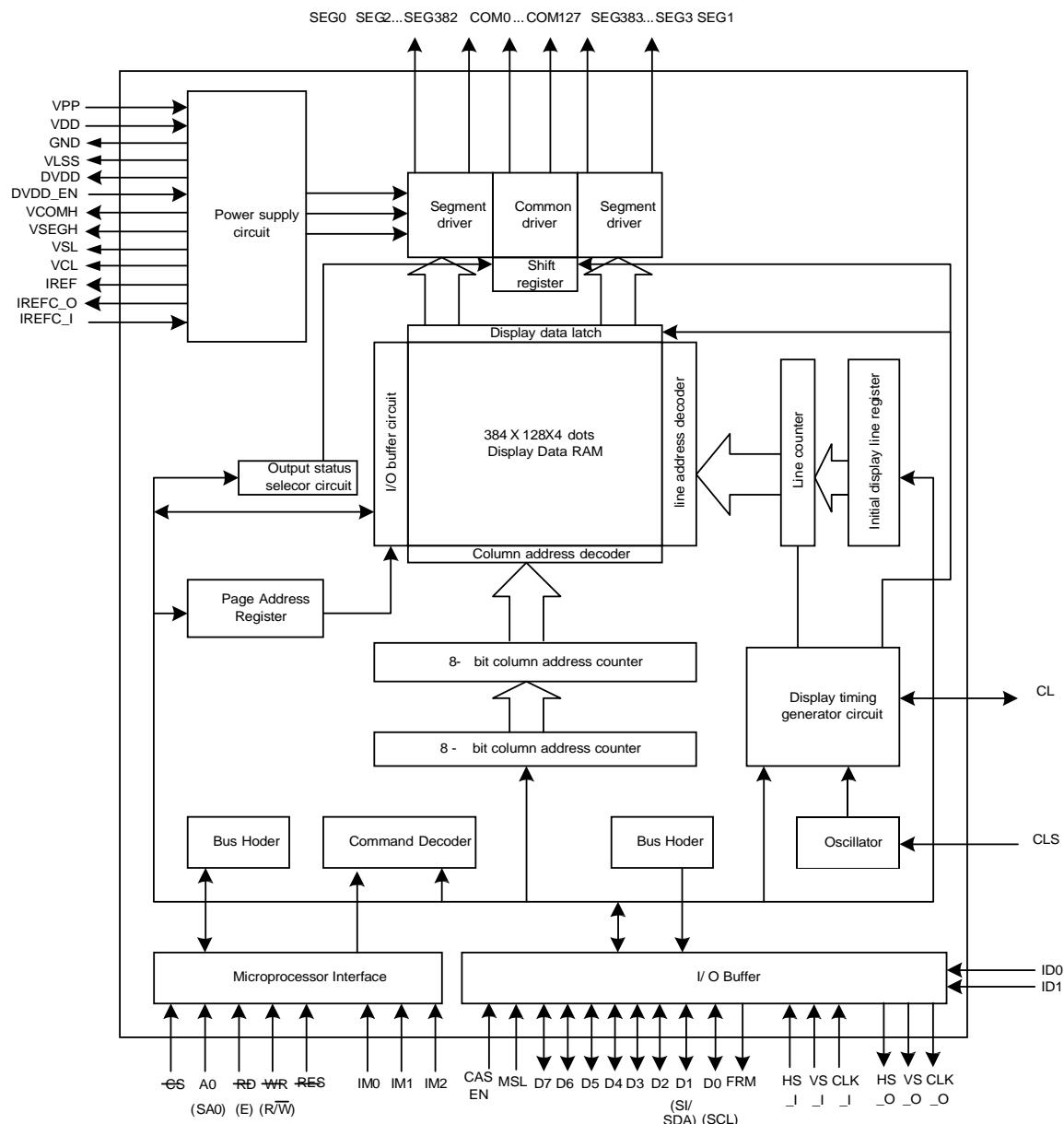


Figure 1 SP5140 Block Diagram

Pad Description**Power Supply**

Pad NO.	Symbol	I/O	Description
14,15,52, 56,102	VDD	Supply	1.65V– 3.6V Power supply for logic and input/output
19-21,54, 58,98-100	GND	Supply	Ground for logic and analog. This pad should be connected to GND externally.
47-50	VLSS	Supply	Ground for VSL regulator. This pad should be connected to GND externally.
12-13	DVDD	Supply	This pin is for regulator circuit. A 4.7uF capacitor should be connected between this pad and GND.
29-32 88-91	VSL	Supply	Discharge voltage level pad. A 4.7uF capacitor should be connected between this pad and GND.
37-42 78-83	VCL	Supply	This is a common voltage reference pad. This pad should be connected to GND externally.
23-28 92-97 119-120 313-320 449-456 649-650	VPP	Supply	This is the most positive voltage supply pad of the chip It should be supplied externally
6-7	VDDF	Supply	Power supply for FUSE circuit. This pad should be Left open.

OLED Driver Supplies

Pad NO.	Symbol	I/O	Description
22	IREF	O	This is a segment current reference pad. A resistor should be connected between this pad and GND.
43-46 74-77	VCOMH	O	This is a pad for the voltage output high level for common signals. A 4.7uF capacitor should be connected between this pad and GND.
33-36 84-87	VSEGH	O	This is a segment pre-charge voltage. A 4.7uF capacitor can be connected between this pad and GND.

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System Bus Connection Pads

Pad No.	Symbol	I/O	Description																								
8	CL	I/O	<p>This pad is the system clock input/output. CLS = "H": The internal clock is output from this pad. CLS = "L": This pad is input and not used. When CLS = "H", this pad should be Left open.</p>																								
51	CLS	I	<p>This is the internal clock enable pad. CLS = "H": Internal oscillator circuit is enabled. CLS = "L": Internal oscillator circuit is disabled (requires external input). When CLS = "L", an external clock source must be connected to the CL pad for normal operation. These pins must be connected to "H" or "L".</p>																								
9	FRM	O	<p>This pad output frame frequency signal. Its voltage is equal to VDD1 when the last common output of every frame is active, and is equal to Vss during other time.</p>																								
53 55 57	IM0 IM1 IM2	I	<p>These are the MPU interface mode select pads.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th></th><th>8080</th><th>I²C</th><th>6800</th><th>4-wire SPI</th><th>3-wire SPI</th></tr> <tr> <td>IM0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr> <tr> <td>IM1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr> <tr> <td>IM2</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr> </table> <p>These pins must be connected to "H" or "L".</p>		8080	I ² C	6800	4-wire SPI	3-wire SPI	IM0	0	0	0	0	1	IM1	1	1	0	0	0	IM2	1	0	1	0	0
	8080	I ² C	6800	4-wire SPI	3-wire SPI																						
IM0	0	0	0	0	1																						
IM1	1	1	0	0	0																						
IM2	1	0	1	0	0																						
59	CS	I	<p>This pad is the chip select input. \overline{CS} = "H", then the chip select becomes inactive, and data/command I/O is disabled. \overline{CS} = "L", then the chip select becomes active, and data/command I/O is enabled. These pins must be connected to "H" or "L".</p>																								
60	RES	I	<p>This is a reset signal input pad. \overline{RES} = "H", the settings are not initialized. \overline{RES} = "L", the settings are initialized. The reset operation is performed by the \overline{RES} signal level. These pins must be connected to "H" or "L".</p>																								
61	A0 (SA0)	I	<p>This is the Data/Command control pad that determines whether the byte is a data or command. A0 = "H": the inputs at D0 to D7 are treated as display data. A0 = "L": the inputs at D0 to D7 are transferred to the command registers. In I²C interface, this pad serves as SA0 to distinguish the slave address of OLED driver. These pins must be connected to "H" or "L".</p>																								
62	\overline{WR} (R/W)	I	<p>This is a MPU interface input pad. When connected to an 8080 MPU, this is active LOW. This pad connects to the 8080 MPU \overline{WR} signal. The signals on the data bus are latched at the rising edge of the \overline{WR} signal. When connected to a 6800 Series MPU: This is the read/write control signal input terminal. $R/W = "H"$: Read. $R/W = "L"$: Write. These pins must be connected to "H" or "L".</p>																								
63	\overline{RD} (E)	I	<p>This is a MPU interface input pad. When connected to an 8080 series MPU, it is active LOW. This pad is connected to the \overline{RD} signal of the 8080 series MPU, and the SP5140 data bus is in an output status when this signal is "L". When connected to a 6800 series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU. These pins must be connected to "H" or "L".</p>																								

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66-73	D[0] – D[7] (SCL) (SI /SDA) (SO)	I/O II	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SI). When reading, D2 can be select as data output pad. D2(3) to D7 are set to high impedance. When the I ₂ C interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SDA). At this time, D2 to D7 are set to high impedance.															
10 11	ID0 ID1	I	These pins are Panel ID setting for customers use. Customers can connect these pins to H or L through read register E1h to confirm which panel and send corresponding initial code. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th></th><th>Panel ID1</th><th>Panel ID2</th><th>Panel ID3</th><th>Panel ID4</th></tr> <tr> <td>ID0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr> <td>ID1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> </table> This pin must be connected to "H" or "L".		Panel ID1	Panel ID2	Panel ID3	Panel ID4	ID0	0	0	1	1	ID1	0	1	0	1
	Panel ID1	Panel ID2	Panel ID3	Panel ID4														
ID0	0	0	1	1														
ID1	0	1	0	1														
18	DVDD _EN	I	When VDD >1.98V, this pin should be connected to "H" to turn on regulator for digital circuit. The relation between DVDD_EN hardware pin and DVDD regulator off command is as below: <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>DVDD_EN Hardware pin</th><th>DVDD regulator off Command</th><th>Result</th></tr> </thead> <tbody> <tr> <td>0</td><td>0 (5A.A5.AA)</td><td>0 (Regulator OFF)</td></tr> <tr> <td>0</td><td>1 (RESET)</td><td>0 (Regulator OFF)</td></tr> <tr> <td>1</td><td>0 (5A.A5.AA)</td><td>0 (Regulator OFF)</td></tr> <tr> <td>1</td><td>1 (RESET)</td><td>1 (Regulator ON)</td></tr> </tbody> </table> This pin must be connected to "H" or "L".	DVDD_EN Hardware pin	DVDD regulator off Command	Result	0	0 (5A.A5.AA)	0 (Regulator OFF)	0	1 (RESET)	0 (Regulator OFF)	1	0 (5A.A5.AA)	0 (Regulator OFF)	1	1 (RESET)	1 (Regulator ON)
DVDD_EN Hardware pin	DVDD regulator off Command	Result																
0	0 (5A.A5.AA)	0 (Regulator OFF)																
0	1 (RESET)	0 (Regulator OFF)																
1	0 (5A.A5.AA)	0 (Regulator OFF)																
1	1 (RESET)	1 (Regulator ON)																
101	CASEN	I	Cascade enable bit. CASEN="H": Cascade is enable. CASEN="L": Cascade is disable. This pin must be connected to "H" or "L".															
103	MSL	I	This pin sets master or slave. When MSL="H", it is a Master IC. When MSL="L", it is a Slave IC. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>MSL</th><th>Mode</th></tr> <tr> <td>0</td><td>Slave</td></tr> <tr> <td>1</td><td>Master</td></tr> </table> CASEN="L": This pad is pulled high in IC.	MSL	Mode	0	Slave	1	Master									
MSL	Mode																	
0	Slave																	
1	Master																	
5	IREFC_I	I	Slave : This pad input master' IREF current. CASEN="L": This pad is Hz.															
114	IREFC_O	O	Master : This pad output IREF current. CASEN="L": This pad is Hz.															
116	HS_I	I	Horizontal synchronous signal for cascade slave IC. CASEN="L": This pad is pulled low in IC, no connection for user.															
4	VS_I	I	Vertical synchronous signal for cascade slave IC. CASEN="L": This pad is pulled low in IC, no connection for user.															
117	CLK_I	I	Clock synchronous signal for cascade slave IC. CASEN="L": This pad is pulled low in IC, no connection for user.															

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3	HS_O	O	Hsync synchronous signal output for cascade mode master IC. CASEN="L": This pad output low, no connection for user.
115	VS_O	O	Vsync synchronous signal for cascade mode master IC. CASEN="L": This pad output low, no connection for user.
2	CLK_O	O	CLK synchronous signal for cascade mode master IC. CASEN="L": This pad output low, no connection for user.

OLED Drive Pads

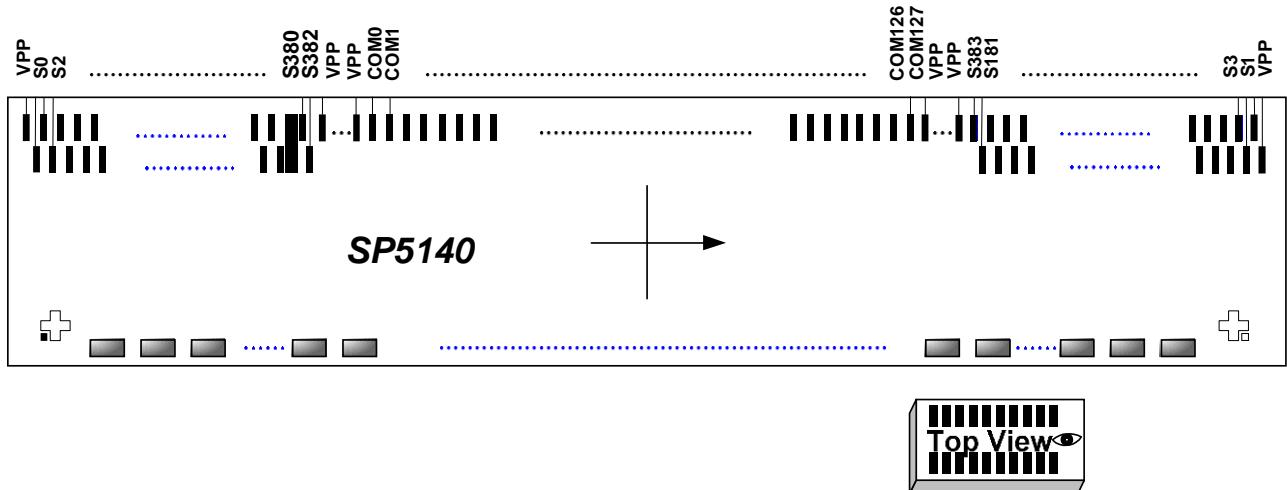
Pad No.	Symbol	I/O	Description
121~312	SEG1,3 - 383	O	These pads are odd Segment signal output for OLED display.
321~448	COM127 - 0	O	These pads are Common signal output for OLED display.
457~648	SEG382 - 2,0	O	These pads are even Segment signal output for OLED display.

Test Pads

Pad No.	Symbol	I/O	Description
104	TEST1	I	Test pads, no connection for user.
105	TEST2	I	Test pads, no connection for user.
106	TESTO[0]	O	Test pads, no connection for user.
107	TESTO[1]	O	Test pads, no connection for user.
108	TESTO[2]	O	Test pads, no connection for user.
109	TESTO[3]	O	Test pads, no connection for user.
110	TESOT[4]	O	Test pads, no connection for user.
111	TESTO[5]	O	Test pads, no connection for user.
112	TESTO[6]	O	Test pads, no connection for user.
113	TESTO[7]	O	Test pads, no connection for user.
16	TEST_AOV	O	Test pads, no connection for user.
17	TEST_AOI	O	Test pads, no connection for user.
1	Dummy1	-	NC pads, no connection for user.
64-65	Dummy2	-	NC pads, no connection for user. Note: Two dummy internal short.
118	Dummy3	-	NC pads, no connection for user.

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Pad Configuration

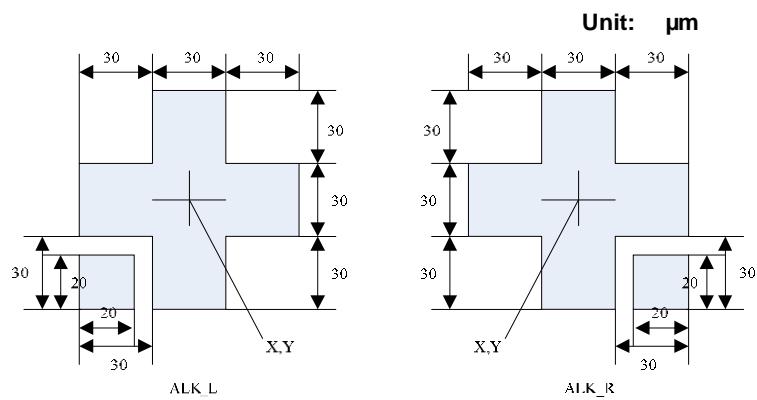


Chip Outline Dimensions

Item	Pad No.	Size (μm)	
		X	Y
Chip boundary	-	14679	862
Chip height	All pads	300	
Bump size	I/O	100	40
	SEG	14	110
	COM	20	110
Pad pitch	COM	35	
	SEG	49	
	I/O	120	
Bump height	All pads	9±2	

Alignment Mark Location

NO	X	Y
ALK_L	-7215.5	-307
ALK_R	7215.5	-307



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Pad Location (Total: 650 pads)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	DUMMY1	-7020	-350	71	D[5]	1380	-350	141	SEG[41]	6729	314	211	SEG[181]	5014	314
2	CLK_O	-6900	-350	72	D[6]	1500	-350	142	SEG[43]	6704.5	174	212	SEG[183]	4989.5	174
3	HS_O	-6780	-350	73	D[7]	1620	-350	143	SEG[45]	6680	314	213	SEG[185]	4965	314
4	VS_I	-6660	-350	74	VCOMH	1740	-350	144	SEG[47]	6655.5	174	214	SEG[187]	4940.5	174
5	IREFC_I	-6540	-350	75	VCOMH	1860	-350	145	SEG[49]	6631	314	215	SEG[189]	4916	314
6	VDDF	-6420	-350	76	VCOMH	1980	-350	146	SEG[51]	6606.5	174	216	SEG[191]	4891.5	174
7	VDDF	-6300	-350	77	VCOMH	2100	-350	147	SEG[53]	6582	314	217	SEG[193]	4867	314
8	CL	-6180	-350	78	VCL	2220	-350	148	SEG[55]	6557.5	174	218	SEG[195]	4842.5	174
9	FRM	-6060	-350	79	VCL	2340	-350	149	SEG[57]	6533	314	219	SEG[197]	4818	314
10	ID0	-5940	-350	80	VCL	2460	-350	150	SEG[59]	6508.5	174	220	SEG[199]	4793.5	174
11	ID1	-5820	-350	81	VCL	2580	-350	151	SEG[61]	6484	314	221	SEG[201]	4769	314
12	DVDD	-5700	-350	82	VCL	2700	-350	152	SEG[63]	6459.5	174	222	SEG[203]	4744.5	174
13	DVDD	-5580	-350	83	VCL	2820	-350	153	SEG[65]	6435	314	223	SEG[205]	4720	314
14	VDD	-5460	-350	84	VSEGH	2940	-350	154	SEG[67]	6410.5	174	224	SEG[207]	4695.5	174
15	VDD	-5340	-350	85	VSEGH	3060	-350	155	SEG[69]	6386	314	225	SEG[209]	4671	314
16	TEST_AOV	-5220	-350	86	VSEGH	3180	-350	156	SEG[71]	6361.5	174	226	SEG[211]	4646.5	174
17	TEST_AOI	-5100	-350	87	VSEGH	3300	-350	157	SEG[73]	6337	314	227	SEG[213]	4622	314
18	DVDD_EN	-4980	-350	88	VSL	3420	-350	158	SEG[75]	6312.5	174	228	SEG[215]	4597.5	174
19	GND	-4860	-350	89	VSL	3540	-350	159	SEG[77]	6288	314	229	SEG[217]	4573	314
20	GND	-4740	-350	90	VSL	3660	-350	160	SEG[79]	6263.5	174	230	SEG[219]	4548.5	174
21	GND	-4620	-350	91	VSL	3780	-350	161	SEG[81]	6239	314	231	SEG[221]	4524	314
22	IREF	-4500	-350	92	VPP	3900	-350	162	SEG[83]	6214.5	174	232	SEG[223]	4499.5	174
23	VPP	-4380	-350	93	VPP	4020	-350	163	SEG[85]	6190	314	233	SEG[225]	4475	314
24	VPP	-4260	-350	94	VPP	4140	-350	164	SEG[87]	6165.5	174	234	SEG[227]	4450.5	174
25	VPP	-4140	-350	95	VPP	4260	-350	165	SEG[89]	6141	314	235	SEG[229]	4426	314
26	VPP	-4020	-350	96	VPP	4380	-350	166	SEG[91]	6116.5	174	236	SEG[231]	4401.5	174
27	VPP	-3900	-350	97	VPP	4500	-350	167	SEG[93]	6092	314	237	SEG[233]	4377	314
28	VPP	-3780	-350	98	VSS	4620	-350	168	SEG[95]	6067.5	174	238	SEG[235]	4352.5	174
29	VSL	-3660	-350	99	VSS	4740	-350	169	SEG[97]	6043	314	239	SEG[237]	4328	314
30	VSL	-3540	-350	100	VSS	4860	-350	170	SEG[99]	6018.5	174	240	SEG[239]	4303.5	174
31	VSL	-3420	-350	101	CASEN	4980	-350	171	SEG[101]	5994	314	241	SEG[241]	4279	314
32	VSL	-3300	-350	102	VDD	5100	-350	172	SEG[103]	5969.5	174	242	SEG[243]	4254.5	174
33	VSEGH	-3180	-350	103	MSL	5220	-350	173	SEG[105]	5945	314	243	SEG[245]	4230	314
34	VSEGH	-3060	-350	104	TEST1	5340	-350	174	SEG[107]	5920.5	174	244	SEG[247]	4205.5	174
35	VSEGH	-2940	-350	105	TEST2	5460	-350	175	SEG[109]	5896	314	245	SEG[249]	4181	314
36	VSEGH	-2820	-350	106	TESTO[0]	5580	-350	176	SEG[111]	5871.5	174	246	SEG[251]	4156.5	174
37	VCL	-2700	-350	107	TESTO[1]	5700	-350	177	SEG[113]	5847	314	247	SEG[253]	4132	314
38	VCL	-2580	-350	108	TESTO[2]	5820	-350	178	SEG[115]	5822.5	174	248	SEG[255]	4107.5	174
39	VCL	-2460	-350	109	TESTO[3]	5940	-350	179	SEG[117]	5798	314	249	SEG[257]	4083	314
40	VSL	-2340	-350	110	TESTO[4]	6060	-350	180	SEG[119]	5773.5	174	250	SEG[259]	4058.5	174
41	VCL	-2220	-350	111	TESTO[5]	6180	-350	181	SEG[121]	5749	314	251	SEG[261]	4034	314
42	VCL	-2100	-350	112	TESTO[6]	6300	-350	182	SEG[123]	5724.5	174	252	SEG[263]	4009.5	174
43	VCOMH	-1980	-350	113	TESTO[7]	6420	-350	183	SEG[125]	5700	314	253	SEG[265]	3985	314
44	VCOMH	-1860	-350	114	IREFC_O	6540	-350	184	SEG[127]	5675.5	174	254	SEG[267]	3960.5	174
45	VCOMH	-1740	-350	115	VS_O	6660	-350	185	SEG[129]	5651	314	255	SEG[269]	3936	314
46	VCOMH	-1620	-350	116	HS_I	6780	-350	186	SEG[131]	5626.5	174	256	SEG[271]	3911.5	174
47	VLSS	-1500	-350	117	CLK_I	6900	-350	187	SEG[133]	5602	314	257	SEG[273]	3887	314
48	VLSS	-1380	-350	118	DUMMY3	7020	-350	188	SEG[135]	5577.5	174	258	SEG[275]	3862.5	174
49	VLSS	-1260	-350	119	VPP	7268	174	189	SEG[137]	5553	314	259	SEG[277]	3838	314
50	VLSS	-1140	-350	120	VPP	7243.5	314	190	SEG[139]	5528.5	174	260	SEG[279]	3813.5	174
51	CLS	-1020	-350	121	SEG[1]	7219	314	191	SEG[141]	5504	314	261	SEG[281]	3789	314
52	VDD	-900	-350	122	SEG[3]	7194.5	174	192	SEG[143]	5479.5	174	262	SEG[283]	3764.5	174
53	IM0	-780	-350	123	SEG[5]	7170	314	193	SEG[145]	5455	314	263	SEG[285]	3740	314
54	VSS	-660	-350	124	SEG[7]	7145.5	174	194	SEG[147]	5430.5	174	264	SEG[287]	3715.5	174
55	IM1	-540	-350	125	SEG[9]	7121	314	195	SEG[149]	5406	314	265	SEG[289]	3691	314
56	VDD	-420	-350	126	SEG[11]	7096.5	174	196	SEG[151]	5381.5	174	266	SEG[291]	3666.5	174
57	IM2	-300	-350	127	SEG[13]	7072	314	197	SEG[153]	5357	314	267	SEG[293]	3642	314
58	VSS	-180	-350	128	SEG[15]	7047.5	174	198	SEG[155]	5332.5	174	268	SEG[295]	3617.5	174
59	CSB	-60	-350	129	SEG[17]	7023	314	199	SEG[157]	5308	314	269	SEG[297]	3593	314
60	RESB	60	-350	130	SEG[19]	6998.5	174	200	SEG[159]	5283.5	174	270	SEG[299]	3568.5	174
61	A0	180	-350	131	SEG[21]	6974	314	201	SEG[161]	5259	314	271	SEG[301]	3544	314
62	WRB	300	-350	132	SEG[23]	6949.5	174	202	SEG[163]	5234.5	174	272	SEG[303]	3519.5	174
63	RDB	420	-350	133	SEG[25]	6925	314	203	SEG[165]	5210	314	273	SEG[305]	3495	314
64	DUMMY2	540	-350	134	SEG[27]	6900.5	174	204	SEG[167]	5185.5	174	274	SEG[307]	3470.5	174
65	DUMMY2	660	-350	135	SEG[29]	6876	314	205	SEG[169]	5161	314	275	SEG[309]	3446	314
66	D[0]	780	-350	136	SEG[31]	6851.5	174	206	SEG[171]	5136.5	174	276	SEG[311]	3421.5	174
67	D[1]	900	-350	137	SEG[33]	6827	314	207	SEG[173]	5112	314	277	SEG[313]	3397	314
68	D[2]	1020	-350	138	SEG[35]	6802.5	174	208	SEG[175]	5087.5	174	278	SEG[315]	3372.5	174
69	D[3]	1140	-350	139	SEG[37]	6778	314	209	SEG[177]	5063	314	279	SEG[317]	3348	314
70	D[4]	1260	-350	140	SEG[39]	6753.5	174	210	SEG[179]	5038.5	174	280	SEG[319]	3323.5	174

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Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
281	SEG[321]	3299	174	351	COM[97]	1172.5	314	421	COM[27]	-1277.5	314	491	SEG[314]	-3372.5	174
282	SEG[323]	3274.5	314	352	COM[96]	1137.5	314	422	COM[26]	-1312.5	314	492	SEG[312]	-3397	314
283	SEG[325]	3250	174	353	COM[95]	1102.5	314	423	COM[25]	-1347.5	314	493	SEG[310]	-3421.5	174
284	SEG[327]	3225.5	314	354	COM[94]	1067.5	314	424	COM[24]	-1382.5	314	494	SEG[308]	-3446	314
285	SEG[329]	3201	174	355	COM[93]	1032.5	314	425	COM[23]	-1417.5	314	495	SEG[306]	-3470.5	174
286	SEG[331]	3176.5	314	356	COM[92]	997.5	314	426	COM[22]	-1452.5	314	496	SEG[304]	-3495	314
287	SEG[333]	3152	174	357	COM[91]	962.5	314	427	COM[21]	-1487.5	314	497	SEG[302]	-3519.5	174
288	SEG[335]	3127.5	314	358	COM[90]	927.5	314	428	COM[20]	-1522.5	314	498	SEG[300]	-3544	314
289	SEG[337]	3103	174	359	COM[89]	892.5	314	429	COM[19]	-1557.5	314	499	SEG[298]	-3568.5	174
290	SEG[339]	3078.5	314	360	COM[88]	857.5	314	430	COM[18]	-1592.5	314	500	SEG[296]	-3593	314
291	SEG[341]	3054	174	361	COM[87]	822.5	314	431	COM[17]	-1627.5	314	501	SEG[294]	-3617.5	174
292	SEG[343]	3029.5	314	362	COM[86]	787.5	314	432	COM[16]	-1662.5	314	502	SEG[292]	-3642	314
293	SEG[345]	3005	174	363	COM[85]	752.5	314	433	COM[15]	-1697.5	314	503	SEG[290]	-3666.5	174
294	SEG[347]	2980.5	314	364	COM[84]	717.5	314	434	COM[14]	-1732.5	314	504	SEG[288]	-3691	314
295	SEG[349]	2956	174	365	COM[83]	682.5	314	435	COM[13]	-1767.5	314	505	SEG[286]	-3715.5	174
296	SEG[351]	2931.5	314	366	COM[82]	647.5	314	436	COM[12]	-1802.5	314	506	SEG[284]	-3740	314
297	SEG[353]	2907	174	367	COM[81]	612.5	314	437	COM[11]	-1837.5	314	507	SEG[282]	-3764.5	174
298	SEG[355]	2882.5	314	368	COM[80]	577.5	314	438	COM[10]	-1872.5	314	508	SEG[280]	-3789	314
299	SEG[357]	2858	174	369	COM[79]	542.5	314	439	COM[9]	-1907.5	314	509	SEG[278]	-3813.5	174
300	SEG[359]	2833.5	314	370	COM[78]	507.5	314	440	COM[8]	-1942.5	314	510	SEG[276]	-3838	314
301	SEG[361]	2809	174	371	COM[77]	472.5	314	441	COM[7]	-1977.5	314	511	SEG[274]	-3862.5	174
302	SEG[363]	2784.5	314	372	COM[76]	437.5	314	442	COM[6]	-2012.5	314	512	SEG[272]	-3887	314
303	SEG[365]	2760	174	373	COM[75]	402.5	314	443	COM[5]	-2047.5	314	513	SEG[270]	-3911.5	174
304	SEG[367]	2735.5	314	374	COM[74]	367.5	314	444	COM[4]	-2082.5	314	514	SEG[268]	-3936	314
305	SEG[369]	2711	174	375	COM[73]	332.5	314	445	COM[3]	-2117.5	314	515	SEG[266]	-3960.5	174
306	SEG[371]	2686.5	314	376	COM[72]	297.5	314	446	COM[2]	-2152.5	314	516	SEG[264]	-3985	314
307	SEG[373]	2662	174	377	COM[71]	262.5	314	447	COM[1]	-2187.5	314	517	SEG[262]	-4009.5	174
308	SEG[375]	2637.5	314	378	COM[70]	227.5	314	448	COM[0]	-2222.5	314	518	SEG[260]	-4034	314
309	SEG[377]	2613	174	379	COM[69]	192.5	314	449	VPP	-2257.5	314	519	SEG[258]	-4058.5	174
310	SEG[379]	2588.5	314	380	COM[68]	157.5	314	450	VPP	-2292.5	314	520	SEG[256]	-4083	314
311	SEG[381]	2564	174	381	COM[67]	122.5	314	451	VPP	-2327.5	314	521	SEG[254]	-4107.5	174
312	SEG[383]	2539.5	314	382	COM[66]	87.5	314	452	VPP	-2362.5	314	522	SEG[252]	-4132	314
313	VPP	2502.5	314	383	COM[65]	52.5	314	453	VPP	-2397.5	314	523	SEG[250]	-4156.5	174
314	VPP	2467.5	314	384	COM[64]	17.5	314	454	VPP	-2432.5	314	524	SEG[248]	-4181	314
315	VPP	2432.5	314	385	COM[63]	-17.5	314	455	VPP	-2467.5	314	525	SEG[246]	-4205.5	174
316	VPP	2397.5	314	386	COM[62]	-52.5	314	456	VPP	-2502.5	314	526	SEG[244]	-4230	314
317	VPP	2362.5	314	387	COM[61]	-87.5	314	457	SEG[382]	-2539.5	174	527	SEG[242]	-4254.5	174
318	VPP	2327.5	314	388	COM[60]	-122.5	314	458	SEG[380]	-2564	314	528	SEG[240]	-4279	314
319	VPP	2292.5	314	389	COM[59]	-157.5	314	459	SEG[378]	-2588.5	174	529	SEG[238]	-4303.5	174
320	VPP	2257.5	314	390	COM[58]	-192.5	314	460	SEG[376]	-2613	314	530	SEG[236]	-4328	314
321	COM[127]	2222.5	314	391	COM[57]	-227.5	314	461	SEG[374]	-2637.5	314	531	SEG[234]	-4352.5	174
322	COM[126]	2187.5	314	392	COM[56]	-262.5	314	462	SEG[372]	-2662	314	532	SEG[232]	-4377	314
323	COM[125]	2152.5	314	393	COM[55]	-297.5	314	463	SEG[370]	-2686.5	314	533	SEG[230]	-4401.5	174
324	COM[124]	2117.5	314	394	COM[54]	-332.5	314	464	SEG[368]	-2711	314	534	SEG[228]	-4426	314
325	COM[123]	2082.5	314	395	COM[53]	-367.5	314	465	SEG[366]	-2735.5	314	535	SEG[226]	-4450.5	174
326	COM[122]	2047.5	314	396	COM[52]	-402.5	314	466	SEG[364]	-2760	314	536	SEG[224]	-4475	314
327	COM[121]	2012.5	314	397	COM[51]	-437.5	314	467	SEG[362]	-2784.5	314	537	SEG[222]	-4499.5	174
328	COM[120]	1977.5	314	398	COM[50]	-472.5	314	468	SEG[360]	-2809	314	538	SEG[220]	-4524	314
329	COM[119]	1942.5	314	399	COM[49]	-507.5	314	469	SEG[358]	-2833.5	314	539	SEG[218]	-4548.5	174
330	COM[118]	1907.5	314	400	COM[48]	-542.5	314	470	SEG[356]	-2858	314	540	SEG[216]	-4573	314
331	COM[117]	1872.5	314	401	COM[47]	-577.5	314	471	SEG[354]	-2882.5	314	541	SEG[214]	-4597.5	174
332	COM[116]	1837.5	314	402	COM[46]	-612.5	314	472	SEG[352]	-2907	314	542	SEG[212]	-4622	314
333	COM[115]	1802.5	314	403	COM[45]	-647.5	314	473	SEG[350]	-2931.5	314	543	SEG[210]	-4646.5	174
334	COM[114]	1767.5	314	404	COM[44]	-682.5	314	474	SEG[348]	-2956	314	544	SEG[208]	-4671	314
335	COM[113]	1732.5	314	405	COM[43]	-717.5	314	475	SEG[346]	-2980.5	314	545	SEG[206]	-4695.5	174
336	COM[112]	1697.5	314	406	COM[42]	-752.5	314	476	SEG[344]	-3005	314	546	SEG[204]	-4720	314
337	COM[111]	1662.5	314	407	COM[41]	-787.5	314	477	SEG[342]	-3029.5	314	547	SEG[202]	-4744.5	174
338	COM[110]	1627.5	314	408	COM[40]	-822.5	314	478	SEG[340]	-3054	314	548	SEG[200]	-4769	314
339	COM[109]	1592.5	314	409	COM[39]	-857.5	314	479	SEG[338]	-3078.5	314	549	SEG[198]	-4793.5	174
340	COM[108]	1557.5	314	410	COM[38]	-892.5	314	480	SEG[336]	-3103	314	550	SEG[196]	-4818	314
341	COM[107]	1522.5	314	411	COM[37]	-927.5	314	481	SEG[334]	-3127.5	314	551	SEG[194]	-4842.5	174
342	COM[106]	1487.5	314	412	COM[36]	-962.5	314	482	SEG[332]	-3152	314	552	SEG[192]	-4867	314
343	COM[105]	1452.5	314	413	COM[35]	-997.5	314	483	SEG[330]	-3176.5	314	553	SEG[190]	-4891.5	174
344	COM[104]	1417.5	314	414	COM[34]	-1032.5	314	484	SEG[328]	-3201	314	554	SEG[188]	-4916	314
345	COM[103]	1382.5	314	415	COM[33]	-1067.5	314	485	SEG[326]	-3225.5	314	555	SEG[186]	-4940.5	174
346	COM[102]	1347.5	314	416	COM[32]	-1102.5	314	486	SEG[324]	-3250	314	556	SEG[184]	-4965	314
347	COM[101]	1312.5	314	417	COM[31]	-1137.5	314	487	SEG[322]	-3274.5	314	557	SEG[182]	-4989.5	174
348	COM[100]	1277.5	314	418	COM[30]	-1172.5	314	488	SEG[320]	-3299	314	558	SEG[180]	-5014	314
349	COM[99]	1242.5	314	419	COM[29]	-1207.5	314	489	SEG[318]	-3323.5	314	559	SEG[178]	-5038.5	174
350	COM[98]	1207.5	314	420	COM[28]	-1242.5	314	490	SEG[316]	-3348	314	560	SEG[176]	-5063	314

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Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
561	SEG[174]	-5087.5	174	631	SEG[34]	-6802.5	174
562	SEG[172]	-5112	314	632	SEG[32]	-6827	314
563	SEG[170]	-5136.5	174	633	SEG[30]	-6851.5	174
564	SEG[168]	-5161	314	634	SEG[28]	-6876	314
565	SEG[166]	-5185.5	174	635	SEG[26]	-6900.5	174
566	SEG[164]	-5210	314	636	SEG[24]	-6925	314
567	SEG[162]	-5234.5	174	637	SEG[22]	-6949.5	174
568	SEG[160]	-5259	314	638	SEG[20]	-6974	314
569	SEG[158]	-5283.5	174	639	SEG[18]	-6998.5	174
570	SEG[156]	-5308	314	640	SEG[16]	-7023	314
571	SEG[154]	-5332.5	174	641	SEG[14]	-7047.5	174
572	SEG[152]	-5357	314	642	SEG[12]	-7072	314
573	SEG[150]	-5381.5	174	643	SEG[10]	-7096.5	174
574	SEG[148]	-5406	314	644	SEG[8]	-7121	314
575	SEG[146]	-5430.5	174	645	SEG[6]	-7145.5	174
576	SEG[144]	-5455	314	646	SEG[4]	-7170	314
577	SEG[142]	-5479.5	174	647	SEG[2]	-7194.5	174
578	SEG[140]	-5504	314	648	SEG[0]	-7219	314
579	SEG[138]	-5528.5	174	649	VPP	-7243.5	174
580	SEG[136]	-5553	314	650	VPP	-7268	314
581	SEG[134]	-5577.5	174				
582	SEG[132]	-5602	314				
583	SEG[130]	-5626.5	174				
584	SEG[128]	-5651	314				
585	SEG[126]	-5675.5	174				
586	SEG[124]	-5700	314				
587	SEG[122]	-5724.5	174				
588	SEG[120]	-5749	314				
589	SEG[118]	-5773.5	174				
590	SEG[116]	-5798	314				
591	SEG[114]	-5822.5	174				
592	SEG[112]	-5847	314				
593	SEG[110]	-5871.5	174				
594	SEG[108]	-5896	314				
595	SEG[106]	-5920.5	174				
596	SEG[104]	-5945	314				
597	SEG[102]	-5969.5	174				
598	SEG[100]	-5994	314				
599	SEG[98]	-6018.5	174				
600	SEG[96]	-6043	314				
601	SEG[94]	-6067.5	174				
602	SEG[92]	-6092	314				
603	SEG[90]	-6116.5	174				
604	SEG[88]	-6141	314				
605	SEG[86]	-6165.5	174				
606	SEG[84]	-6190	314				
607	SEG[82]	-6214.5	174				
608	SEG[80]	-6239	314				
609	SEG[78]	-6263.5	174				
610	SEG[76]	-6288	314				
611	SEG[74]	-6312.5	174				
612	SEG[72]	-6337	314				
613	SEG[70]	-6361.5	174				
614	SEG[68]	-6386	314				
615	SEG[66]	-6410.5	174				
616	SEG[64]	-6435	314				
617	SEG[62]	-6459.5	174				
618	SEG[60]	-6484	314				
619	SEG[58]	-6508.5	174				
620	SEG[56]	-6533	314				
621	SEG[54]	-6557.5	174				
622	SEG[52]	-6582	314				
623	SEG[50]	-6606.5	174				
624	SEG[48]	-6631	314				
625	SEG[46]	-6655.5	174				
626	SEG[44]	-6680	314				
627	SEG[42]	-6704.5	174				
628	SEG[40]	-6729	314				
629	SEG[38]	-6753.5	174				
630	SEG[36]	-6778	314				

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Function Description

Microprocessor Interface Selection

The 8080-Parallel Interface, 6800-Parallel Interface, Serial Interface (SPI) can be selected by different selections of IM0~2 as shown in Table 1.

Table

Interface	Config			Data signal								Control signal				
	IM0	IM1	IM2	D7	D6	D5	D4	D3	D2	D1	D0	E/RDB	WRB	CSB	A0	RESB
6800	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W	CS	A0	RES
8080	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	RD	WR	CS	A0	RES
4-Wire SPI	0	0	0	Hz (Note1)					SO (Note)	SI/SO (Note)	SCL	Pull Low		CS	A0	RES
3-Wire SPI	1	0	0	Hz (Note1)					SO (Note)	SI/SO (Note)	SCL	Pull Low		CS	Pull Low	RES
I²C	0	1	0	Hz (Note1)					SDA	SCL	Pull Low		Pull Low	SA0	RES	

Note1:

When Serial Interface (SPI) or I²C Interface is selected, D7~D2 is Hz. D7~D2 is recommended to connect the VDD or GND. It is also allowed to leave D7~D2 unconnected.

Note: When reading in SPI interface, D2 can be select as data output pad.

6800-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), R/W, E, A0 and CS. It includes 2 forms.

Form 1: A falling edge of E input serve as READ latch signal while CS is kept low and R/W is kept high. A falling edge of E input serve as WRITE latch signal while CS is kept low and R/W is kept low. This is shown in Table.2 below.

Table 2 (Form 1)

Function	CS	A0	R/W	E
Write command	L	L	L	↓
Read status	L	L	H	↓
Write data	L	H	L	↓
Read data	L	H	H	↓

Note:

1. '↓' stands for falling edge of signal.

2. 'H' stands for high in signal, 'L' stands for low in signal.

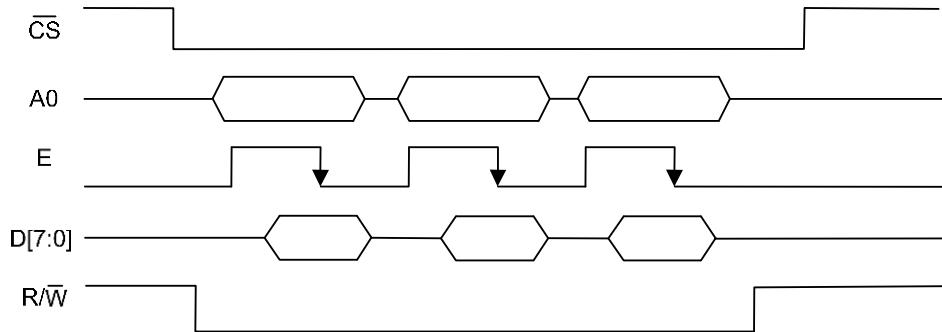


Figure 2 Example of write procedure in 6800 parallel interface form 1

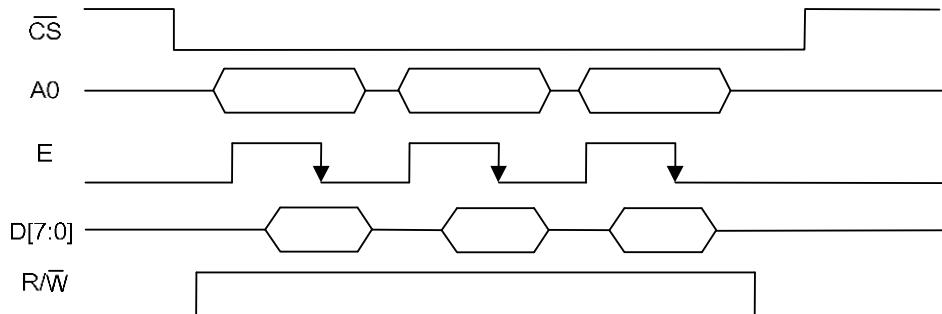


Figure 3 Example of read procedure in 6800 parallel interface form 1

Form 2: A rising edge of \overline{CS} input serve as READ latch signal while E is kept high and $\overline{R/W}$ is kept high. A rising edge of \overline{CS} input serve as WRITE latch signal while E is kept high and $\overline{R/W}$ is kept low. A low in A0 indicates COMMAND read/write and high in A0 indicates DATA read/write. This is shown in Table.3 below.

Table 3 (6800 Form 2)

Function	\overline{CS}	A0	R/\overline{W}	E
Write command	↑	L	L	H
Read status	↑	L	H	H
Write data	↑	H	L	H
Read data	↑	H	H	H

Note:

1. '↑' stands for rising edge of signal.

2. 'H' stands for high in signal, 'L' stands for low in signal.

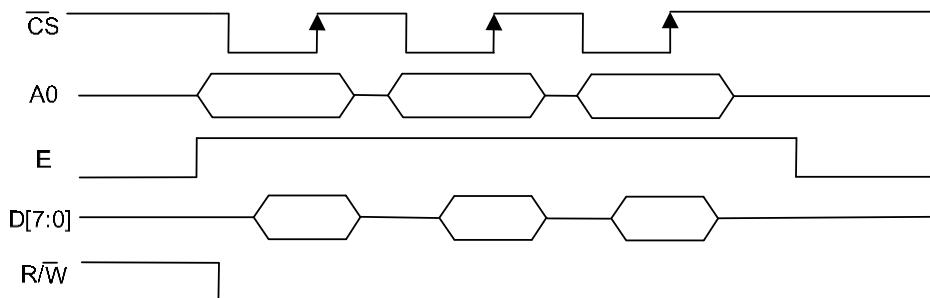


Figure 4 Example of write procedure in 6800 parallel interface form 2

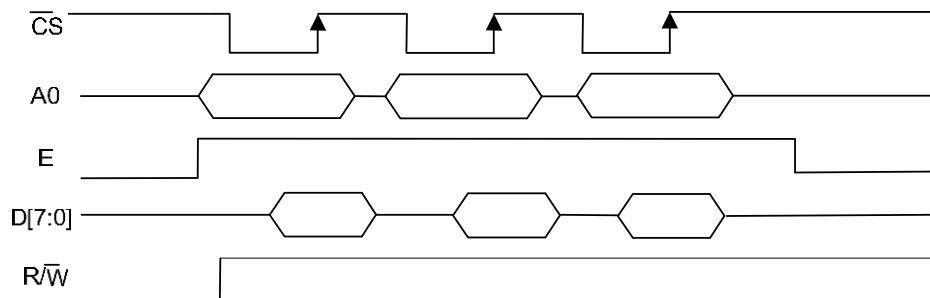


Figure 5 Example of read procedure in 6800 parallel interface form 2

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing are internally performed, which require the insertion of a dummy read before the first actual display data read. This is shown in Figure. 5 below.

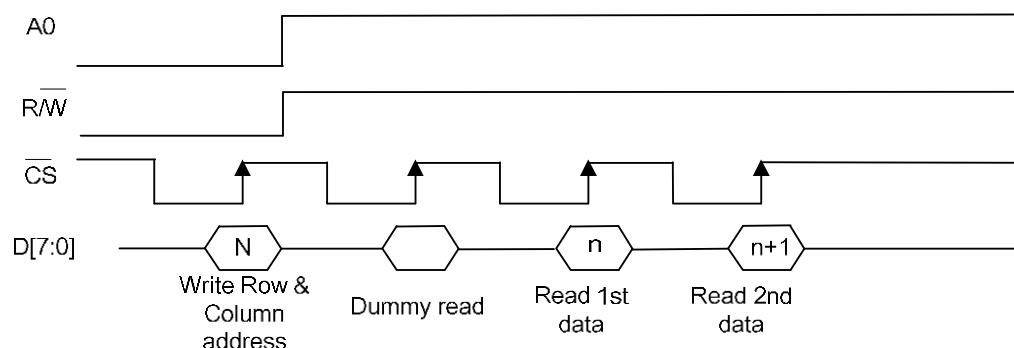


Figure 6 Read RAM data process with dummy read

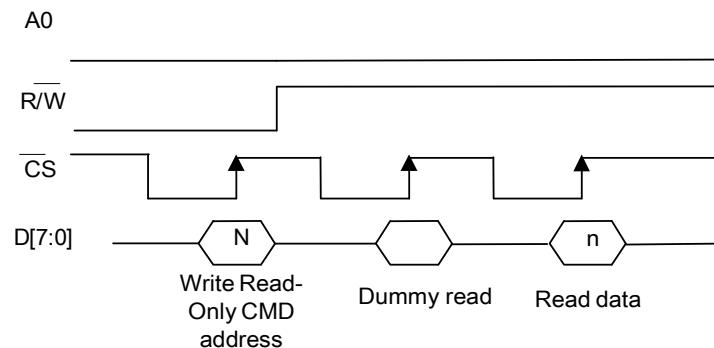


Figure 7 Read Read-Only CMD process with dummy read

8080-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), \overline{WR} , \overline{RD} , A0 and \overline{CS} . It includes 2 forms.

Form 1: A rising edge of \overline{RD} input serve as data READ latch signal while \overline{CS} is kept low. A rising edge of \overline{WR} input serve as data/command Write latch signal while \overline{CS} is kept low. A low in A0 indicates COMMAND read/write and high in A0 indicates DATA read/write. This is shown in Table.4 below.

Table 4 (8080 Form1)

Function	\overline{CS}	A0	\overline{RD}	\overline{WR}
Write command	L	L	H	\uparrow
Read command	L	L	\uparrow	H
Write data	L	H	H	\uparrow
Read data	L	H	\uparrow	H

Note:

1. ' \uparrow ' stands for rising edge of signal.
2. 'H' stands for high in signal, 'L' stands for low in signal.

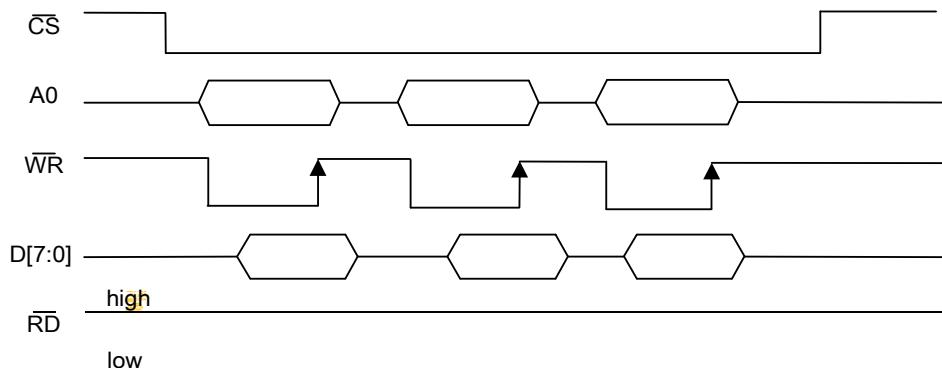


Figure 8 Example of write procedure in 8080 parallel interface form 1

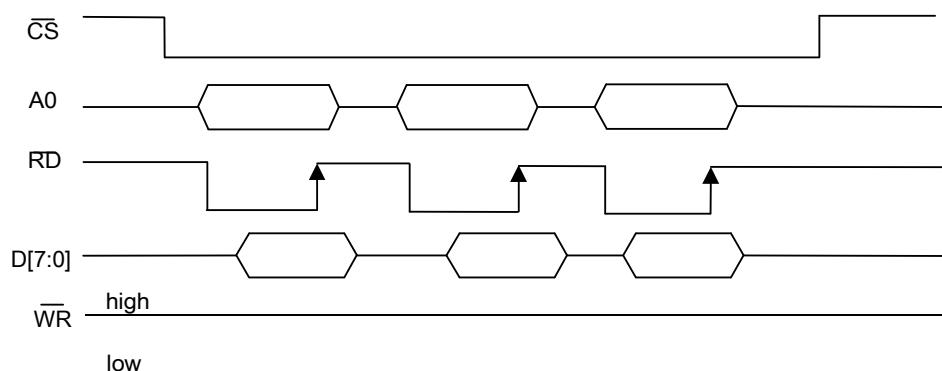


Figure 9 Example of read procedure in 8080 parallel interface form 1

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Form 2: A rising edge of \overline{CS} input serve as data READ latch signal while \overline{RD} is kept low. A rising edge of \overline{CS} input serve as data Write latch signal while \overline{WR} is kept low. A low in A0 indicates COMMAND read/write and high in A0 indicates DATA read/write. This is shown in Table.5 below.

Table 5 (8080 Form2)

Function	\overline{CS}	A0	\overline{RD}	\overline{WR}
Write command	↑	L	H	L
Read command	↑	L	L	H
Write data	↑	H	H	L
Read data	↑	H	L	H

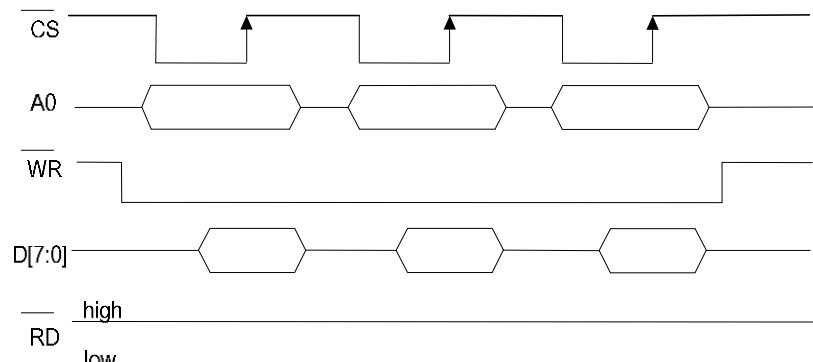


Figure 10 Example of write procedure in 8080 parallel interface form 2

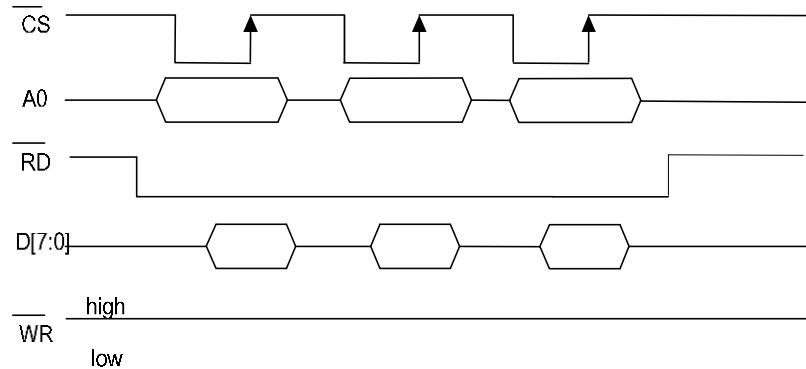


Figure 11 Example of read procedure in 8080 parallel interface form 2

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing are internally performed, which require the insertion of a dummy read before the first actual display data read.

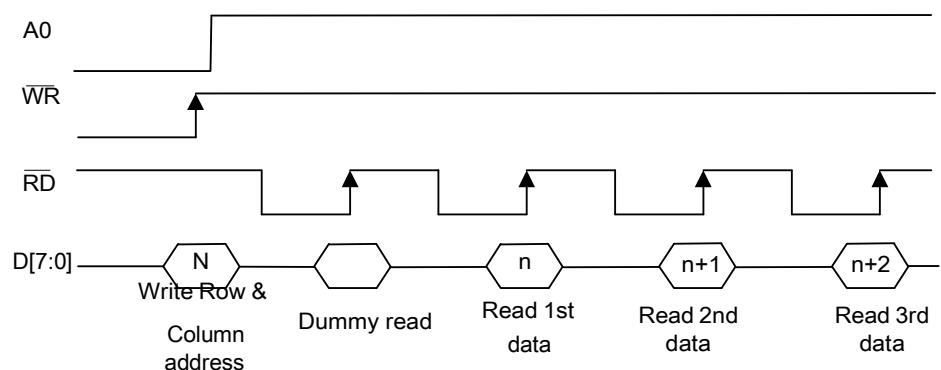


Figure 12 Read RAM data process dummy read

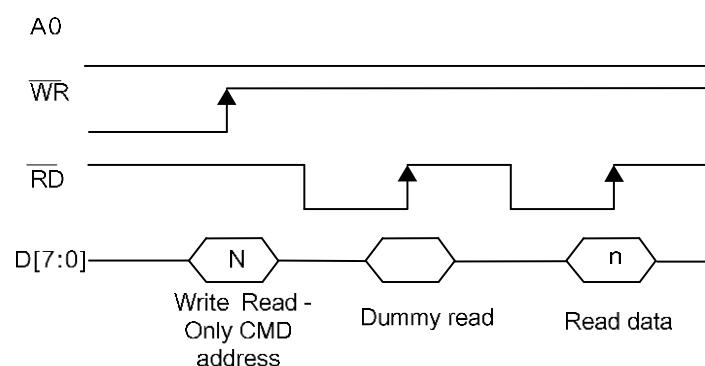


Figure 13 Read Read-Only CMD process with dummy read

SP5140 internal SPEC

4 Wire Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCL, serial data SI, A0 and \overline{CS} . SI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6 ... and D0. A0 is sampled on every eighth clock and the data byte in the shift register is written to the display data RAM (A0=1) or command register (A0=0) in the same clock.

Table 6

IM0	IM1	IM2	Type	\overline{CS}	A0	\overline{RD}	\overline{WR}	D0	D1	D2	D3 to D7
0	0	0	4-wire SPI	\overline{CS}	A0	-	-	SCL	SI/SO	SO	(Hi-z)

Note: “-” pin must always be HIGH or LOW. D7~D2 is recommended to connect the VDD or GND. It's also allowed to leave D7~D2 unconnected.

The serial interface is initialized when \overline{CS} is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on \overline{CS} enables the serial interface and indicates the start of data transmission. The SPI is also able to work properly when the \overline{CS} always keep low, but it is not recommended.

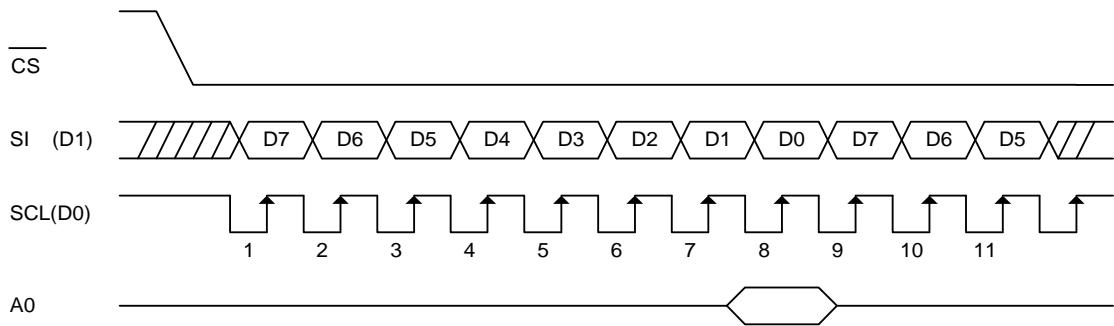


Figure 14 4-wire SPI data transfer

SP5140 internal SPEC

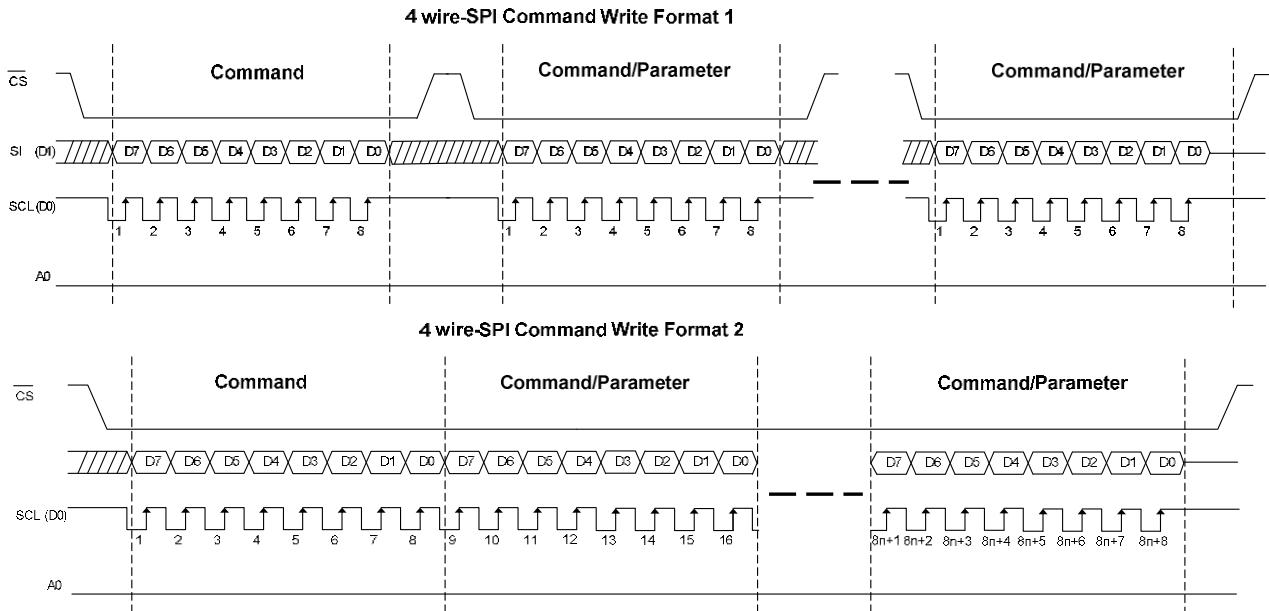


Figure 15 4-wire SPI write command

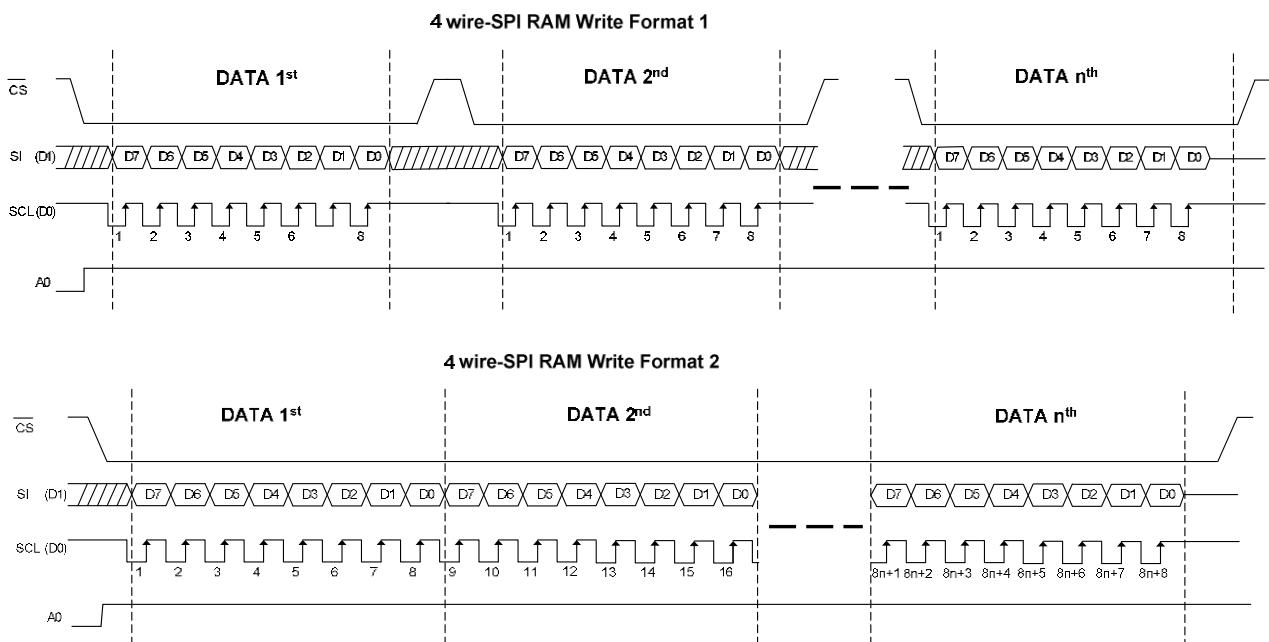
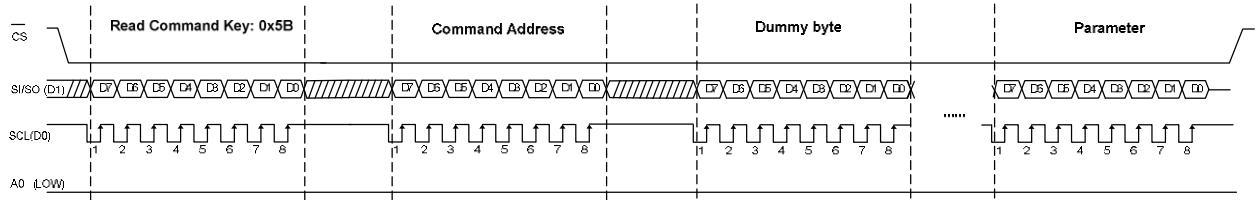


Figure 16 4-wire SPI write RAM

SP5140 internal SPEC

When the chip is not active, the shift registers and the counter are reset to their initial statuses. When finish read command, CSB signal must be pull high. Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

92h = 0x69, SPI data output to data pin D1.



92h ≠ 0x69, SPI data output to data pin D2. (RESET)

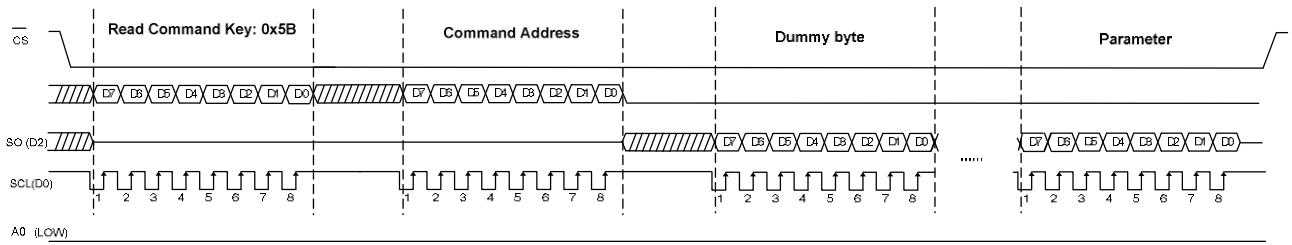
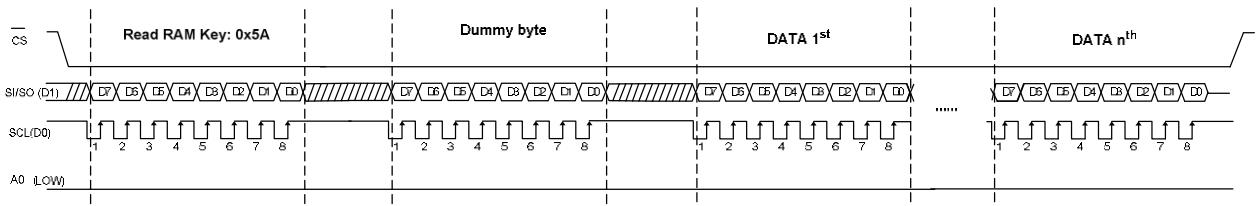


Figure 17 4-wire SPI read command

92h = 0x69, SPI data output to data pin D1.



92h ≠ 0x69, SPI data output to data pin D2. (RESET)

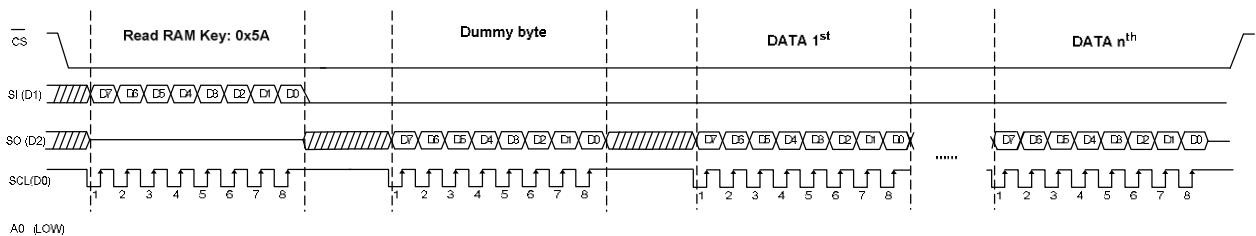


Figure 18 4-wire SPI read RAM

3 Wire Serial Interface (3-wire SPI)

The 3 wire serial interface consists of serial clock SCL, serial data SI, and \overline{CS} . SI is shifted into a 9-bit shift register on every rising edge of SCL in the order of D/C, D7, D6 ... D0. The D/C bit (first of the 9 bit) will determine the transferred data is written to the display data RAM (D/C=1) or command register (D/C=0).

Table 7

IM0	IM1	IM2	Type	\overline{CS}	A0	\overline{RD}	\overline{WR}	D0	D1	D2	D2 to D7
1	0	0	3-wire SPI	\overline{CS}	A0	-	-	SCL	SI/SO	SO	(Hi-z)

Note: “-” pin must always be HIGH or LOW. D7~ D2 is recommended to connect the VDD or GND. It is also allowed to leave D7~ D2 unconnected.

The serial interface is initialized when \overline{CS} is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on \overline{CS} enables the serial interface and indicates the start of data transmission. The SPI is also able to work properly when the \overline{CS} always keep low, but it is not recommended.

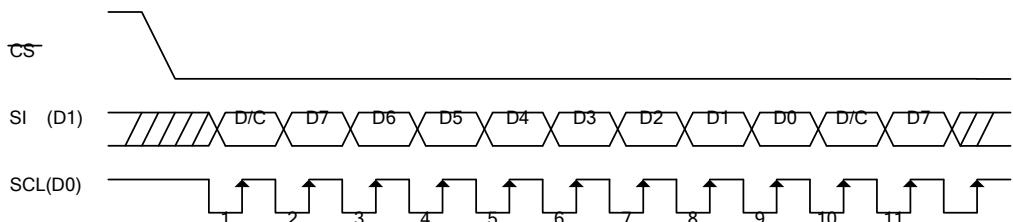


Figure19 3-wire SPI data transfer

SP5140 internal SPEC

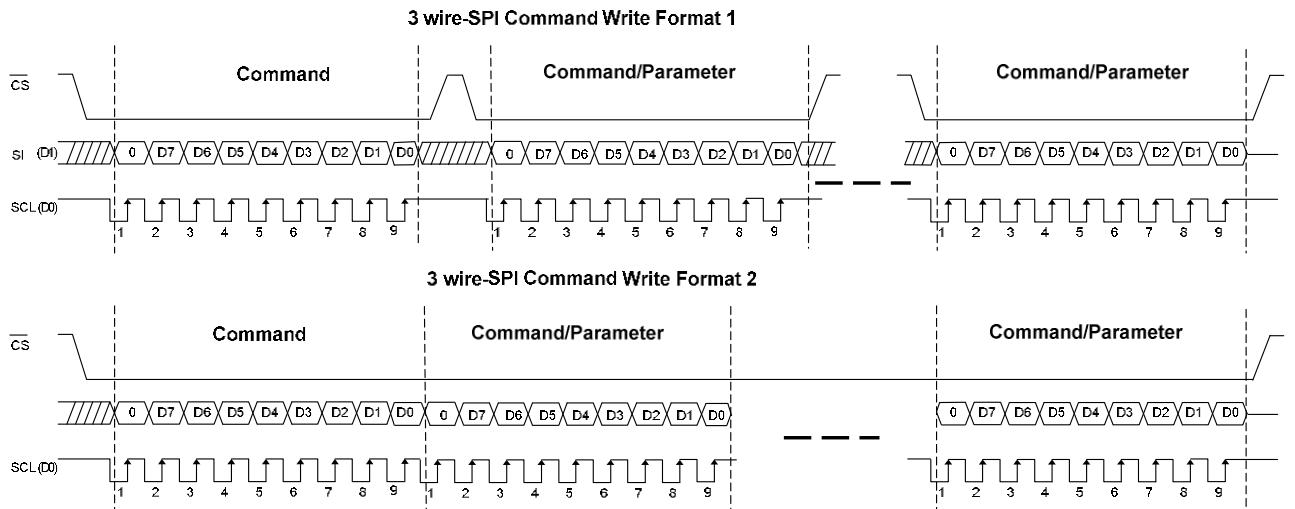
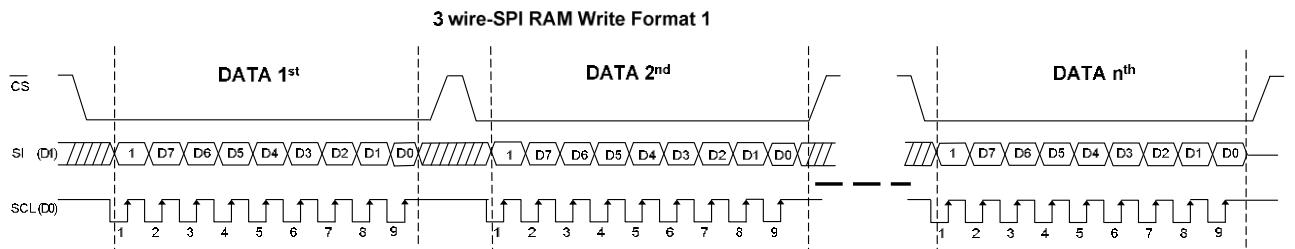


Figure 20 3-wire SPI write command



3 wire SPI format 2 (RAM Write)

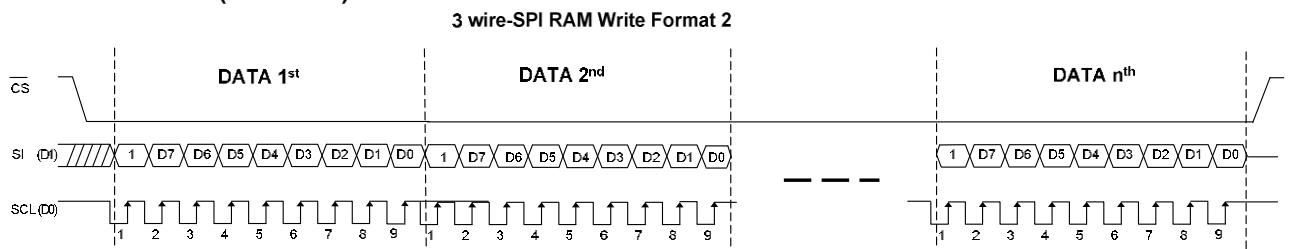
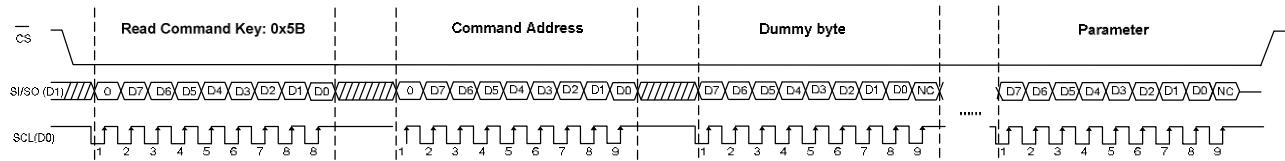


Figure 21 3-wire SPI write RAM

SP5140 internal SPEC

When the chip is not active, the shift registers and the counter are reset to their initial statuses. When finish read command, CSB signal must be pull high. Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

92h = 0x69, SPI data output to data pin D1.



92h ≠ 0x69, SPI data output to data pin D2. (RESET)

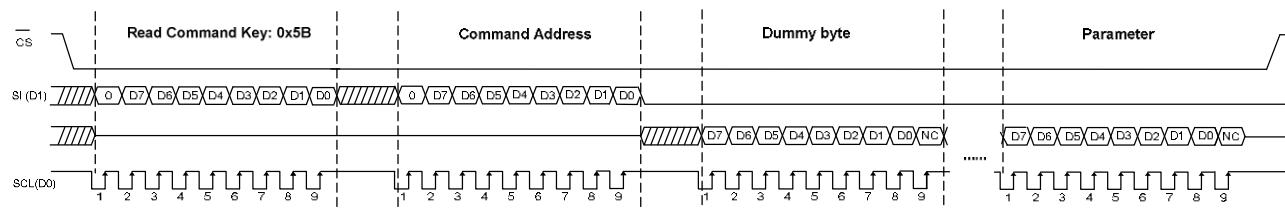
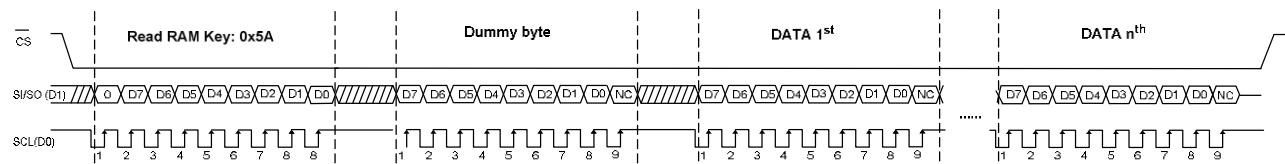


Figure 22 3-wire SPI read command

92h = 0x69, SPI data output to data pin D1.



92h ≠ 0x69, SPI data output to data pin D2. (RESET)

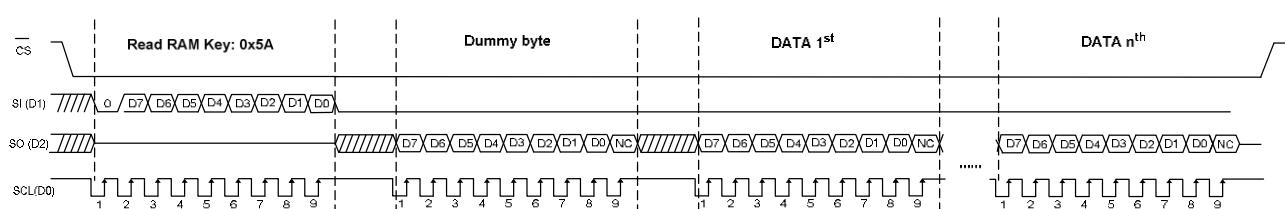


Figure 23 4-wire SPI read RAM

SP5140 internal SPEC

I²C-bus Interface

The SP5140 can transfer data via a standard I²C-bus and has slave mode only in communication. The command or RAM data can be written into the chip and the status and RAM data can be read out of the chip.

Table 8

IM0	IM1	IM2	Type	CS	A0	RD	WR	D0	D1	D2 to D17
0	1	0	I ² C Interface	CS	SA0	-	-	SCL	SI	(Hi-z)

Note:

"-" pin must always be HIGH or LOW. D7~ D2 is recommended to connect the VDD or GND. It is also allowed to leave D7~ D2 unconnected.

CS Signal could always pull low in I²C-bus application.

Characteristics of the I²C-bus

The I²C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Note: The positive supply of pull-up resistor must equal to the value of VDD.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

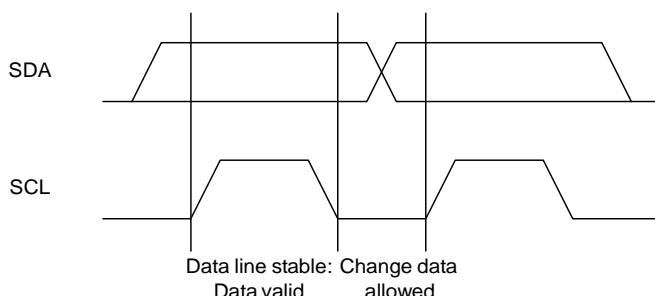


Figure 24 Bit Transfer

Start and Stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

SP5140 internal SPEC

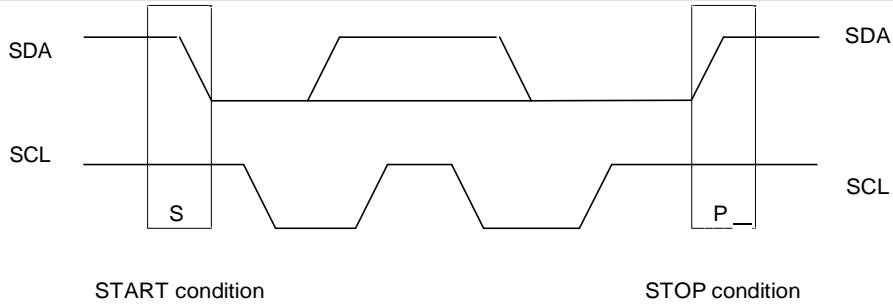


Figure 25 Start and Stop conditions

System configuration

- Transmitter: The device that sends the data to the bus.
- Receiver: The device that receives the data from the bus.
- Master: The device that initiates a transfer generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-Master: More than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.

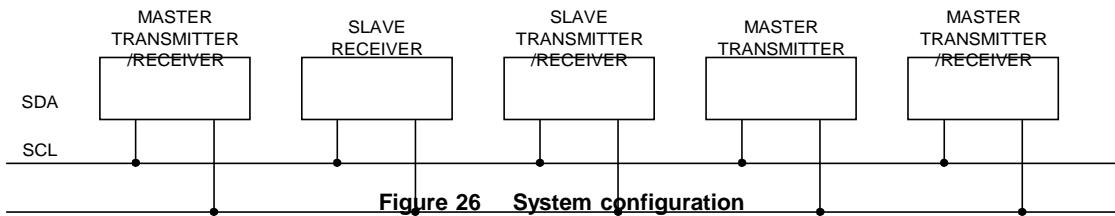


Figure 26 System configuration

Acknowledge

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

SP5140 internal SPEC

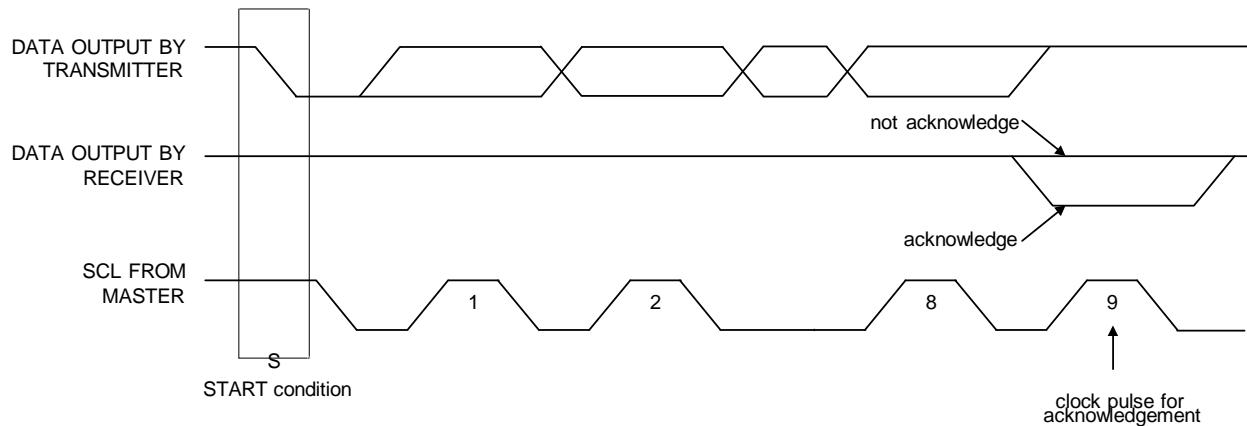


Figure 27 Acknowledge

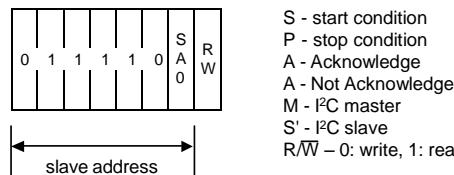
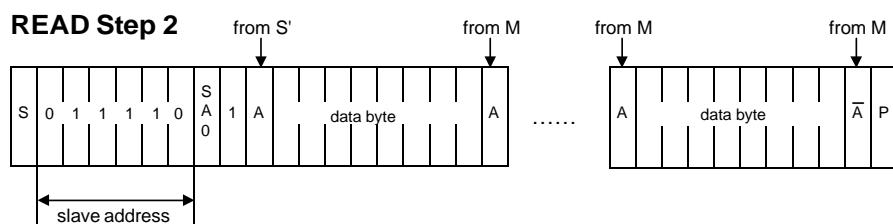
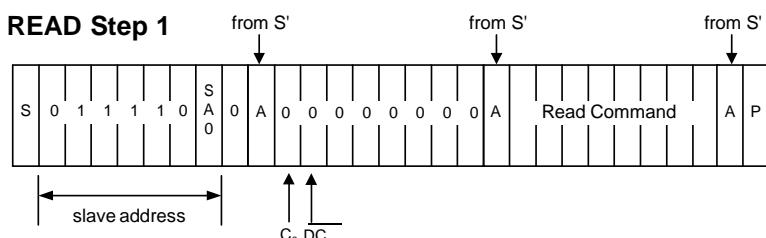
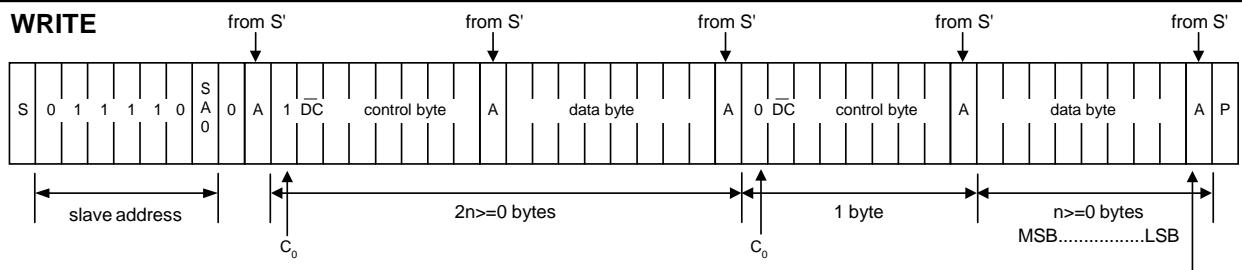
Protocol

The SP5140 supports both read and write access. The R / \overline{W} bit is part of the slave address. Before any data is transmitted on the I²C-bus, the device that should respond is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the SP5140. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(GND) or 1(VDD). The I²C-bus protocol is illustrated in Fig.14. The sequence is initiated with a START condition (S) from the I²C-bus master that is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and D / C (note1), plus a data byte (see Fig.19). The last control byte is tagged with a cleared most significant bit, the continuation bit Co. After a control byte with a cleared Co-bit, only data bytes will follow. The state of the D / C-bit defines whether the data-byte is interpreted as a command or as RAM-data. The control and data bytes are also acknowledged by all addressed slaves on the bus. After the last control byte, depending on the D / C bit setting, either a series of display data bytes or command data bytes may follow. If the D / C bit was set to '1', these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended SP5140 device. If the D / C bit of the last control byte was set to '0', these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed slave. At the end of the transmission the I²C-bus master issues a stop condition (P). If the R / w bit is set to 1 in the slave-address, the chip will output data immediately after the slave-address according to the D / C bit, which was sent during the last write access. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

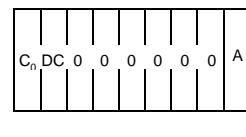
Whether the dummy packet needed or not in the read protocol of all interface as below:

I/F	Only-Read CMD	Read Ram data
I2C	Yes	No dummy packet

SP5140 internal SPEC



S - start condition
 P - stop condition
 A - Acknowledge
 A - Not Acknowledge
 M - I²C master
 S' - I²C slave
 R/W - 0: write, 1: read



Note:

Read Command = NULL , means that reading status.

Read Command = Command Address , means that reading command parameters.

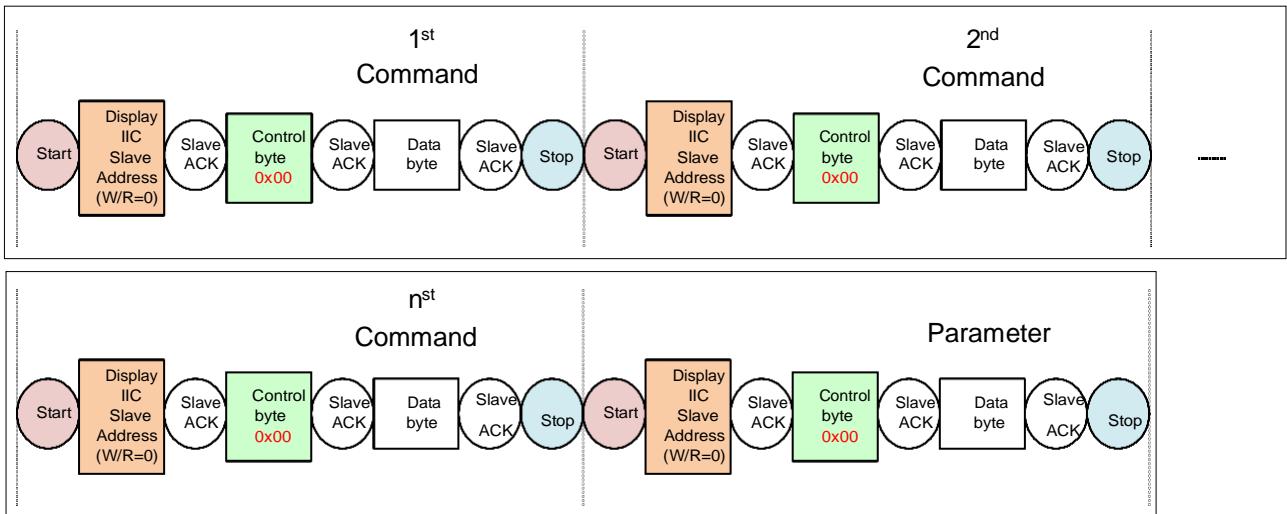
Figure 28 I²C Protocol

Note1:

1. Co = “ 0 ” : The last control byte , only data bytes to follow, Co = “ 1 ” : Next two bytes are a data byte and another control byte;
2. D/C = “ 0 ” : The data byte is for command operation, D/C = “ 1 ” : The data byte is for RAM operation.

SP5140 internal SPEC

Format1 :



Format2 :

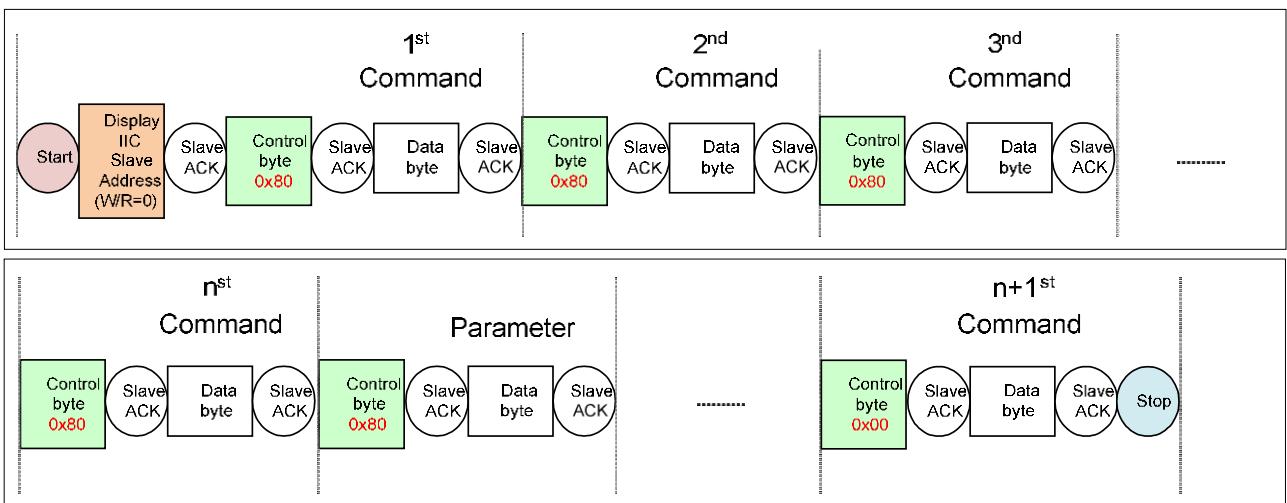
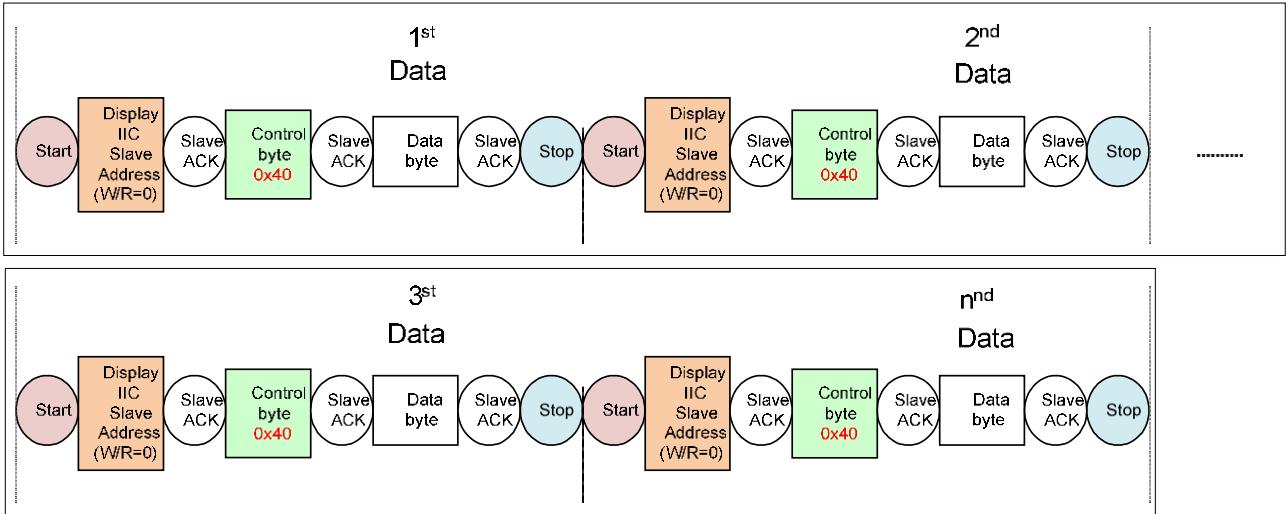


Figure 29 I²C Write Command

SP5140 internal SPEC

Format1 :



Format2 :

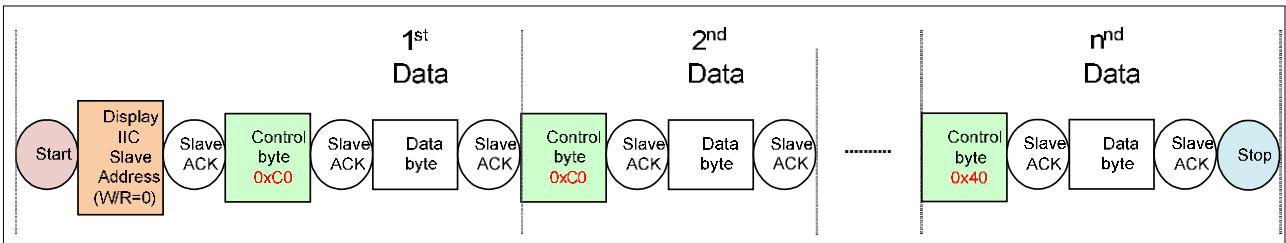


Figure 30 I²C Write RAM

SP5140 internal SPEC

Read Command:

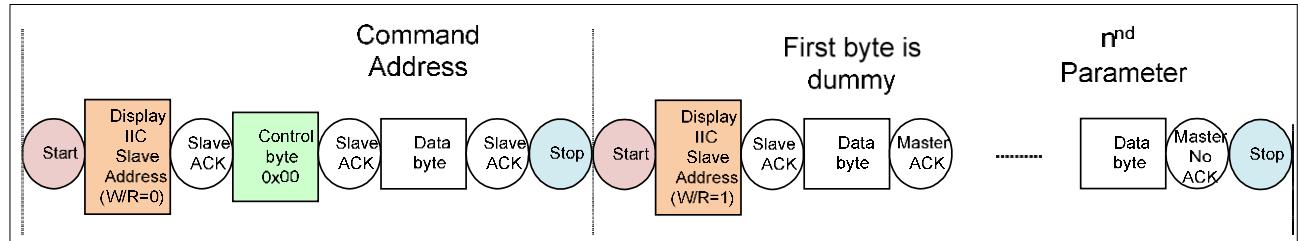


Figure 31 I²C read Command

Whether the dummy packet needed or not in the read protocol of all interface as below:

I/F	Read CMD	Read Ram
6800	Yes	Yes
8080	Yes	Yes
4-wire	Yes	Yes
3-wire	Yes	Yes
I ² C	Yes	-

SP5140 internal SPEC

Access to Display Data RAM and Internal Registers

This module determines whether the input data is interpreted as data or command. When A0 = "H", the inputs at D7 - D0 are interpreted as data and be written to display RAM. When A0 = "L", the inputs at D7 - D0 are interpreted as command, they will be decoded and be written to the corresponding command registers.

Display Data RAM

The Display Data RAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 384 X 128 X 4 bits. For mechanical flexibility, re-mapping on both segment and common outputs can be selected by software.

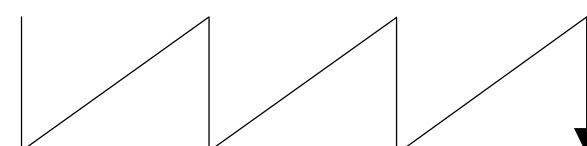
Horizontal Addressing Mode

SEG Scan Direction		A0H (Normal)	SEG0	SEG1	---	SEG 382	SEG 383
COM Scan Direction		A1H (Remap)	SEG383	SEG382	---	SEG 1	SEG 0
C0H (Normal)	C8H (Reverse)	Column Row		00H	---	BFH	
COM0	COM127	00H	D0[3:0]	D0[7:4]	---	D191[3:0]	D191[7:4]
COM1	COM126	01H	D192[3:0]	D192[7:4]	---	D383[3:0]	D383[7:4]
COM2	COM125	02H	D384[3:0]	D384[7:4]	---	D575[3:0]	D575[7:4]
COM3	COM124	03H	D576[3:0]	D576[7:4]	---	D767[3:0]	D767[7:4]
---	---	---					
COM124	COM3	7CH	D23808[3:0]	D23808[7:4]	---	D23999[3:0]	D23999[7:4]
COM125	COM2	7DH	D24000[3:0]	D24000[7:4]	---	D24191[3:0]	D24191[7:4]
COM126	COM1	7EH	D24192[3:0]	D24192[7:4]	---	D24383[3:0]	D24383[7:4]
COM127	COM0	7FH	D24384[3:0]	D24384[7:4]	---	D24575[3:0]	D24575[7:4]

SP5140 internal SPEC

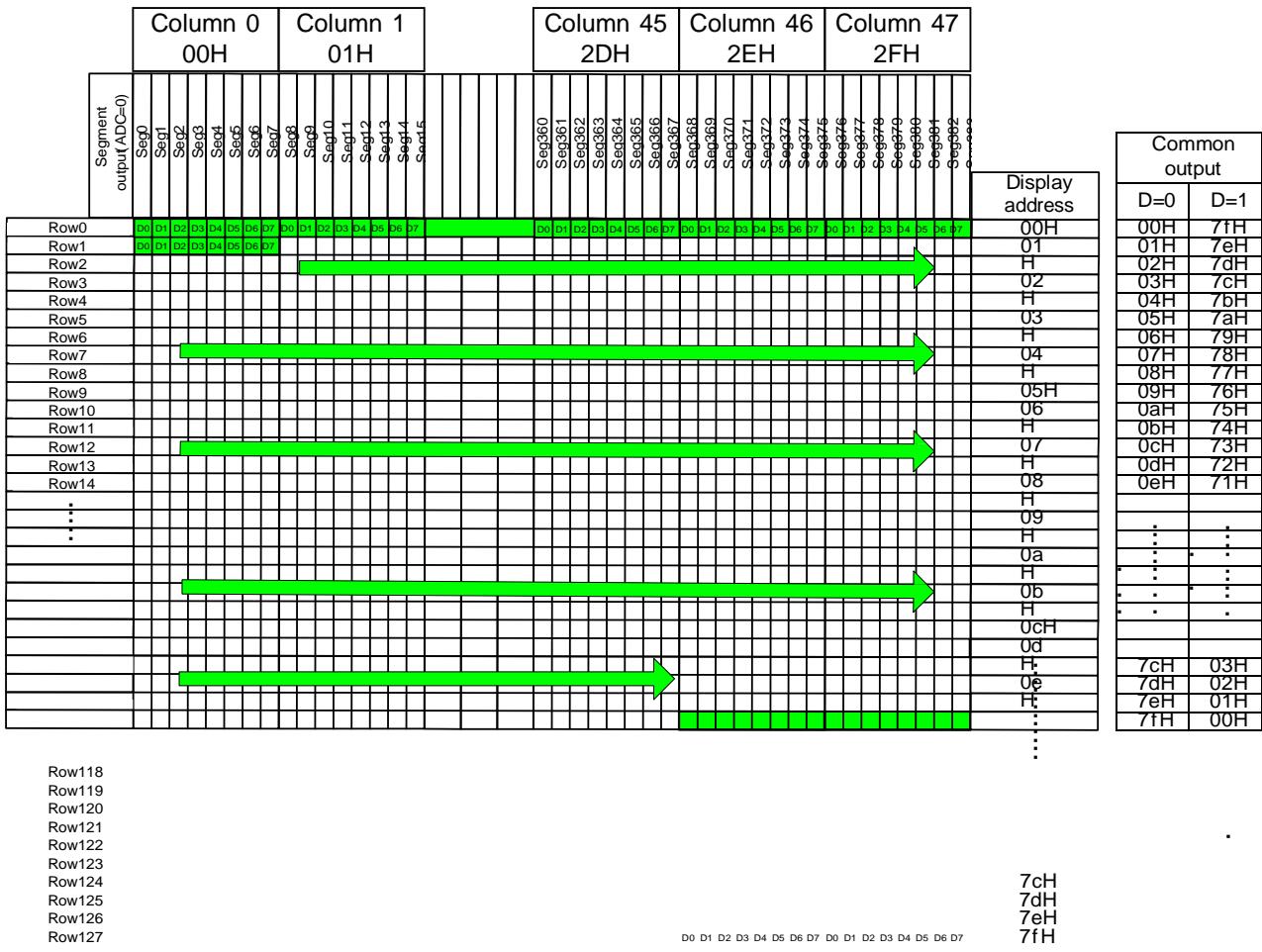
Vertical addressing mode

SEG Scan Direction		A0H (Normal)	SEG0	SEG1	---	SEG 382	SEG 383
COM Scan Direction		A1H (Remap)	SEG383	SEG382	---	SEG 1	SEG 0
C0H (Normal)	C8H (Reverse)	Column Row	00H		---	BFH	
COM0	COM127	00H	D0[3:0]	D0[7:4]	---	D24448[3:0]	D24448 [7:4]
COM1	COM126	01H	D1[3:0]	D1 [7:4]	---	D24449 [3:0]	D24449 [7:4]
COM2	COM125	02H	D2[3:0]	D2[7:4]	---	D24450 [3:0]	D24450 [7:4]
COM3	COM124	03H	D3[3:0]	D3[7:4]	---	D24451 [3:0]	D24451 [7:4]
---	---	---					
COM124	COM3	7CH	D124[3:0]	D124[7:4]	---	D24572 [3:0]	D24572 [7:4]
COM125	COM2	7DH	D125[3:0]	D125[7:4]	---	D24573 [3:0]	D24573 [7:4]
COM126	COM1	7EH	D126[3:0]	D126[7:4]	---	D24574 [3:0]	D24574 [7:4]
COM127	COM0	7FH	D127[3:0]	D127[7:4]	---	D24575[3:0]	D24575[7:4]



SP5140 internal SPEC

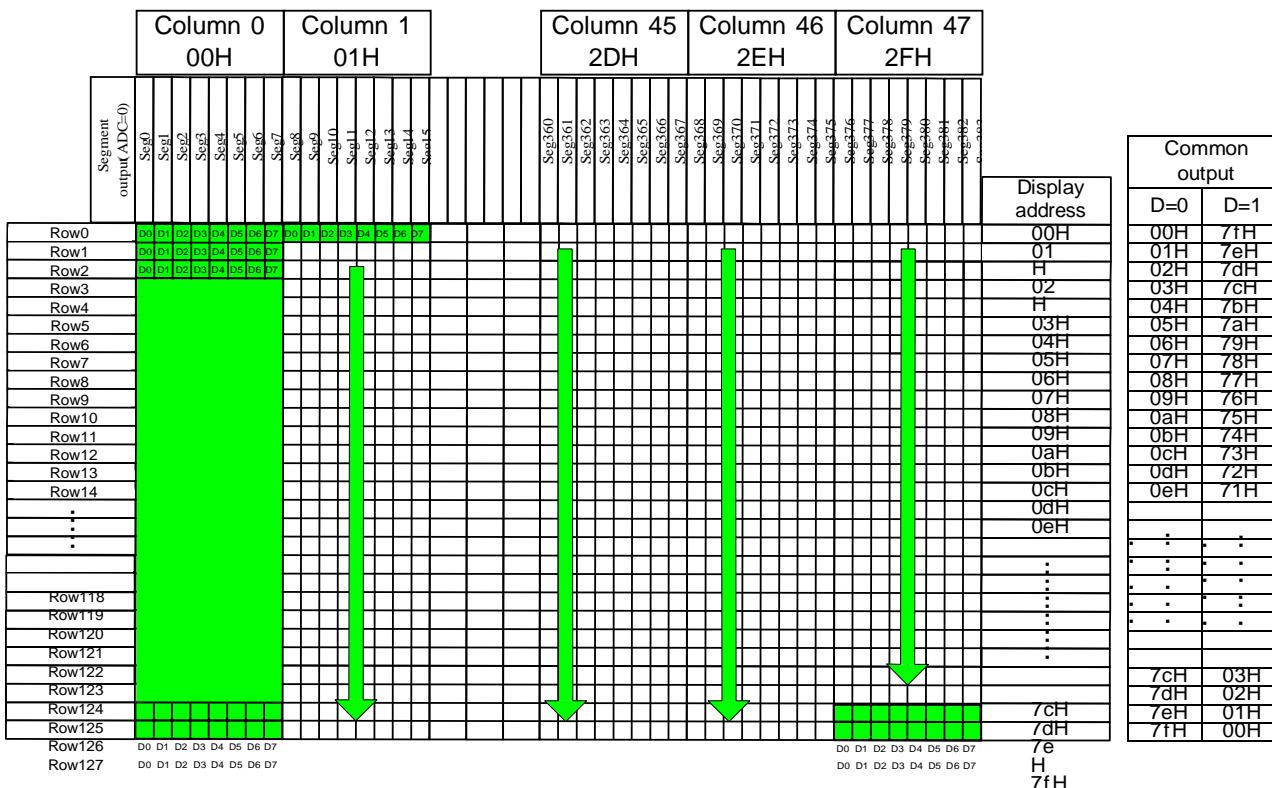
1 bit Mode Mono Display (1 byte data composed of 8 SEG pixel data, Horizontal addressing mode)



Note: In mono mode, RAM is written by gray mode, and read by gray mode.

1 bit Mode Mono Display (1 Byte data composed of 8 Seg pixel data, Vertical addressing mode)

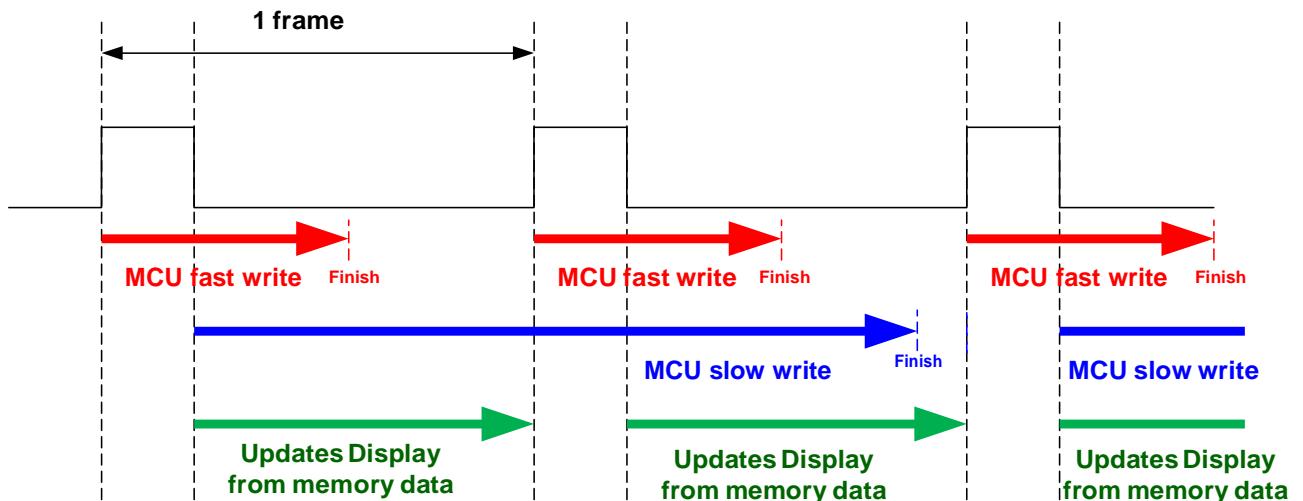
Register setting : ACh= 0x01, 20h= 0x01



Note: In mono mode, RAM is written by gray mode, and read by gray mode.

FRM Synchronization

FRM synchronization signal can be used to prevent tearing effect.



MCU fast write : MCU should start to write new frame of ram data just after rising edge of FRM pulse and should be finished well before the rising edge of the next FRM pulse

MCU slow write : MCU should start to write new frame of ram data just after the falling edge of the 1st FRM pulse and must be finished well before the rising edge of the 3rd FRM pulse

The Oscillator Circuit

This is a RC type oscillator that produces the display clock. The oscillator circuit is only enabled when CLS = "H".

When CLS = "L", the oscillation is off and the display clock comes from the CL pad.

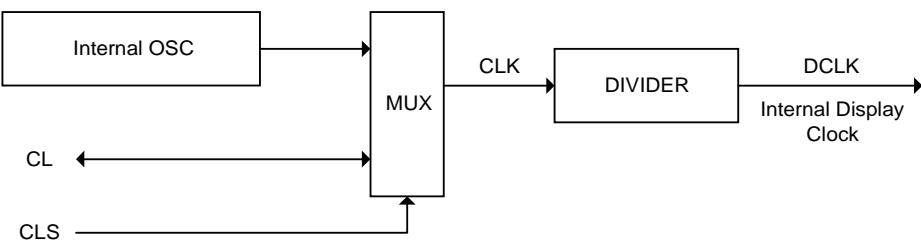


Figure 33

SP5140 internal SPEC

Current Control and Voltage Control

VPP is from external power supplies. I_{REF} is a reference current source for segment current drivers, it can change the brightness of the screen and the value depends on the resistance of $R_{I_{REF}}$ and VPP.

When VPP=15V, contrast = 0xFF, the value of resistor $R_{I_{REF}}$ can be found as Table 9:

Table 9

$R_{I_{REF}}$	$I_{SEG}(\mu A)$
900K	300
670K	400
530K	500
440K	600

Common Drivers/Segment Drivers

Segment drivers with 160 current sources drive OLED panel. The driving current can be adjusted up to $600\mu A$ with 256 steps. Common drivers generate voltage scanning pulses.

16 Grayscale

The gray scale effect is generated by controlling the pulse width (PW) of current drive phase. The Gray Scale Table stores the corresponding gray scale setting of the 16 gray scale levels (GS0~GS15) through the software commands B8H and BAH. As shown in Table10, RAM data has 4 bits, represent the 16 gray scale levels from GS0 to GS15.

Note: GS0 cannot be adjusted.

Table 10

RAM Data(4 bits)	Gamma Setting (Command B8H)	RESET Gamma Setting for PWM-driving (Command BAH)
0000	GS0	GP0
0001	GS1	GP1
0010	GS2	GP2
...
1110	GS14	GP14
1111	GS15	GP15

Reset Circuit

When power is turned on or the RESB input falls to “L”, these reenter their RESET state.

The RESET settings are shown below:

1. Display is OFF. Common and segment are in high impedance state.
2. 384 X 128 Display mode.
3. Normal segment and display data mapping (SEG0 is mapped to the top line of the display).
4. Shift register data clear in serial interface.
5. Column address counter is set at 0.
6. Contrast control register is set at 80H.
7. Normal common scan direction

SP5140 internal SPEC

Command Set

1. Set Lower Column Start Address: (00H - 0FH)

2. Set Higher Column Start Address: (10H – 1BH)

Specify column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them into successions. When the microprocessor repeats to access to the display RAM, the column address counter is incremented during each access until address BFH is accessed (In horizontal addressing mode). Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

	A0	RD(E)	WR (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
Column Start High	0	1	0	0	0	0	1	A7	A6	A5	A4
Column Start Low bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Display address
0	0	0	0	0	0	0	0	0 (Column Start RESET)
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
1	0	1	1	1	1	1	0	BEH
1	0	1	1	1	1	1	1	BFH

Note: Don't use any command not mentioned above.

This command cannot be used if user has written the 21H for column start and end address.

3. Set Row Start Address of Display RAM: (Double Bytes Command)

Specify Row address to load display RAM data to Row address register. Any RAM data bit can be accessed when its row address and column address are specified. The display remains unchanged even when the Row address is changed.

- Row address Mode Setting: (B0H)

A0	RD(E)	WR (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	0	0	0	0

- Row address setting:

Row Start	A0	RD(E)	WR (R/W)	D7	D6	D5	D4	D3	D2	D1	D0
	0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Row address
0	0	0	0	0	0	0	0	0 (Row Start RESET)
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
...
0	0	0	1	1	1	0	1	7DH
0	0	0	1	1	1	1	0	7EH
0	0	0	1	1	1	1	1	7FH

Note: Don't use any commands not mentioned above.

This command cannot be used if user has written the 22H for row start and end address.

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4. Set Column Start and End Address : (21H)

This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. In horizontal addressing mode, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

	A0	RD (E)	WR (R / W)	D7	D6	D5	D4	D3	D2	D1	D0
	0	1	0	0	0	1	0	0	0	0	1
	0	1	0	0	0	0	0	0	0	0	C0
Column Start	0	1	0	A7	A6	A5	A4	A3	A2	A1	A0
Column End	0	1	0	B7	B6	B5	B4	B3	B2	B1	B0

A7	A6	A5	A4	A3	A2	A1	A0	Display address
0	0	0	0	0	0	0	0	0 (Column Start RESET)
0	0	0	0	0	0	0	1	1
		:						:
1	0	1	1	1	1	1	0	BEH
1	0	1	1	1	1	1	1	BFH

B7	B6	B5	B4	B3	B2	B1	B0	Display address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
		:						:
1	0	1	1	1	1	1	0	BEH
1	0	1	1	1	1	1	1	BFH (Column End RESET)

C0	Column address setting Flag
0	Disable(RESET)
1	Enable

SP5140 internal SPEC

5. Set Row Start and End Address: (22H)

This triple byte command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. In vertical addressing mode, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address and the column address is incremented to the next column.

	A0	RD (E)	WR (R / W)	D7	D6	D5	D4	D3	D2	D1	D0
	0	1	0	0	0	1	0	0	0	1	0
	0	1	0	0	0	0	0	0	0	C0	0
Row Start	0	1	0	A7	A6	A5	A4	A3	A2	A1	A0
Row End	0	1	0	B7	B6	B5	B4	B3	B2	B1	B0

A7	A6	A5	A4	A3	A2	A1	A0	Display address
0	0	0	0	0	0	0	0	0 (Row Start RESET)
0	0	0	0	0	0	0	1	1
		:						:
0	1	1	1	1	1	1	0	7EH
0	1	1	1	1	1	1	1	7FH

B7	B6	B5	B4	B3	B2	B1	B0	Display address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
		:						:
0	1	1	1	1	1	1	0	7EH
0	1	1	1	1	1	1	1	7FH (Row End RESET)

C0	Row address setting Flag
0	Disable(RESET)
1	Enable

		SEG0	SEG1	SEG2	SEG3	---	SEG380	SEG381	SEG382	SEG383
	Address	00H		01H		---		BFH		BFH
COM0	00H									
COM1	01H									
COM2	02H									
COM3	03H									
---	---									
COM124	7CH									
COM125	7DH									
COM126	7EH									
COM127	7FH									

Column and Row Address Pointer Movement

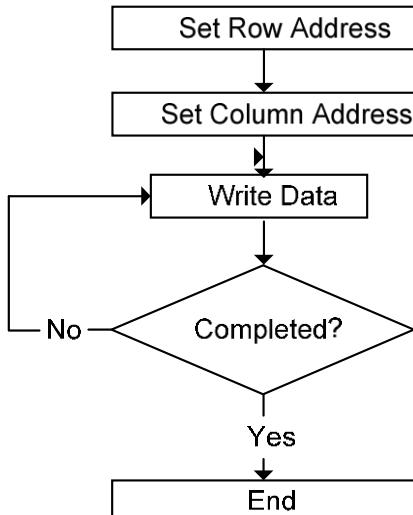


Figure 34 Write Ram flow

Once writing column start address and row start address for writing data to ram or reading data from ram, the position of ram for writing or reading should be pointed to the row & column start address setting. In horizontal addressing mode, after writing data to ram or reading data from ram, the column address will increase one automatically. When the column address reaches the column end address, it will be return to column start address and the row address will increase one. In vertical addressing mode, after writing data to ram or reading data from ram, the row address will increase one automatically. When the row address reaches the row end address, it will be return to row start address and the column address will increase one.

SP5140 internal SPEC

6. Set Memory addressing mode (20H)

There are two different memory addressing modes in SP5140: row addressing mode and vertical addressing mode. This command sets the way of memory addressing into one of the above two modes, "COL" means column.

A0	\overline{RD} (E)	\overline{WR} (R / \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	0	0	0
0	1	0	*	*	*	*	*	*	*	D

- Horizontal addressing mode (D=0) (RESET)

In Horizontal addressing mode, after the display RAM is read/ written, the column address is increased automatically by 1. If the column address reaches column end address, the column address is reset to column start address and row address is increased automatically by 1. When the Segment is remapped, the direction of both page and byte are reversed. The sequence of movement of the row and column address for row addressing mode is shown in figure 35-1.

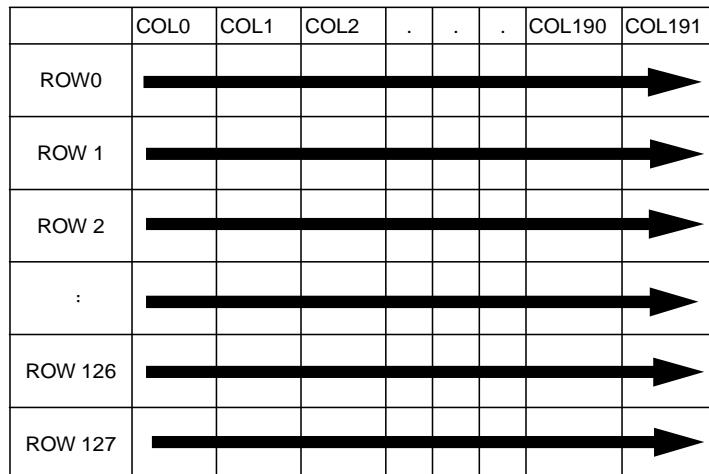


Figure35-1(a)

	Column	SEG0	SEG1	SEG2	SEG3	---	SEG382	SEG383	
Row	Address	00H				01H			
COM0	00H	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]	---	D191[3:0]	D191[7:4]	
COM1	01H	D192[3:0]	D192[7:4]	D193[3:0]	D193[7:4]	---	D383[3:0]	D383[7:4]	
COM2	02H	D384[3:0]	D384[7:4]	D385[3:0]	D385[7:4]	---	D575[3:0]	D575[7:4]	
COM3	03H	D576[3:0]	D576[7:4]	D577[3:0]	D577[7:4]	---	D767[3:0]	D767[7:4]	
---	---								
COM124	7CH	D23808[3:0]	D23808[7:4]	D23809[3:0]	D23809[7:4]	---	D23999[3:0]	D23999[7:4]	
COM125	7DH	D24000[3:0]	D24000[7:4]	D24001[3:0]	D24001[7:4]	---	D24191[3:0]	D24191[7:4]	
COM126	7EH	D24192[3:0]	D24192[7:4]	D24193[3:0]	D24193[7:4]	---	D24383[3:0]	D24383[7:4]	
COM127	7FH	D24384[3:0]	D24384[7:4]	D24385[3:0]	D24385[7:4]	---	D24575[3:0]	D24575[7:4]	

Figure35-1(b)

Figure35-1 Horizontal addressing mode (Seg-remap=0)

SP5140 internal SPEC

- Vertical addressing mode: (D=1)

In vertical addressing mode, after the display RAM is read/ written, the row address is increased automatically by 1. If the row address reaches the row end address, the row address is reset to row start address and column address is increased automatically by 1. When the Segment is remapped, the direction of both page and byte are reversed. The sequence of movement of the page and column address for vertical addressing mode is shown in Figure 35-3.

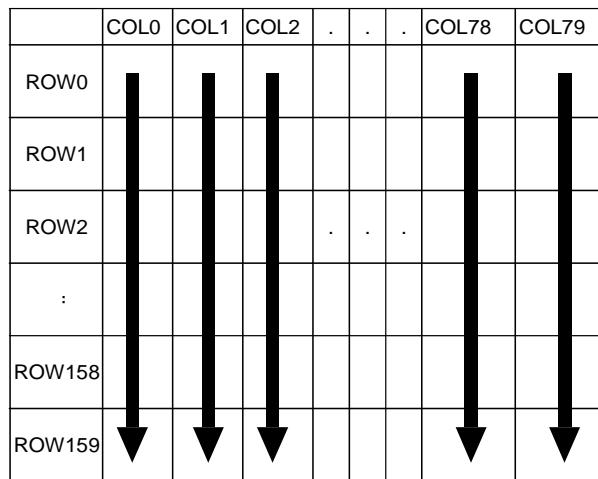


Figure 35-3 (a)

	Column	SEG0	SEG1	SEG2	SEG3	---	SEG158	SEG159
Row	Address	00H		01H		---	4FH	
COM0	00H	D0[3:0]	D0[7:4]	D128[3:0]	D128[7:4]	---	D24448[3:0]	D24448 [7:4]
COM1	01H	D1[3:0]	D1 [7:4]	D129[3:0]	D129[7:4]	---	D24449 [3:0]	D24449 [7:4]
COM2	02H	D2[3:0]	D2[7:4]	D130[3:0]	D130[7:4]	---	D24450 [3:0]	D24450 [7:4]
COM3	03H	D3[3:0]	D3[7:4]	D131[3:0]	D131[7:4]	---	D24451 [3:0]	D24451 [7:4]
---	---							
COM124	7CH	D124[3:0]	D124[7:4]	D254[3:0]	D254[7:4]	---	D24572 [3:0]	D24572 [7:4]
COM125	7DH	D125[3:0]	D125[7:4]	D254[3:0]	D254[7:4]	---	D24573 [3:0]	D24573 [7:4]
COM126	7EH	D126[3:0]	D126[7:4]	D254[3:0]	D254[7:4]	---	D24574 [3:0]	D24574 [7:4]
COM127	7FH	D127[3:0]	D127[7:4]	D255[3:0]	D255[7:4]	---	D24575[3:0]	D24575 [7:4]

Figure35-3 (b)
Figure 35-3 Vertical addressing mode (Seg remap=0)

SP5140 internal SPEC

7. Set Breathing/dimming Display Effect (23H): (Double Bytes Command)

This command set Breathing Display Effect ON/OFF and Time Interval.

- Breathing Display Effect Set: (23H)

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	0	1	1
0	1	0	ON/OFF	TEST	MODE	A4	A3	A2	A1	A0
0	1	0	0	C2	C1	C0	0	B2	B1	B0

- ON/OFF set:

When ON/OFF = "L", Breathing/dimming Display Effect OFF. (RESET)

When ON/OFF = "H", Breathing/dimming Display Effect ON.

- MODE

When Mode = "L", Breathing mode. (RESET)

When Mode = "H", dimming mode, maximum Brightness is decided contrast (81h).

- TEST

When TEST = "L", Breath light test mode is disable. (Default)

When TEST = "H", Breath light test mode is enable. (To change by line)

- Breathing Display Effect Maximum Brightness Adjust Set: (A4 – A3)

A4	A3	Maximum Brightness (Contrast+1)
0	0	256(RESET)
0	1	128
1	0	64
1	1	32

- Breathing/dimming Effect Time Interval Set: (A2 – A0)

A2	A1	A0	Time Interval step
0	0	0	1 Frames
0	0	1	2 Frames(RESET)
0	1	0	3 Frames
:	:	:	:
1	1	0	7 Frames
1	1	1	8 Frames

- Breathing Display t Dark Time Interval Set: (B2 – B0)

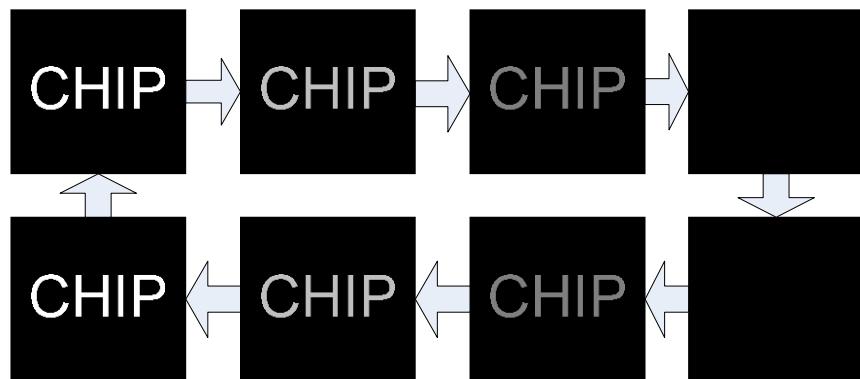
B2	B1	B0	Time Interval step
0	0	0	+0 Frame
0	0	1	+25 Frames (RESET)
0	1	0	+50 Frames
0	1	1	+100 Frames
1	0	0	+150 Frames
1	0	1	+200 Frames
1	1	0	+250 Frames
1	1	1	+300 Frames

SP5140 internal SPEC

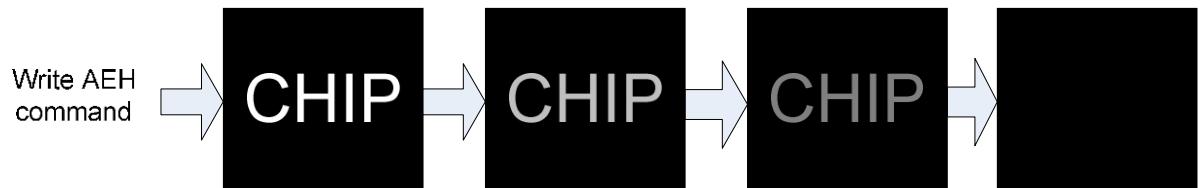
Breathing Display Effect Brightest Time Interval Set: (C2 – C0)

C2	C1	C0	Time Interval step
0	0	0	+0 Frame
0	0	1	+25 Frames
0	1	0	+50 Frames
0	1	1	+100 Frames
1	0	0	+150 Frames
1	0	1	+200 Frames
1	1	0	+250 Frames
1	1	1	+300 Frames

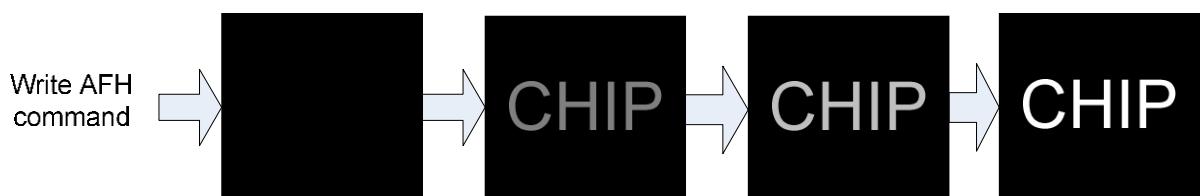
Breathing Display effect:



Gradual down Display effect:



Gradual up Display effect:



Note:

1. AEH isn't allowed to be written before AFH dimming ends.
2. AFH isn't allowed to be written before AEH dimming ends.
3. If AEH is written before AFH dimming ends, AFH dimming will run to the end, and then AEH dimming runs to the end.
4. If AFH is written before AEH dimming ends, AEH dimming will run to the end, and then dimming must be disable.
5. If dimming ON and AEH are written in the same frame, dimming ON will be invalid.

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8. Set Horizontal Scroll & Vertical Scroll (24H-27H): (Six Bytes Command)

This command consists of 6 consecutive bytes to set up the horizontal scroll and the vertical scroll parameters. It determined the scrolling start column, end column, start row, end row and time interval.

Before issuing this command, the horizontal scroll must be deactivated (2EH). Otherwise, ram content may be corrupted.

- Horizontal Scroll & Vertical Scroll Setup Mode Set: (24H-27H)

A0	E RD	R / W <u>WR</u>	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	1	D1	D0
0	1	0	*	*	*	*	*	*	*	A8
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	*	*	*	*	*	*	*	B8
0	1	0	B7	B6	B5	B4	B3	B2	B1	B0
0	1	0	C7	C6	C5	C4	C3	C2	C1	C0
0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	*	*	*	*	E3	E2	E1	E0

D1	D0	Scroll Direction Set
0	0	Scroll Down
0	1	Scroll Up
1	0	Scroll Right(RESET)
1	1	Scroll Left

- Start Column Position Set: (A8 – A0)

A0	E RD	R / W <u>WR</u>	D8	D7	D6	D5	D4	D3	D2	D1	D0	Start Column Position
0	1	0	0	0	0	0	0	0	0	0	0	0(RESET)
0	1	0	0	0	0	0	0	0	0	0	1	1
0	1	0						:				:
0	1	0	1	0	1	1	1	1	1	1	0	382
0	1	0	1	0	1	1	1	1	1	1	1	383

- End Column Position Set: (B8 – B0)

A0	E RD	R / W <u>WR</u>	D8	D7	D6	D5	D4	D3	D2	D1	D0	End Column Position
0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	1	1
0	1	0						:				:
0	1	0	1	0	1	1	1	1	1	1	0	382
0	1	0	1	0	1	1	1	1	1	1	1	383(RESET)

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- Start Row Position Set: (C7 – C0)

A0	E RD	R/W <u>WR</u>	D7	D6	D5	D4	D3	D2	D1	D0	Start Row Position
0	1	0	0	0	0	0	0	0	0	0	0(RESET)
0	1	0	0	0	0	0	0	0	0	1	1
0	1	0					:				:
0	1	0	0	1	1	1	1	1	1	0	126
0	1	0	0	1	1	1	1	1	1	1	127

- End Row Position Set: (D7 – D0)

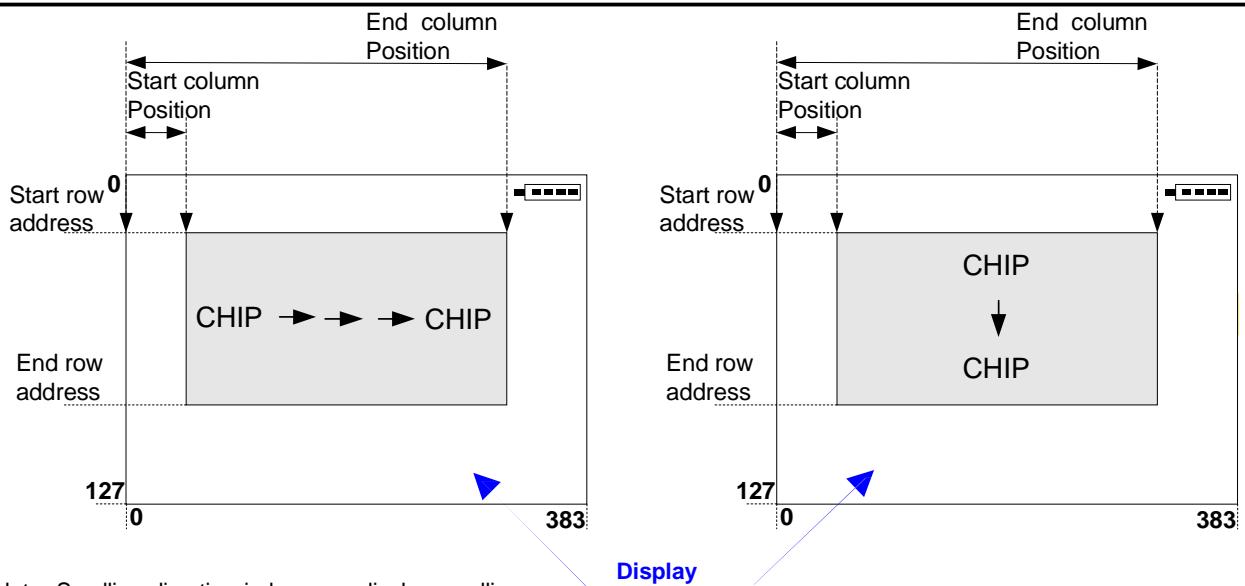
A0	E RD	R/W <u>WR</u>	D7	D6	D5	D4	D3	D2	D1	D0	End Row Position
0	1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1	1
0	1	0					:				:
0	1	0	0	1	1	1	1	1	1	0	126
0	1	0	0	1	1	1	1	1	1	1	127 (RESET)

- Time Interval Set: (E3 – E0)

A0	E RD	R/W <u>WR</u>	D7	D6	D5	D4	D3	D2	D1	D0	Time Interval
0	1	0	*	*	*	*	0	0	0	0	1 frames
0	1	0	*	*	*	*	0	0	0	1	2 frames
0	1	0	*	*	*	*	0	0	1	0	3 frames
0	1	0	*	*	*	*	0	0	1	1	4 frames
0	1	0	*	*	*	*	0	1	0	0	5 frames
0	1	0	*	*	*	*	0	1	0	1	6 frames(RESET)
0	1	0	*	*	*	*	0	1	1	0	7 frames
0	1	0	*	*	*	*	0	1	1	1	8 frames
0	1	0	*	*	*	*	1	0	0	0	9 frames
0	1	0	*	*	*	*	1	0	0	1	10 frames
0	1	0	*	*	*	*	1	0	1	0	11 frames
0	1	0	*	*	*	*	1	0	1	1	16 frames
0	1	0	*	*	*	*	1	1	0	0	32 frames
0	1	0	*	*	*	*	1	1	0	1	64 frames
0	1	0	*	*	*	*	1	1	1	0	128 frames
0	1	0	*	*	*	*	1	1	1	1	256 frames

Note: “*” stands for “Don’t care”.

SP5140 internal SPEC



SP5140 internal SPEC

9. Set Scroll Mode: (28H-2BH)

Control continuous or single screen scroll.

A0	E RD	R / W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	0	D1	D0

When D0="L", Continuous horizontal/vertical scroll. (RESET)

When D0="H", Single Screen scroll. Scrolled area is filled "0" data.

When D1="L", Disable write 1 Column/Row ram data for scrolling mode. (RESET)

When D1="H", Enable write 1 Column/Row ram data for scrolling mode.

D1 D0		Scroll mode
0	0	Continuous horizontal/vertical scroll(RESET)
0	1	Single Screen scroll
1	0	-
1	1	1 Column/Row scroll mode

10. Set Deactivate /Activate Scroll: (2EH - 2FH)

Stop or start motion of horizontal/vertical scrolling. This command should only be issued after horizontal/vertical scroll setup parameters (24H/25H/26H/27H/28H/29H/2BH) are defined.

A0	E RD	R / W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	1	1	D

When D="L", Stop motion of horizontal scroll. (RESET)

When D="H", Start motion of horizontal scroll.

Valid command sequence 1: 24h, XXh, XXh, XXh, XXh, XXh, XXh, XXh, 28h or 29h or 2Bh, 2Fh.

Valid command sequence 2: 25h, XXh, XXh, XXh, XXh, XXh, XXh, XXh, 28h or 29h or 2Bh, 2Fh

Valid command sequence 3: 26h, XXh, XXh, XXh, XXh, XXh, XXh, XXh, 28h or 29h or 2Bh, 2Fh

Valid command sequence 4: 27h, XXh, XXh, XXh, XXh, XXh, XXh, XXh, 28h or 29h or 2Bh, 2Fh

Valid command sequence 5: 27h, XXh, XXh, XXh, XXh, XXh, XXh, XXh, 28h or 29h or 2Bh, 2Fh

 今 2Eh 今 delay 1 fame

 今 27h, XXh, XXh, XXh, XXh, XXh, XXh, XXh, 28h or 29h or 2Bh, 2Fh

Note :

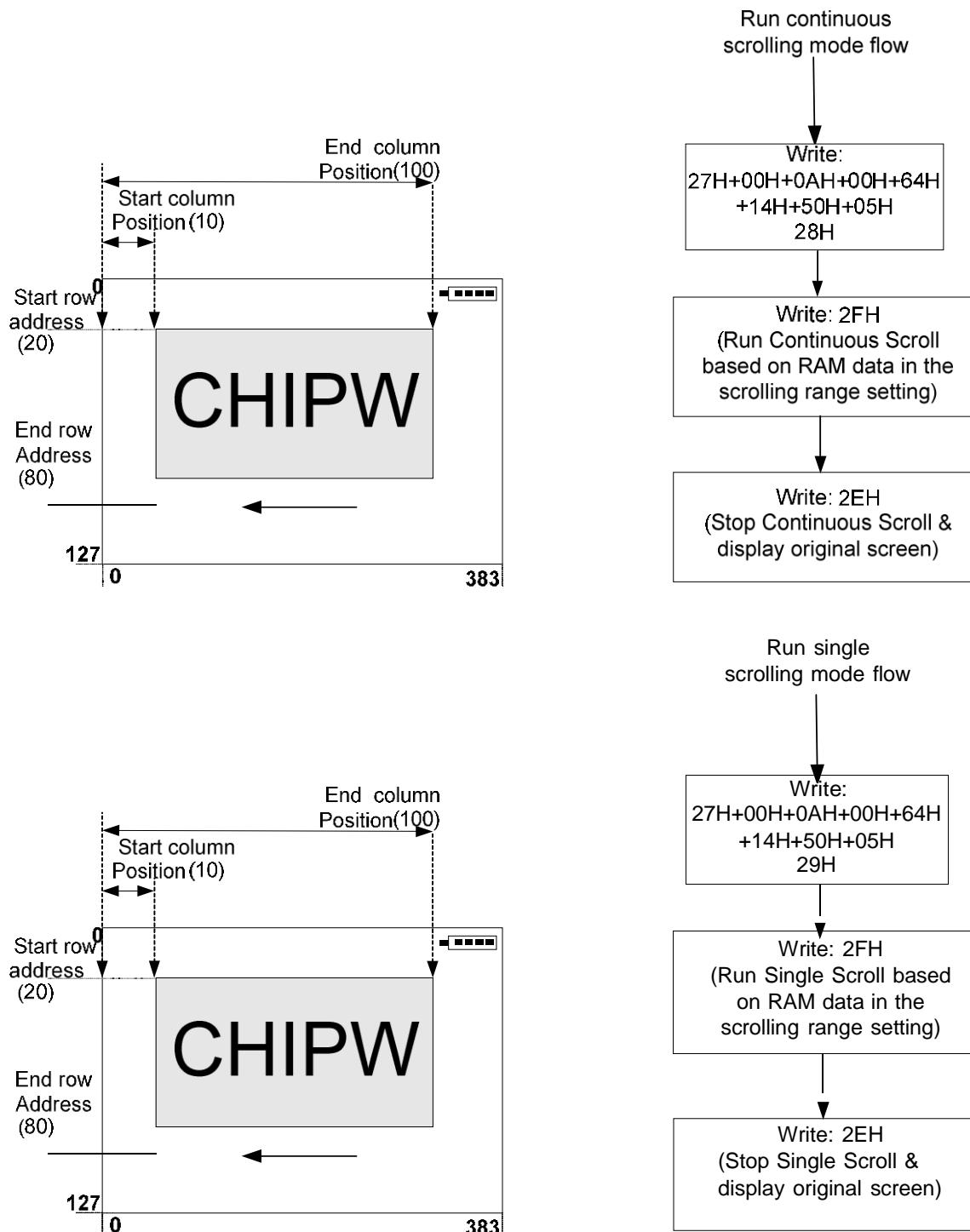
The following actions are prohibited after the horizontal scroll is activated

- Changing additional horizontal scroll setup parameters.
- Changing horizontal scroll setup parameters.
- Changing continuous or single screen scroll setup parameters.

After the deactivating horizontal scroll issued, the display of screen is reset to original status.

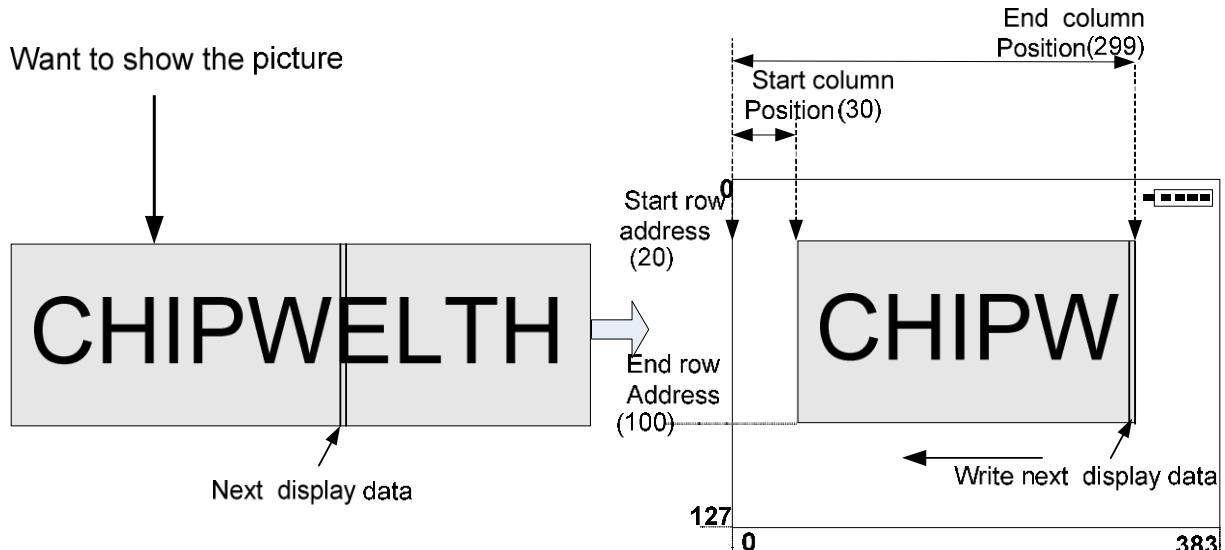
SP5140 internal SPEC

- Continuous scroll & Single scroll flow



SP5140 internal SPEC

- 1 Column/Row scroll flow



Step	Action	A0	Code	Notes
1	Set 1 column scrolling window : Row start position: 20 Row end position: 100 Column start position: 30 Column end position: 299	0	27H	Left and horizontal scroll
		0	00H	A[8] : Define higher start column position
		0	1EH	A[7:0] : Define lower start column position
		0	01H	B[8] : Define higher end column position
		0	2BH	B[7:0] : Define lower end column position
		0	14H	C[3:0] : Define start row position
		0	64H	D[3:0] : Define end row position
		0	2BH	Select 1 Column/Row scroll mode
		0	21H	Set RAM Column address range
2	Set updated ram address range	0	95H	Column start: (299-1)/2
		0	95H	Column end: (299-1)/2
		0	22H	Set RAM Row range
		0	14H	Row start
		0	64H	Row end
		-	-	Create "For loop" for 1 column scrolling
3	For i = 1 to n	0	2FH	Start scroll
4	Start scroll	-	-	Delay time of about 2 frames
5	Delay	-	-	Set time interval between each scroll step if necessary
6	Write the next display data to column address 95	1	-	Go to 3, when i>n, go to 9
7	Delay	-	-	Write 81 bytes data to the RAM
8	i=i+1	-	-	
9	End	-	-	

Note:

1. Two SEGs are scrolled together once.
2. Column start position must be even.
3. Column end position must be odd.
4. If set multi-ratio and start line, the following conditions must be met.
Start row \geq start line(A2H)
End row \leq multi-ratio(A8H) + start line(A2H)

11. Set Display Start Line: (A2H) (Double Bytes Command)

Specifies line address determine the initial display line or COM0. The RAM display data becomes the top line of OLED screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

- The Display Start line Mode Set: (A2H)

A0	E RD	R / W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	1	0

- The Display Start line Register Set: (00H – 7FH)

A0	E RD	R / W WR	D7	D6	D5	D4	D3	D2	D1	D0	COMx
0	1	0	0	0	0	0	0	0	0	0	0(RESET)
0	1	0	0	0	0	0	0	0	0	1	1
0	1	0	0	0	0	0	0	0	1	0	2
0	1	0			:						
0	1	0	0	1	1	1	1	1	1	0	126
0	1	0	0	1	1	1	1	1	1	1	127

COM pin	Multiplex ratio (A8) = 7Fh				Multiplex ratio (A8) = 3Fh			
	Display start line(A2H) =00h		Display start line(A2H) =0Ah		Display start line(A2H) =00h		Display start line(A2H) =0Ah	
COM0	Row 0		Row 10		Row 0		Row 10	
COM1	Row 1		Row 11		Row 1		Row 11	
COM2	Row 2		Row 12		Row 2		Row 12	
:	:		:		:		:	
:	:		:		:		:	
COM8	Row 8		Row 18		Row 8		Row 18	
COM9	Row 9		Row 19		Row 9		Row 19	
COM10	Row 10		Row 20		Row 10		Row 20	
COM11	Row 11		Row 21		Row 11		Row 21	
:	:		:		:		:	
:	:		:		:		:	
COM61	Row 61		Row 71		Row 61		Row 71	
COM62	Row 62		Row 72		Row 62		Row 72	
COM63	Row 63		Row 73		Row 63		Row 73	
COM64	Row 64		Row 74		-		-	
:	:		:		:		:	
COM116	Row 116		Row 126		-		-	
COM117	Row 117		Row 127		-		-	
COM118	Row 118		Row 0		-		-	
COM119	Row 119		Row 1		-		-	
COM120	Row 120		Row 2		-		-	
:	:		:		:		:	
COM124	Row 124		Row 6		-		-	
COM125	Row 125		Row 7		-		-	
COM126	Row 126		Row 8		-		-	
COM127	Row 127		Row 9		-		-	

Display start line COM output (C0H - COM0 to COM [N -1])

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COM pin	Multiplex ratio (A8) = 7Fh		Multiplex ratio (A8) = 3Fh	
	Display start line(A2H) =00h	Display start line(A2H) =0Ah	Display start line(A2H) =00h	Display start line(A2H) =0Ah
COM0	Row 127	Row 9	Row 63	Row 73
COM1	Row 126	Row 8	Row 62	Row 72
COM2	Row 125	Row 7	Row 61	Row 71
:	:	:	:	:
:	:	:	:	:
COM8	Row 119	Row 1	Row 55	Row 65
COM9	Row 118	Row 0	Row 54	Row 64
COM10	Row 117	Row 127	Row 53	Row 63
COM11	Row 116	Row 126	Row 52	Row 62
:	:	:	:	:
:	:	:	:	:
COM61	Row 66	Row 76	Row 2	Row 12
COM62	Row 65	Row 75	Row 1	Row 11
COM63	Row 64	Row 74	Row 0	Row 10
COM64	Row 63	Row 73	-	-
:	:	:	:	:
COM116	Row 11	Row 21	-	-
COM117	Row 10	Row 20	-	-
COM118	Row 9	Row 19	-	-
COM119	Row 8	Row 18	-	-
COM120	Row 7	Row 17	-	-
:	:	:	-	-
COM124	Row 3	Row 13	:	:
COM125	Row 2	Row 12	-	-
COM126	Row 1	Row 11	-	-
COM127	Row 0	Row 10	-	-

Display start line COM output (C8H - COM [N -1] to COM0)

12. Set Contrast Control Register: (81H) (Double Bytes Command)

This command is to set contrast setting of the display. The chip has 256 contrast steps from 00 to FF. The segment output current increases as the contrast step value increases. Segment output current setting: ISEG = $\alpha/256 \times IREF \times$ scale factor
Where: α is contrast step; IREF is reference current equals 9.375 μ A; Scale factor = 32

- The Contrast Control Mode Set: (81H)

When this command is input, the contrast data register set command becomes enabled. Once the contrast control mode has been set, no other command except for the contrast data register command can be used. Once the contrast data set command has been used to set data into the register, then the contrast control mode is released.

A0	E RD	R/W <u>WR</u>	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

- Contrast Data Register Set: (00H - FFH)

By using this command to set eight bits of data to the contrast data register; the OLED segment output assumes one of the 256 current levels. When this command is input, the contrast control mode is released after the contrast data register has been set.

A0	E RD	R/W <u>WR</u>	D7	D6	D5	D4	D3	D2	D1	D0	lseg
0	1	0	0	0	0	0	0	0	0	0	Small
0	1	0	0	0	0	0	0	0	0	1	
0	1	0	0	0	0	0	0	0	1	0	
0	1	0					:				:
0	1	0	1	0	0	0	0	0	0	0	RESET
0	1	0					:				:
0	1	0	1	1	1	1	1	1	1	0	
0	1	0	1	1	1	1	1	1	1	1	Large

When the contrast control function is not used, set the D7 - D0 to 1000,0000.

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13. Set External or internal IREF : (ADH)

IREF can be controlled by external resistor or internal resistor.

- IREF Register Set: (ADH)

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	1	0
0	1	0	*	*	*	*	*	A2	A1	A0

When A2 = "L", External resistor is selected(RESET).

When A2 = "H", Internal resistor is selected.

- Internal Resister Set: (A1 – A0)

A1	A0	I _{SEG} (uA)
0	0	300(RESET)
0	1	400
1	0	500
1	1	600

When VPP=15V,Contrast=256, RIref & I_{REF} Table(Just for reference):

R I _{REF}	I _{SEG} (uA)
1.3M	300
910K	400
750K	500
560K	600

Note: I_{REF} ≈ (VPP-2V) / RIref

14. Set Segment Re-map: (A0H - A1H)

Change the relationship between RAM row address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during OLED module assembly. For details, refer to the page address section of figure. When display data is written or read, the column address or page address (depends on the memory addressing mode) is incremented by 1 as shown in flowing figure

A0	\overline{RD} (E)	\overline{WR} (R / \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	ADC

When ADC = "L", the down rotates (normal direction). (RESET)

When ADC = "H", the up rotates (reverse direction).

Note: The command is executed directly.

15. Set Entire Display OFF/ON: (A4H - A5H)

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.

This command has priority over the normal/reverse display command.

A0	\overline{RD} (E)	\overline{WR} (R / \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D = "L", the normal display status is provided. (RESET)

When D = "H", the entire display ON status is provided.

Note: When A5H and ABH are sent to SP5140, the last written command is effective.

16. Set Black Display OFF/ON: (AAH - ABH)

Forcibly turns the black display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.

This command has priority over the normal/reverse display command.

A0	\overline{RD} (E)	\overline{WR} (R / \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	1	D

When D = "L", the normal display status is provided. (RESET)

When D = "H", the black display ON status is provided.

Note: When A5H and ABH are sent to SP5140, the last written command is effective.

17. Set Normal/Reverse Display: (A6H -A7H)

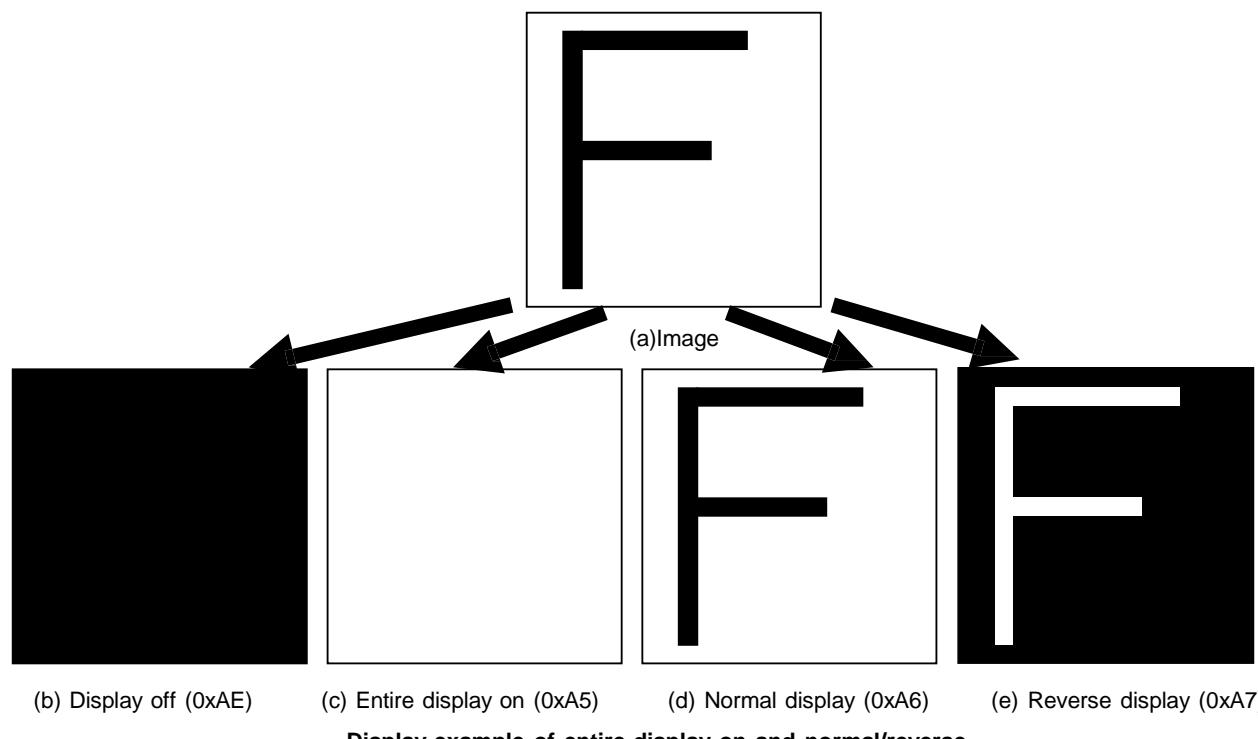
Reverse the display ON/OFF status without rewriting the contents of the display data RAM.

A0	RD (E)	WR (R / W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D = "L", the RAM data is high, being OLED ON potential (normal display). (RESET)

When D = "H", the RAM data is low, being OLED ON potential (reverse display)

The display example of Entire display off/on and normal/reverse command are showed in flowing figure.



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18. Set Multiplex Ratio: (A8H) (Double Bytes Command)

This command switches RESET 128 multiplex modes to any multiplex ratio from 1 to 128. The output pads COM0-COM127 will be switched to corresponding common signal.

- Multiplex Ratio Mode Set: (A8H)

A0	\overline{RD}	\overline{WR} R/\overline{W}	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	0

- Multiplex Ratio Data Set: (00H – 7FH)

A0	\overline{RD} (E)	\overline{WR} (R/ \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0	Multiplex Ratio
0	1	0	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	0	0	1	2
0	1	0	0	0	0	0	..	0	1	1	3
0	1	0				
0	1	0	0	1	1	1	1	1	1	0	127
0	1	0	0	1	1	1	1	1	1	1	128(RESET)

19. Set Grayscale/Mono display mode (ACH): (Double Bytes Command)

This command switches mono or gray mode.

A0	\overline{RD} (E)	\overline{WR} (R/ \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	0
0	1	0	*	*	*	A4	*	*	*	A0

When A0 = "L", the grayscale display mode is provided. (RESET)

When A0 = "H", the mono display mode is provided.

When A4 = "L", In mono mode and sleep mode, A4 must be "L". (RESET)

When A4 = "H", In sleep mode, A4="H" can save current.

Note: In mono mode, RAM is written by gray mode, and read by gray mode.

20. Display OFF/ON: (AEH - AFH)

Alternatively turns the display on and off.

A0	\overline{RD} (E)	\overline{WR} (R/ \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

When D = "L", Display OFF OLED. (RESET)

When D = "H", Display ON OLED.

When the display OFF command is executed, power saver mode will be entered.

Sleep mode:

This mode stops every operation of the OLED display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

- (1) Stops the oscillator circuit.
- (2) Stops the OLED drive and outputs Hiz as the segment/common driver output.
- (3) Holds the display data and operation mode provided before the start of the sleep mode.
- (4) The MPU can access to the built-in display RAM.

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21. Set Gray Scale Table: (B8H) (Double Bytes Command)

This command is used to set each individual gray scale level for the display. Gray scale levels GS0 that has no pre-charge and current drive, each gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK.

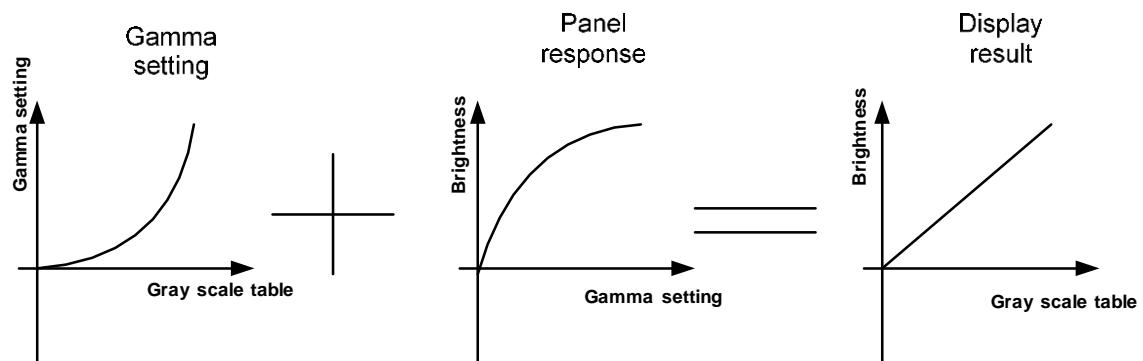
Following the command B8h, the user has to set the gray scale for GS1, GS2... GS14, GS15 one by one in sequence. The setting of gray scale table can perform gamma correction on panel display. Since the perception of the brightness scale shall match the image data value in display data RAM, appropriate gray scale table setting can compensate this effect.

- Gray Scale Table Setting: (B8H)

A0	E RD	R / W WR	D7	D6	D5	D4	D3	D2	D1	D0
	1	0	1	0	1	1	1	0	0	0

- Gamma curve setting is 6 bits data format:

A0	RD (E)	WR (R / W)	D5	D4	D3	D2	D1	D0	· PWM-driving	
									· RESET (hex)	
0	1	0			GS0[5:0]					0
0	1	0			GS1[5:0]					4
0	1	0			GS2[5:0]					8
0	1	0			GS3[5:0]					12
0	1	0			GS4[5:0]					16
0	1	0			GS5[5:0]					20
0	1	0			GS6[5:0]					24
0	1	0			GS7[5:0]					28
0	1	0			GS8[5:0]					32
0	1	0			GS9[5:0]					36
0	1	0			GS10[5:0]					40
0	1	0			GS11[5:0]					44
0	1	0			GS12[5:0]					48
0	1	0			GS13[5:0]					52
0	1	0			GS14[5:0]					56
0	1	0			GS15[5:0]					60



Note : The GS15 must be larger than GS1~GS14.

22. Set Linear Gray Scale Table Setting: (BAH)

This signal byte command is used to reloads linear gray scale level for the display GP0~15 is a RESET linear gray scale level.

RAM Data(4 bits)	Gamma Setting (Command B8h)	RESET Gamma Setting for PWM-driving (Command BAh) (hex)
0000	GS0	0 (note)
0001	GS1	4
0010	GS2	8
0011	GS3	12
0100	GS4	16
0101	GS5	20
0110	GS6	24
0111	GS7	28
1000	GS8	32
1001	GS9	36
1010	GS10	40
1011	GS11	44
1100	GS12	48
1101	GS13	52
1110	GS14	56
1111	GS15	60

The example of gray scale compensate panel display

Note: When GS0 = 0, pre-charge off.. When GS0 > 0, pre-charge on.

23. Set Common Output Scan Direction: (C0H – C8H)

This command sets the scan direction of the common output allowing layout flexibility in OLED module design. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will be vertically flipped.

A0	\overline{RD} (E)	\overline{WR} (R / \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0
	1	0	1	1	0	0	D	*	*	*

When D = "L", Scan from COM0 to COM [N -1]. (RESET)

When D = "H", Scan from COM [N -1] to COM0.

24. Set Display Offset (D3H): (Double Bytes Command)

This is a double byte command. The next command specifies the mapping of display start line to one of COM0-127 (it is assumed that COM0 is the display start line, that equals to 0). For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second byte should be given by 010000. To move in the opposite direction by 16 lines, the 6-bit data should be given by (128-16), so the second byte should be 01110000.

- Display Offset Mode Set: (D3H)

A0	E \overline{RD}	R / \overline{W} \overline{WR}	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	0	1	1

- Display Offset Data Set: (00H~7FH)

A0	\overline{RD} (E)	\overline{WR} (R / \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0	COMx
0	1	0	0	0	0	0	0	0	0	0	0(RESET)
0	1	0	0	0	0	0	0	0	0	1	1
0	1	0	0	0	0	0	0	0	1	0	2
0	1	0					
0	1	0	0	1	1	1	1	1	1	0	126
0	1	0	0	1	1	1	1	1	1	1	127

Note: “*” stands for “Don’t care”

COM pin	Multiplex ratio (A8) = 7Fh		Multiplex ratio (A8) = 3Fh	
	Display offset(D3H) =00h	Display offset(D3H) =0Ah	Display offset(D3H) =00h	Display offset(D3H) =0Ah
COM0	Row 0	Row 10	Row 0	Row 10
COM1	Row 1	Row 11	Row 1	Row 11
COM2	Row 2	Row 12	Row 2	Row 12
:	:	:	:	:
:	:	:	:	:
COM8	Row 8	Row 18	Row 8	Row 18
COM9	Row 9	Row 19	Row 9	Row 19
COM10	Row 10	Row 20	Row 10	Row 20
COM11	Row 11	Row 21	Row 11	Row 21
:	:	:	:	:
COM51	Row 51	Row 61	Row 51	Row 61
COM52	Row 52	Row 62	Row 52	Row 62
COM53	Row 53	Row 63	Row 53	Row 63
:	:	:	:	:

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:	:	:	:	:
COM61	Row 61	Row 71	Row 61	-
COM62	Row 62	Row 72	Row 62	-
COM63	Row 63	Row 73	Row 63	-
COM64	Row 64	Row 74	-	-
:	:	:	:	:
COM116	Row 116	Row 126	-	-
COM117	Row 117	Row 127	-	-
COM118	Row 118	Row 0	-	Row 0
COM119	Row 119	Row 1	-	Row 1
COM120	Row 120	Row 2	-	Row 2
:	:	:	:	:
COM124	Row 124	Row 6	-	Row 6
COM125	Row 125	Row 7	-	Row 7
COM126	Row 126	Row 8	-	Row 8
COM127	Row 127	Row 9	-	Row 9

Display offset COM output (C0H - COM0 to COM [N -1])

COM pin	Multiplex ratio (A8) = 7Fh		Multiplex ratio (A8) = 3Fh	
	Display offset(D3H) =00h	Display offset(D3H) =0Ah	Display offset(D3H) =00h	Display offset(D3H) =0Ah
COM0	Row 127	Row 9	Row 63	-
COM1	Row 126	Row 8	Row 62	-
COM2	Row 125	Row 7	Row 61	-
:	:	:	:	:
:	:	:	:	:
COM8	Row 119	Row 1	Row 55	-
COM9	Row 118	Row 0	Row 54	-
COM10	Row 117	Row 127	Row 53	Row 63
COM11	Row 116	Row 126	Row 52	Row 62
COM12	Row 115	Row 125	Row 51	Row 61
:	:	:	:	:
:	:	:	:	:
COM61	Row 66	Row 76	Row 2	Row 12
COM62	Row 65	Row 75	Row 1	Row 11
COM63	Row 64	Row 74	Row 0	Row 10
COM64	Row 63	Row 73	-	Row 9
:	:	:	:	:
:	:	:	:	:
COM71	Row 56	Row 66	-	Row 2
COM72	Row 55	Row 65	-	Row 1
COM73	Row 54	Row 64	-	Row 0
:	:	:	:	:
COM116	Row 11	Row 21	-	-
COM117	Row 10	Row 20	-	-
COM118	Row 9	Row 19	-	-
COM119	Row 8	Row 18	-	-
COM120	Row 7	Row 17	-	-
:	:	:	-	-
COM124	Row 3	Row 13	:	:
COM125	Row 2	Row 12	-	-
COM126	Row 1	Row 11	-	-
COM127	Row 0	Row 10	-	-

Display offset COM output (C8H - COM [N -1] to COM0)

25. Set Display Clock Divide Ratio/Oscillator Frequency (D5H): (Double Bytes Command)

This command is used to set the frequency of the internal display clocks (DCLKs). It is defined as the divide ratio used to divide the oscillator frequency. Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency.

- Divide Ratio/Oscillator Frequency Mode Set: (D5H)

A0	E RD	R / W <u>WR</u>	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	1	0	1

Divide Ratio/Oscillator Frequency Data Set: (00H - FFH)

A0	E RD	R / W <u>WR</u>	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A7	A6	A5	A4	*	A2	A1	A0

A3 – A0 defines the divide ration of the display clocks (DCLK).

A2	A1	A0	Divide Ratio
0	0	0	1(RESET)
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

A7 – A4 sets the oscillator frequency. Oscillator frequency increase with the value of A[7:4] and vice versa.

A7	A6	A5	A4	Oscillator Frequency of f_{OSC}
0	0	0	0	-25%
0	0	0	1	-20%
0	0	1	0	-15%
0	0	1	1	-10%
0	1	0	0	-5%
0	1	0	1	f_{OSC} (POR)
0	1	1	0	+5%
0	1	1	1	+10%
1	0	0	0	+15%
1	0	0	1	+20%
1	0	1	0	+25%
1	0	1	1	+30%

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1	1	0	0	+35%
1	1	0	1	+40%
1	1	1	0	+45%
1	1	1	1	+50%

Note: 8080/6800 interface speed is less than oscillator frequency.

26. Set Discharge Period (D8H): (Two Bytes Command)

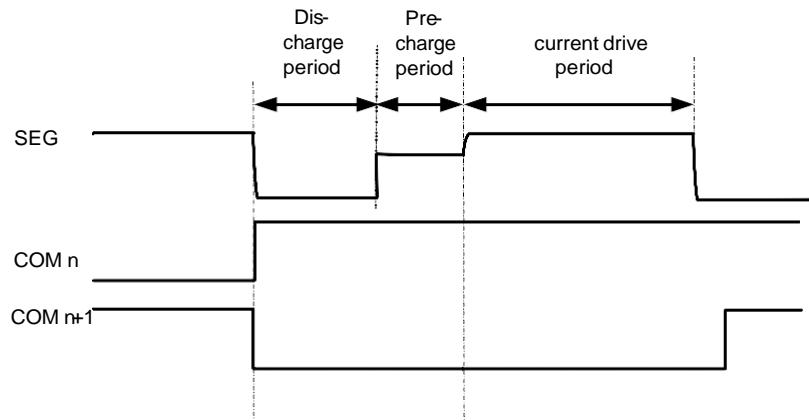
This command is used to set the duration of the discharge period3. The interval is counted in number of DCLK.

- Discharge Period3 Set: (D8H)

A0	RD(E)	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	0	0
0	1	0	*	*	*	A4	A3	A2	A1	A0

Discharge Period Adjust : (A4 - A0)

A4	A3	A2	A1	A0	Discharge Period
0	0	0	0	0	3DCLK
0	0	0	0	1	3 DCLK
0	0	0	1	0	3 DCLK
0	0	0	1	1	3 DCLK (RESET)
0	:	:	:	:	:
1	1	1	1	0	30 DCLK
1	1	1	1	1	31 DCLK



27. Set Pre-charge Period2 (D9H): (Two Bytes Command)

This command is used to set the duration of the pre-charge period2. The interval is counted in number of DCLK.

Drive mode: VSEGH drive.

- Pre-charge Period2 Set: (D9H)

A0	\overline{RD} (E)	\overline{WR} (R / \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	0	1
0	1	0	0	0	0	A4	A3	A2	A1	A0

Pre-charge Period2 Adjust : (A4 - A0)

A4	A3	A2	A1	A0	Pre-charge Period2
0	0	0	0	0	0 DCLK
0	0	0	0	1	1 DCLK
:	:	:	:	:	:
0	0	1	0	0	4 DCLK (RESET)
:	:	:	:	:	:
1	1	1	1	0	30 DCLK
1	1	1	1	1	31 DCLK

28. Set SEG pads hardware configuration: (DAH) (Double Bytes Command)

This command is to set the SEG signals pad configuration to match the OLED panel hardware layout.

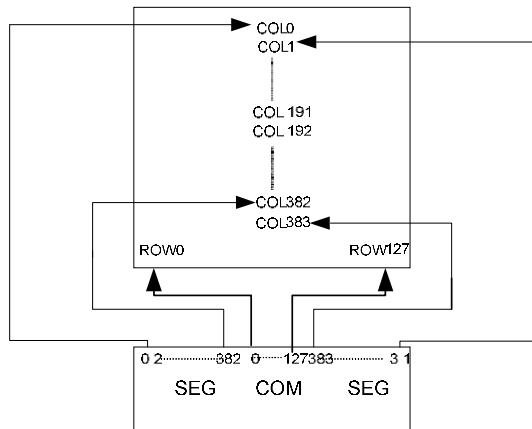
- SEG Pads Hardware Configuration Mode Set: (DAH)

A0	E RD	R / W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	1	0
0	1	0	0	0	0	0	0	0	0	A0

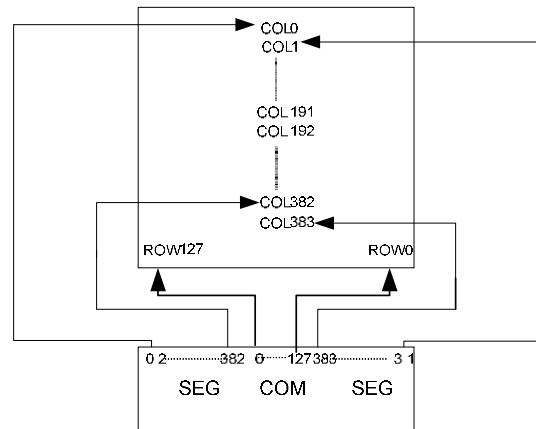
When A0 = "L", Even on the left. (RESET)

When A0 = "H", Even on the right.

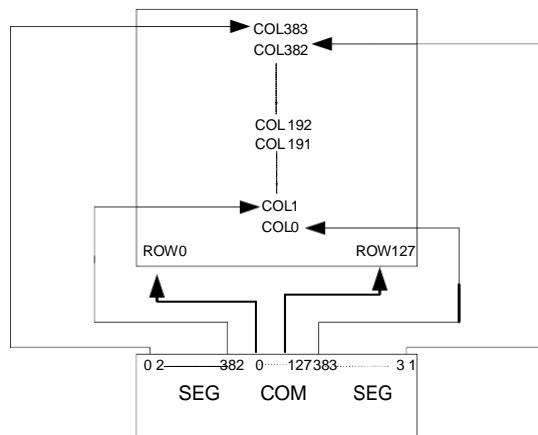
Please see the following figure for Set Segment Re-map and SEG pads hardware configuration.



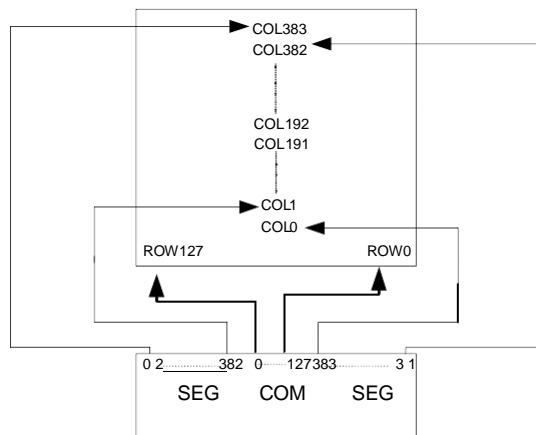
(1) DAH=00 , A0H(SEG0 to SEG383),
C0H(COM0 to COM[N-1])



(2) DAH=00 , A0H(SEG0 to SEG383),
C8H(COM[N-1] to COM0)

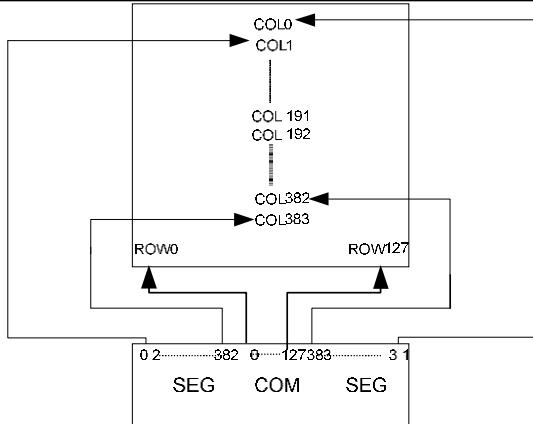


(3) DAH=00 , A1H(SEG383 to SEG0),
C0H(COM0 to COM[N-1])

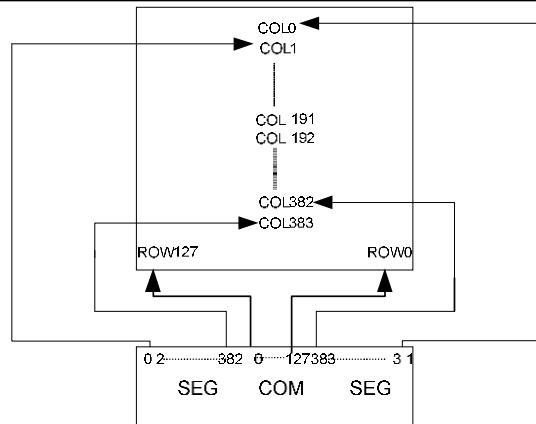


(4) DAH=00 , A1H(SEG383 to SEG0),
C8H(COM[N-1] to COM0)

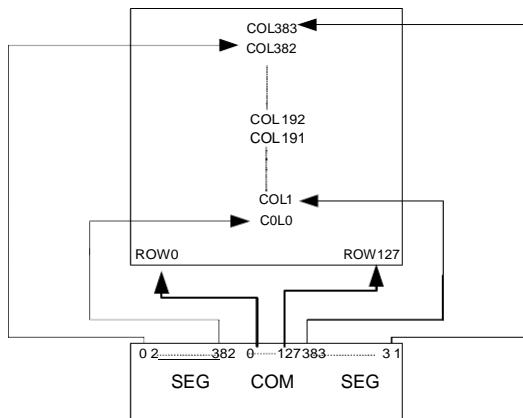
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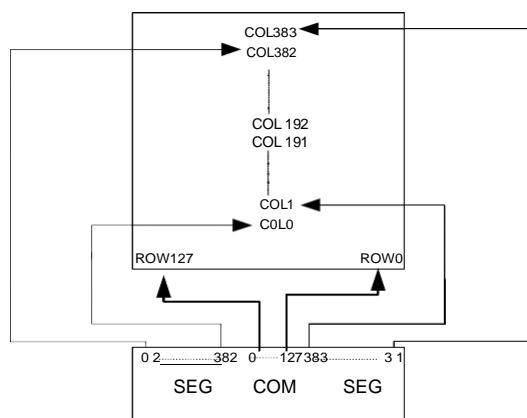
(5) DAH=01 , A0H(SEG0 to SEG383),
C0H(COM0 to COM[N-1])



(6) DAH=01 , A0H(SEG0 to SEG383),
C8H(COM[N-1] to COM0)



(7) DAH=01 , A1H(SEG383 to SEG0),
C0H(COM0 to COM[N-1])



(8) DAH=01 , A1H(SEG383 to SEG0),
C8H(COM[N-1] to COM0)

SEG pads hardware configuration

29. Set VCOM Deselect Level: (DBH) (Double Bytes Command)

This command is to set the common pad output voltage level at deselect stage.

VCOM Deselect Level Mode Set: (DBH)

A0	\overline{RD} (E)	\overline{WR} (R / \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	1	1

VCOM Deselect Level Data Set: (00H - FFH)

A0	\overline{RD} (E)	\overline{WR} (R / \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

$$VCOMH = \beta_1 \times VPP = (0.430 + A[7:0] \times 0.006415) \times VPP$$

A[7:0]	β_1	A[7:0]	β_1
00H	0.430	20H	0.635
01H	0.436	21H	0.642
02H	0.442	22H	0.648
03H	0.449	23H	0.654
04H	0.456	24H	0.661
05H	0.462	25H	0.667
06H	0.468	26H	0.674
07H	0.475	27H	0.680
08H	0.481	28H	0.687
09H	0.488	29H	0.693
0AH	0.494	2AH	0.699
0BH	0.501	2BH	0.706
0CH	0.507	2CH	0.712
0DH	0.513	2DH	0.719
0EH	0.520	2EH	0.725
0FH	0.526	2FH	0.731
10H	0.533	30H	0.738
11H	0.539	31H	0.744
12H	0.546	32H	0.751
13H	0.552	33H	0.757
14H	0.558	34H	0.764
15H	0.565	35H	0.770(POR)
16H	0.571	36H	0.776
17H	0.578	37H	0.783
18H	0.584	38H	0.789
19H	0.590	39H	0.796
1AH	0.596	3AH	0.802
1BH	0.603	3BH	0.808
1CH	0.610	3CH	0.815
1DH	0.616	3DH	0.821
1EH	0.622	3EH	0.828
1FH	0.629	3FH	0.834
40H - FEH	1	FFH	External

30. Pre-charge VSEGH Level control (DCH): (Double Bytes Command).

This command is to set the segment pad output voltage level at pre-charge stage.

A0	E RD	R / W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	1	0	1
0	1	0	*	*	*	A4	A3	A2	A1	A0

- VSEGH level control: (A4 - A0)

VSEGH[4:0] : VSEGH = N x Vpp

A[4:0]	N	A[4:0]	β_1
00H	0.100	10H	0.500
01H	0.125	11H	0.525
02H	0.150	12H	0.550
03H	0.175	13H	0.575
04H	0.200	14H	0.600
05H	0.225	15H	0.625
06H	0.250	16H	0.650
07H	0.275	17H	0.675
08H	0.300	18H	0.700
09H	0.325	19H	0.725
0AH	0.350	1AH	0.750
0BH	0.375	1BH	0.775
0CH	0.400	1CH	0.800
0DH	0.425	1DH	0.825
0EH	0.450	1EH	0.850
0FH	0.475(RESET)	1FH	External

Note: VSEGH must be less than VCOMH.

31. Set Discharge VSL Level (DDH)

This command is to set the Segment output discharge voltage level.

A0	\overline{RD} (E)	\overline{WR} (R / \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	1	0	1
0	1	0	*	*	*	A4	A3	A2	A1	A0

This command is to set the segment discharge voltage level

- VSL level control: (A4 - A0)

A[4:0]	VSL	A[4:0]	VSL
00H	0.000 VPP(RESET)	10H	0.2875 VPP
01H	0.1000 VPP	11H	0.3000 VPP
02H	0.1125 VPP	12H	0.3125 VPP
03H	0.1250 VPP	13H	0.3250 VPP
04H	0.1375 VPP	14H	0.3375 VPP
05H	0.1500 VPP	15H	0.3500 VPP
06H	0.1625 VPP	16H	0.3625 VPP
07H	0.1750 VPP	17H	0.3750 VPP
08H	0.1875 VPP	18H	0.3875 VPP
09H	0.2000 VPP	19H	0.4000 VPP
0AH	0.2125 VPP	1AH	0.4125 VPP
0BH	0.2250 VPP	1BH	0.4250 VPP
0CH	0.2375 VPP	1CH	0.4375 VPP
0DH	0.2500 VPP	1DH	0.4500 VPP
0EH	0.2625 VPP	1EH	0.4625 VPP
0FH	0.2750 VPP	1FH	0.4750 VPP

32. Read-Modify-Write: (E0H)

A pair of Read-Modify-Write and End commands must always be used. In page addressing mode, once read-modify-write is issued, column address is not incremental by read display data command but incremental by write display data command only. In vertical addressing mode, once read-modify-write is issued, page address is not incremental by read display data command but incremental by write display data command only. It continues until End command is issued. When the End is issued, column address or page address (it depends on the addressing mode) returns to the address when read-modify-write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	\overline{RD} (E)	\overline{WR} (R / W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Cursor display sequence:

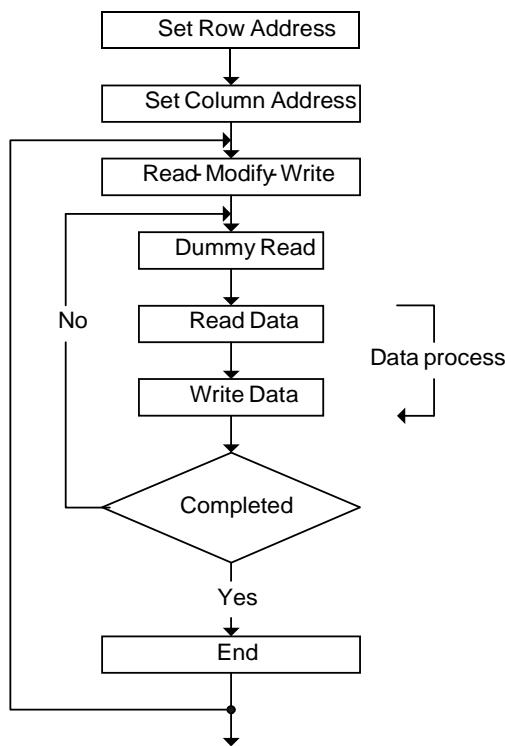


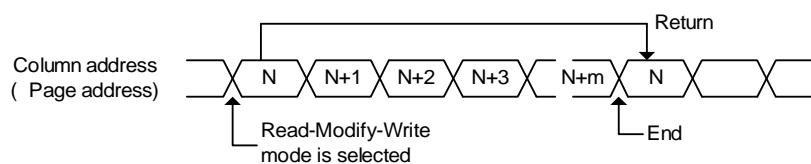
Figure 36

Note. The size of data to write or read per time is one byte.

33. End: (EEH)

Cancels Read-Modify-Write mode and returns column address or page address (it depends on the RAM addressing mode) to the original address (when Read-Modify-Write is issued.)

A0	\overline{RD} (E)	\overline{WR} (R / \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



34. NOP: (E3H)

No Operation Command.

A0	\overline{RD} (E)	\overline{WR} (R / \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

35. Read Panel ID (only-read): (E1H)

This command is to read Panel ID by hardware pin ID0&ID1 setting.

A0	\overline{RD} (E)	\overline{WR} (R / \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	0	0	0	0	1
1	0	1	*	*	*	*	*	*	ID1	ID0

36. Read IC ID (only-read): (E2H)

This command is to read IC ID. The output bits 101000 (it means SP5140).

A0	\overline{RD} (E)	\overline{WR} (R / \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	0	0	0	1	0
1	0	1	BUSY	ON/OFF	IC ID[5:0]					

BUSY: When high, the SP5140 is busy due to internal operation or reset. Any command is rejected until BUSY goes low.
The busy check is not required if enough time is provided for each cycle.

Note: When OSC disable, BUSY=0. When OSC enable, BUSY=1.

ON/OFF: Indicates whether the display is on or off. When it goes low, the display turns on. When it goes high, the display turns off. This is the opposite of Display ON/OFF command.

ID : These bits contain the information of the chip. The output bits 101000(it means SP5140).

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37. Read RAM Key in SPI interface(5AH)

A0	\overline{RD} (E)	\overline{WR} (R/ \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	1	1	0	1	0

38. Read command Key in SPI interface(5BH)

A0	\overline{RD} (E)	\overline{WR} (R/ \overline{W})	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	1	1	0	1	1

39. SPI read data output mode (92H)

When Serial Interface (SPI) is selected, control data output to pin D1 or D2 in read command or ram.

A0	E \overline{RD}	R/ \overline{W} \overline{WR}	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	1	0	0	1	0
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

A[7:0] = 0x00, SPI data output to pin D2. (RESET)

A[7:0] = 0x69, SPI data output to pin D1.

Command Table

Command	Code											Function	
	A0	<u>RD</u>	<u>WR</u>	D7	D6	D5	D4	D3	D2	D1	D0		
1. Set Lower Column Start Address (00H-0FH)	0	1	0	0	0	0	0	Lower column start address				Sets 4 lower bits of column start address of display RAM in register. (RESET = 00H)	
2. Set Higher Column Start Address (10H-1BH)	0	1	0	0	0	0	1	0	Higher column start address			Sets 4 higher bits of column start address of display RAM in register. (RESET = 10H)	
3. Set Row Start Address of Display RAM (B0H)	0	1	0	1	0	1	1	0	0	0	0	Specify Row address to load display RAM data to Row address register. (RESET=00H)	
	0	1	0	Row start address									
4. Set Column Start/End Address of Display RAM (21H)	0	1	0	0	0	1	0	0	0	0	1	Specifies column start/end address to load display RAM data to row address register. (C0 RESET = 0 Start address RESET = 00H, END address RESET = BFH)	
	0	1	0	0	0	0	0	0	0	0	C0		
	0	1	0	0	Column start address								
	0	1	0	0	Column end address								
5. Set Row Start/End Address of Display RAM (22H)	0	1	0	0	0	1	0	0	0	1	0	Specifies row start/end address to load display RAM data to row address register. (C0 RESET = 0 Start address RESET = 00H, END address RESET = 7FH)	
	0	1	0	0	0	1	0	0	0	1	0		
	0	1	0	Row start address									
	0	1	0	Row end address									
6. Set memory addressing mode (20H)	0	1	0	0	0	1	0	0	0	0	0	D = 1, Vertical Addressing Mode	
	0	1	0	*	*	*	*	*	*	*	D	D = 0, Horizontal Addressing Mode (RESET=00H)	
7. Set Breathing/dimming Display Effect (23H)	0	1	0	0	0	1	0	0	0	1	1	This command set Breathing/dimming Display Effect (RESET=01H)	
	0	1	0	ON/OFF	TEST	MOD E	A4	A3	A2	A1	A0		
8. Horizontal Scroll & Vertical Scroll Setup (24H-27H)	0	1	0	0	0	1	0	0	1	D1	D0	This command determined the scrolling direction (RESET=26H) and the scrolling start column (RESET=00H,00H), end column (RESET=01H,7FH), start row (RESET=00H), end row (RESET=7FH) position and time interval(RESET=05H). Before issuing this command, the horizontal/vertical scroll	
	0	1	0	*	*	*	*	*	*	*	A8		
	0	1	0	A7	A6	A5	A4	A3	A2	A1	A0		
	0	1	0	*	*	*	*	*	*	*	B8		
	0	1	0	B7	B6	B5	B4	B3	B2	B1	B0		
	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0		
	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0		

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	0	1	0	*	*	*	*	*	E2	E1	E0	must be deactivated (2EH).
9. Set Scroll Mode (28H-2BH)	0	1	0	0	0	1	0	1	0	D1	D0	Control continuous/single screen scroll and the way of writing all ram data or 1 column/row ram data for scrolling. (RESET=28H)
10. Set Deactivate/Activate Horizontal Scroll (2EH-2FH)	0	1	0	0	0	1	0	1	1	1	D	This command is to Stop or start motion of horizontal/vertical scrolling. (RESET=2EH)
11. Set Display Start Line(A2H)	0	1	0	1	0	1	0	0	0	1	0	Specifies line address to determine the initial display line or COM0.(RESET=00H)
	0	1	0	Display Start line Set								
12. The Contrast Control Mode Set Contrast Data Register Set(81H)	0	1	0	1	0	0	0	0	0	0	1	This command is to set Contrast Setting of the display.
	0	1	0	Contrast Data								The chip has 256 contrast steps from 00 to FF. (RESET = 80H)
13. External or internal IREF Set(ADH)	0	1	0	1	0	0	0	0	0	1	0	IREF can be controlled by external resister or internal resister.(RESET=00H)
	0	1	0	*	*	*	*	*	A2	A1	A0	
14. Set Segment Re-map (ADC) (A0H-A1H)	0	1	0	1	0	1	0	0	0	0	ADC	The down (0) or up (1) rotation. (RESET = A0H)
15. Set Entire Display OFF/ON(A4H-A5H)	0	1	0	1	0	1	0	0	1	0	D	Selects normal display (0) or Entire Display ON (1). (RESET = A4H)
16. Set Black Display OFF/ON (AAH-ABH)	0	1	0	1	0	1	0	1	0	1	D	Set Black Display OFF/ON (RESET = AAH)
17. Set Normal/Reverse Display (A6H-A7H)	0	1	0	1	0	1	0	0	1	1	D	Normal indication (0) when low, but reverse indication (1) when high. (RESET = A6H)
18. Set Multiplex Ratio (A8H)	0	1	0	1	0	1	0	1	0	0	0	This command switches RESET 160 multiplex modes to any multiplex ratio from 1 to160.(RESET=7FH)
	0	1	0	Resolution set								
19. Set Grayscale/Mono display mode (ACH)	0	1	0	1	0	1	0	1	1	0	0	Grayscale display mode (D=0) or Mono display mode (D=1). (RESET = 00H)
	0	1	0	*	*	*	*	*	*	*	D	
20. Display OFF/ON (AEH-AFH)	0	1	0	1	0	1	0	1	1	1	D	Turns on OLED panel (1) or turns off (0). (RESET = AEH)
21. Set Gray Scale Table(B8H)	0	1	0	1	0	1	1	1	0	0	0	Set Gray Scale Table (RESET = 0,4,8,12,16,20,24,28,32,36,40, 44,48,52,56,60)
				*	*	GS0 [5]	GS0 [4]	GS0 [3]	GS0 [2]	GS0 [1]	GS0 [0]	

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			*	*	GS15 [5]	GS15 [4]	GS15 [3]	GS15 [2]	GS15 [1]	GS15 [0]			
22. Set RESET Linear Gray Scale Table for PWM-driving mode (BAH)	0	1	0	1	0	1	1	1	0	1	0		Set RESET Linear Gray Scale Table for PWM-driving mode
23. Set Common Output Scan Direction (C8H)	0	1	0	1	1	0	0	D	*	*	*		Scan from COM0 to COM [N - 1] (0) or Scan from COM [N - 1] to COM0 (1). (RESET = C0H)
24. Set Display Offset (D3H)	0	1	0	1	1	0	1	0	0	1	1		The next command specifies the mapping of display start line to one of COM0-127. (RESET=00H)
	0	1	0	Display Offset Data Set									
25. Set Display Divide Ratio/Oscillator Frequency Mode Set (D5H)	0	1	0	1	1	0	1	0	1	0	1		This command is used to set the frequency of the internal display clocks. (RESET = 50H)
	0	1	0	Oscillator Frequency				*	Divide Ratio				
26. Set Discharge Period (D8H)	0	1	0	1	1	0	1	1	0	0	0		This command is used to set the duration of the discharge period. (RESET = 02H)
	0	1	0	*	*	*	A4	A3	A2	A1	A0		
27. Set pre-charge Period (D9H)	0	1	0	1	1	0	1	1	0	0	1		This command is used to set the duration of the pre-charge period. (RESET = 04H)
	0	1	0	*	*	*	A4	A3	A2	A1	A0		
28. Set SEG pads hardware configuration (DAH)	0	1	0	1	1	0	1	1	0	1	0		This command is to set the SEG signals pad configuration to match the OLED panel hardware layout. (RESET = 00H)
	0	1	0	*	*	*	*	*	*	*	*	A0	
29. VCOM Deselect Level (DBH)	0	1	0	1	1	0	1	1	0	1	1		This command is to set the common pad output voltage level at deselect stage. (RESET = 35H)
	0	1	0	VCOM = ($\beta_1 \times V_{PP}$)									
30. Pre-charge VSEGH Level control (DCH)	0	1	0	1	1	0	1	1	1	0	0		This command is used to set Pre-charge VSEGH Level . (RESET = 0FH)
	0	1	0	*	*	*	A4	A3	A2	A1	A0		
31. Set discharge VSL Level (DDH)	0	1	0	1	1	0	1	1	1	0	1		This command is used to Set discharge VSL Level. (RESET = 00H)
	0	1	0	*	*	*	A4	A3	A2	A1	A0		
32. Read-Modify-Write (E0H)	0	1	0	1	1	1	0	0	0	0	0		Read-Modify-Write start.
34. End (EEH)	0	1	0	1	1	1	0	1	1	1	0		Read-Modify-Write end.

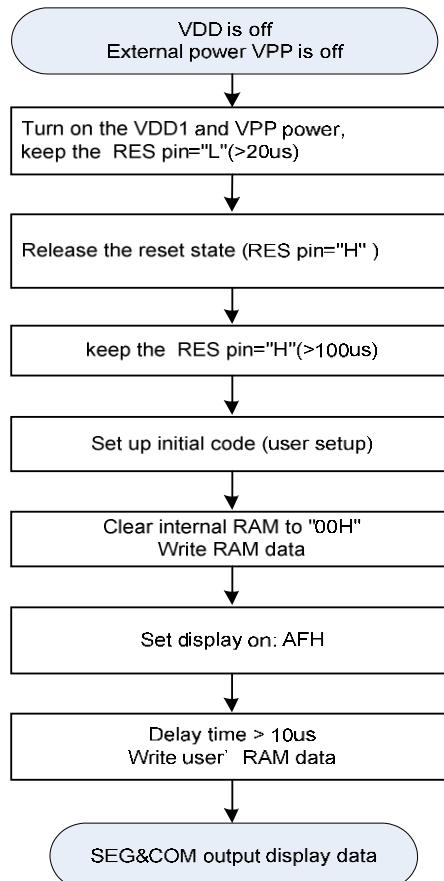
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34. NOP (E3H)	0	1	0	1	1	1	0	0	0	1	1	Non-Operation Command
35. Read Panel ID (E1H)	0	1	0	*	*	*	*	*	*	Read Panel ID[1:0]		This command is to read Panel ID by hardware pin ID0&ID1 setting
36. Read Panel ID (E2H)	0	1	0	BUSY	ON/OFF					IC ID[5:0]		This command is to read IC ID. The output bits 101000 (it means SP5140)
37. Read RAM Key in SPI interface(5AH)	0	1	0	0	1	0	1	1	0	1	0	
38. Read command Key in SPI interface(5BH)	0	1	0	0	1	0	1	1	0	1	1	
39. SPI read data output mode (92H)	0	1	0	1	0	0	1	0	0	1	1	When Serial Interface (SPI) is selected, control data output to pin D1 or D2 in read command or ram A[7:0] = 0x00, SPI data output to pin D2. (RESET) A[7:0] = 0x69, SPI data output to pin D1.
	0	1	0	A7	A6	A5	A4	A3	A2	A1	A0	

Note: Do not use any other command, or the system malfunction may result.

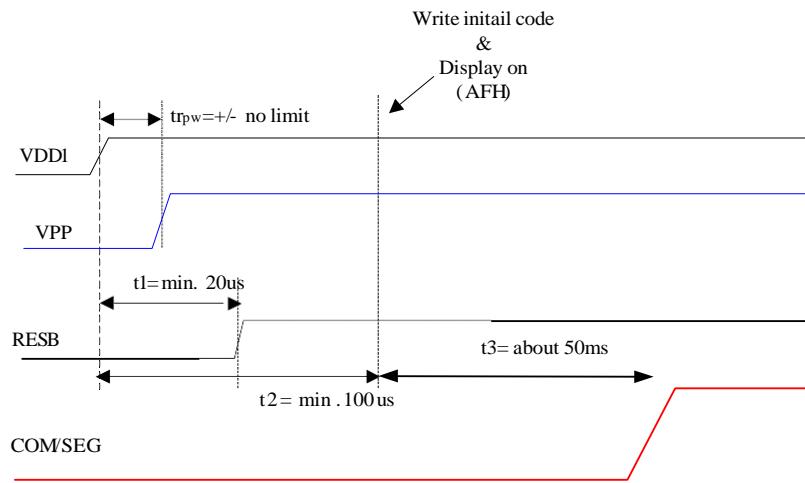
Power On/Off and Initialization

External power is being used immediately after turning on the power:

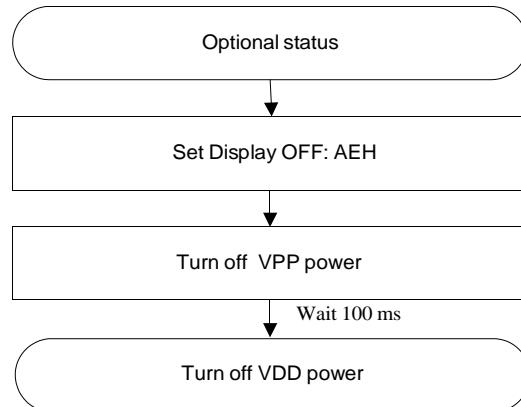


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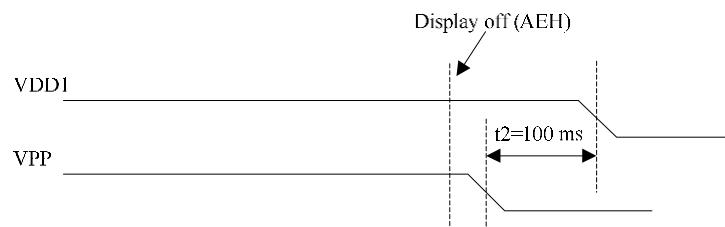
Power on sequence :



Power Off



Power off sequence :



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Absolute Maximum Rating*

DC Supply Voltage (V_{DD})	-0.3V to +3.6V
DC Supply Voltage (V_{PP})	-0.3V to +18.5V
Input Voltage	-0.3V to V_{DD} + 0.3V
Operating Ambient Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics (GND = 0V, VDD = 1.65 – 3.6V, TA =+25°C, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating voltage	1.65	-	3.5	V	
V_{PP}	OLED Operating voltage	8.0	-	18.0	V	
I_{DD}	Dynamic current consumption in V_{DD}	-	-	800	μA	$V_{DD} = 3.0V$, $I_{REF} = -18.75\mu A$, Contrast ≤ 256 , Display ON, display data = All ON
I_{PP}	OLED dynamic current consumption in V_{PP}	-	-	2.5	mA	$V_{DD} = 3.0V$, $V_{PP} = 12V$, $I_{REF} = -18.75\mu A$, Contrast ≤ 256 , Display ON, Display data = All ON, No panel attached
I_{SP}	Sleep mode current Consumption in V_{DD}	-	-	60	μA	During sleep, $TA = +25^{\circ}C$, $V_{DD1} = 3.0V$ 500us after pin reset
	Sleep mode current Consumption in V_{PP}	-	0.01	5	μA	During sleep, $TA = +25^{\circ}C$, $V_{PP} = 12V$
I_{SEG}	Segment output current	540	600	660	μA	$V_{DD} = 3.0V$, $V_{PP} = 12V$, $I_{REF} = -18.75\mu A$, $R_{LOAD} = 10k$,
		371	412.5	453	μA	$V_{DD} = 3.0V$, $V_{PP} = 12V$, $I_{REF} = -18.75\mu A$, $R_{LOAD} = 10k$,
		270	300	330	μA	$V_{DD} = 3.0V$, $V_{PP} = 12V$, $I_{REF} = -18.75\mu A$, $R_{LOAD} = 10k$,
		202	225.5	248	μA	$V_{DD} = 3.0V$, $V_{PP} = 12V$, $I_{REF} = -18.75\mu A$, $R_{LOAD} = 10k$,
		33.75	37.5	41.25	μA	$V_{DD} = 3.0V$, $V_{PP} = 12V$, $I_{REF} = -18.75\mu A$, $R_{LOAD} = 10k$,
ΔI_{SEG1}	Segment output current uniformity	-	-	± 3	%	$\Delta I_{SEG1} = (I_{SEG} - I_{MID}) / I_{MID} \times 100\%$ $I_{MID} = (I_{MAX} + I_{MIN}) / 2$ I_{SEG} [0:255] at contrast ≤ 256
ΔI_{SEG2}	Adjacent segment output current uniformity	-	-	± 2	%	$\Delta I_{SEG2} = (I_{SEG[N]} - I_{SEG[N+1]}) / (I_{SEG[N]} + I_{SEG[N+1]}) \times 100\%$ I_{SEG} [0:255] at contrast ≤ 256

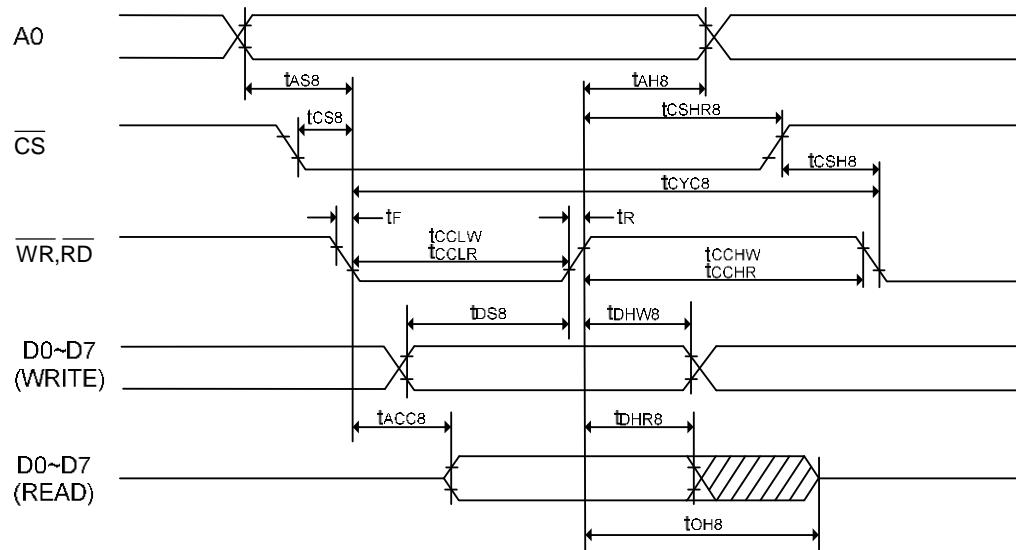
SP5140 internal SPEC

DC Characteristics (Continued)

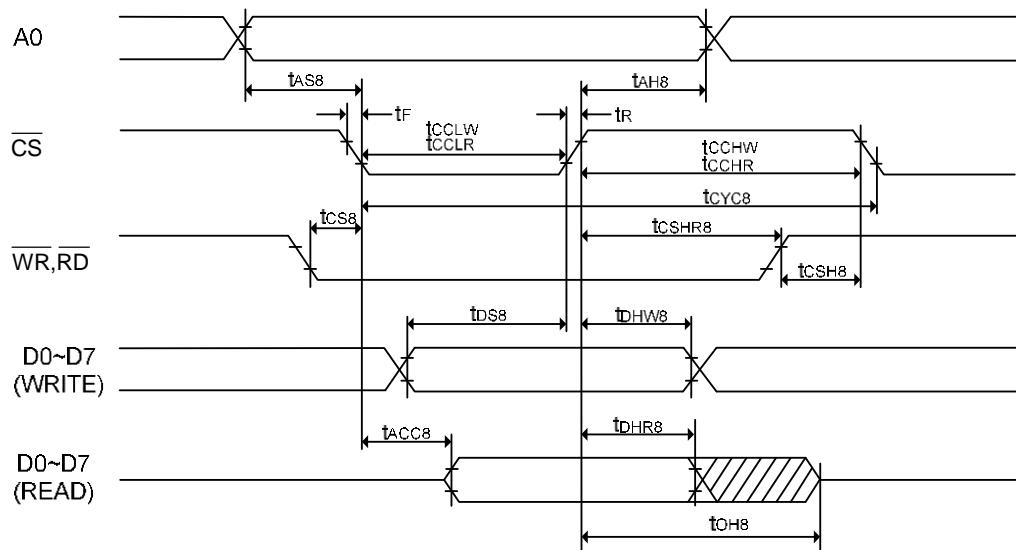
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
V_{IH}	High-level input voltage	$0.8 \times V_{DD}$	-	V_{DD}	V	A0, D0 - D7, \overline{RD} (E), \overline{WR} (R/W), \overline{CS} , CLS, CL, IM0~2 and \overline{RES} .	
V_{IL}	Low-level input voltage	GND	-	$0.2 \times V_{DD}$	V		
V_{OH}	High-level output voltage	$0.8 \times V_{DD}$	-	V_{DD}	V	$I_{OH} = -0.5mA$ (D0 - D7, and CL).	
V_{OL}	Low -level output voltage	GND	-	$0.2 \times V_{DD}$	V	$I_{OL} = 0.5mA$ (D0, D2 - D7, and CL)	
V_{OLCS}	SDA low -level output voltage	GND	-	$0.2 \times V_{DD}$	V	$V_{DD} < 2V$	$I_{OL}=2mA$ (SDA)
				0.4		$V_{DD} > 2V$	$I_{OL}=3mA$ (SDA)
I_{LI}	Input leakage current	-1.0	-	1.0	μA	$V_{IN} = V_{DD}$ or GND (A0, RD(E), WR (R/W), \overline{CS} , CLS, IM0~2 and RES).	
I_{Hz}	Hz leakage current	-1.0	-	1.0	μA	When the D2 - D7, and CL are in high impedance.	
f_{osc}	Oscillation frequency	3.42	3.8	4.18	MHz	$T_A = +25^\circ C$.	
f_{FRM}	Frame frequency for 128 Commons	-	110	-	Hz	When $f_{osc} = 3.8MHz$, Divide ratio =1, display width = 252+18DCLKs.	
R_{ON1}	Common switch resistance	10	15	35	Ω	$V_{pp}=12V, V_{COM}= GND +0.4V$	
R_{ON2}	Common switch resistance	400	500	600	Ω	$V_{pp}=12V, V_{COM}=0.770 \times V_{pp}-0.4V$	

AC Characteristics

(1) System buses Read/Write characteristics 1 (For the 8080 Series Interface MPU)



8080-series parallel interface cycle (Form1)



8080-series parallel interface cycle (Form2)

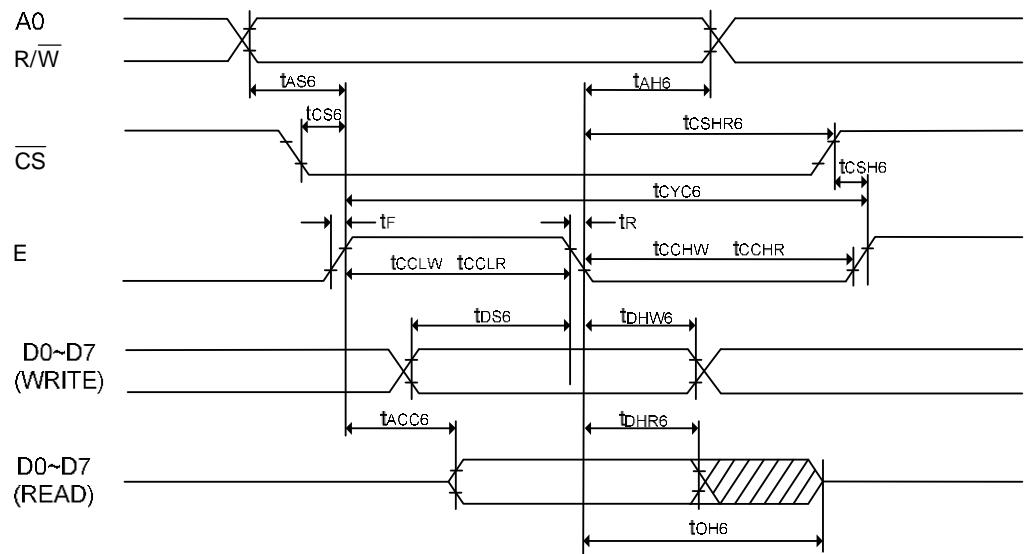
SP5140 internal SPEC

(VDD1 = 1.65 - 3.5V, TA = +25°C)

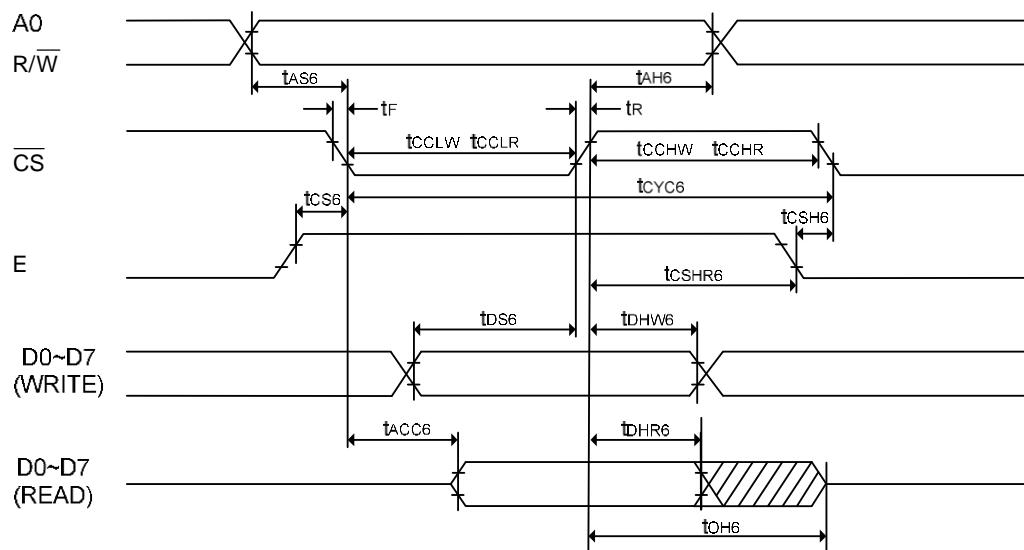
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tCYC8	System cycle time	600	-	-	ns	
tAS8	Address setup time	0	-	-	ns	
tAH8	Address hold time	0	-	-	ns	
tDS8	Data setup time	80	-	-	ns	
tDHW8	Write Data hold time	20	-	-	ns	
tDHR8	Read Data hold time	20	-	-	ns	
ToH8	Output disable time	-	-	140	ns	CL = 100pF
tACC8	\overline{RD} access time	-	-	280	ns	CL = 100pF
tcCLW	Control L pulse width (WR)	300	-	-	ns	
tcCLR	Control L pulse width (RD)	300	-	-	ns	
tcCHW	Control H pulse width (WR)	300	-	-	ns	
tcCHR	Control H pulse width (RD)	300	-	-	ns	
tR	Rise time	-	-	30	ns	
tF	Fall time	-	-	30	ns	
tCS8	Chip select setup time	0	-	-	ns	
tCSH8	Chip select hold time	40	-	-	ns	
tCSHR8	Chip select hold time to read signal	40	-	-	ns	

Note: 8080 interface speed is less than oscillator frequency.

(2) System buses Read/Write Characteristics 2 (For the 6800 Series Interface MPU)



6800-series parallel interface cycle (Form1)



6800-series parallel interface cycle (Form2)

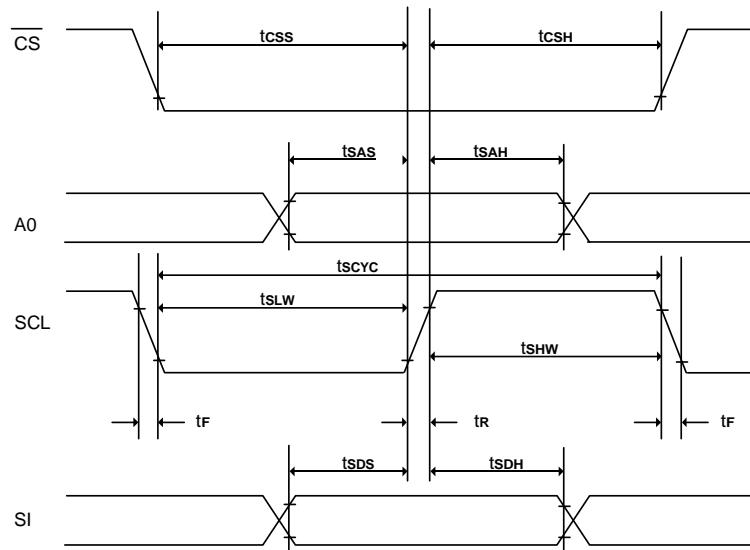
SP5140 internal SPEC

(V_{DD1} = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t _{CYC6}	System cycle time	600	-	-	ns	
t _{AS6}	Address setup time	0	-	-	ns	
t _{AH6}	Address hold time	0	-	-	ns	
t _{DS6}	Data setup time	80	-	-	ns	
t _{DHW6}	Write Data hold time	20	-	-	ns	
t _{DHR6}	Read Data hold time	20	-	-	ns	
t _{OH6}	Output disable time	-	-	140	ns	C _L = 100pF
t _{ACC6}	Access time	-	-	280	ns	C _L = 100pF
t _{EWHW}	Enable H pulse width (Write)	300	-	-	ns	
t _{EWHR}	Enable H pulse width (Read)	300	-	-	ns	
t _{EWLW}	Enable L pulse width (Write)	300	-	-	ns	
t _{EWLR}	Enable L pulse width (Read)	300	-	-	ns	
t _R	Rise time	-	-	30	ns	
t _F	Fall time	-	-	30	ns	
t _{C56}	Chip select setup time	0	-	-	ns	
t _{C5H6}	Chip select hold time	40	-	-	ns	
t _{C5HR6}	Chip select hold time to read signal	40	-	-	ns	

Note: 6800 interface speed is less than oscillator frequency.

(3) System buses Write characteristics 3 (For 4 wire SPI)

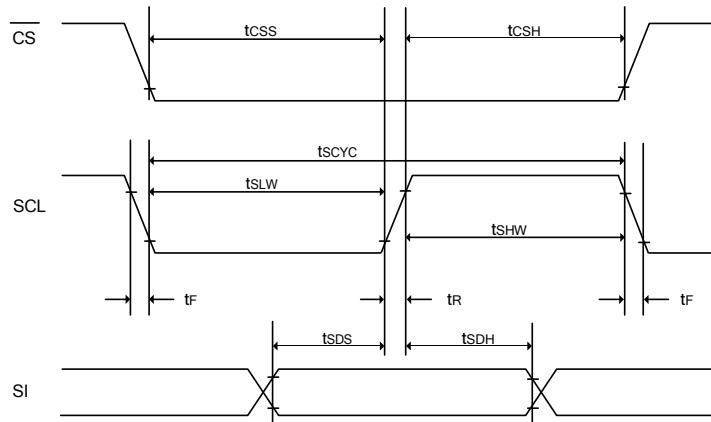


($V_{DD1} = 1.65 - 3.5V$, $TA = +25^{\circ}\text{C}$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tscyc	Serial clock cycle	100	-	-	ns	
tsAS	Address setup time	60	-	-	ns	
tsAH	Address hold time	60	-	-	ns	
tsDS	Data setup time	40	-	-	ns	
tSDH	Data hold time	40	-	-	ns	
tcss	\bar{CS} setup time	90	-	-	ns	
tcsH	\bar{CS} hold time time	24	-	-	ns	
tSHW	Serial clock H pulse width	40	-	-	ns	
tSLW	Serial clock L pulse width	40	-	-	ns	
tR	Rise time	-	-	6	ns	
tF	Fall time	-	-	6	ns	

SP5140 internal SPEC

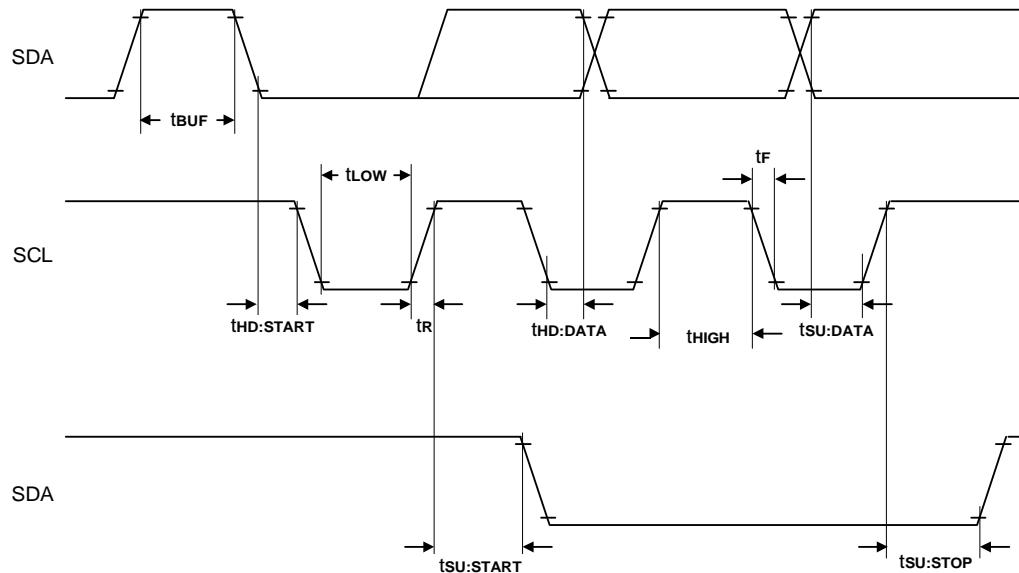
(4) System buses Write characteristics 4(For 3 wire SPI)



($V_{DD1} = 1.65 - 3.5V$, $TA = +25^{\circ}C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tscyc	Serial clock cycle	100	-	-	ns	
tsds	Data setup time	40	-	-	ns	
tsdh	Data hold time	40	-	-	ns	
tcss	CS setup time	90	-	-	ns	
tcsesh	CS hold time time	24	-	-	ns	
tshw	Serial clock H pulse width	40	-	-	ns	
tslw	Serial clock L pulse width	40	-	-	ns	
tr	Rise time	-	-	6	ns	
tf	Fall time	-	-	6	ns	

(5) I²C interface characteristics



(V_{DD1} = 1.65 - 3.5V, TA = +25°C)

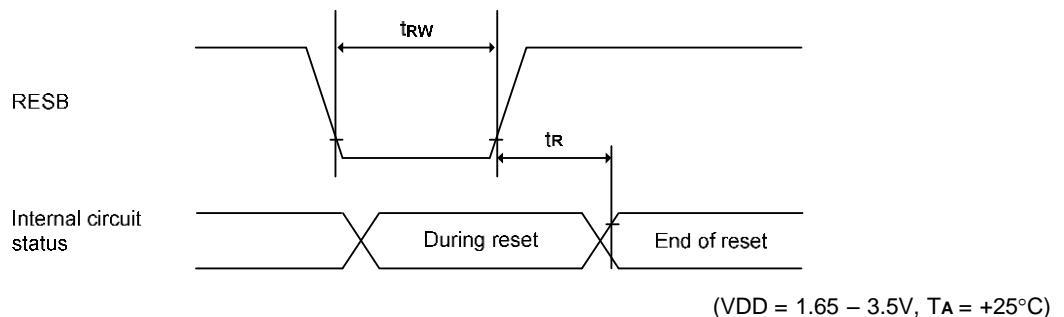
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
f _{SCL}	SCL clock frequency	0	-	400	kHz	
T _{LOW}	SCL clock Low pulse width	1.3	-	-	uS	
T _{HIGH}	SCL clock H pulse width	0.6	-	-	uS	
T _{SU:DATA}	data setup time	100	-	-	nS	
T _{HD:DATA}	data hold time	$\alpha^{(1)}$	-	$\alpha \alpha^{(2)}$	uS	
T _R	SCL · SDA rise time	20	-	300	nS	
T _F	SCL · SDA fall time	20	-	300	nS	
C _b	Capacity load on each bus line	-	-	400	pF	
T _{SU:START}	Setup time for re-START	0.6	-	-	uS	
T _{HD:START}	START Hold time	0.6	-	-	uS	
T _{SU:STOP}	Setup time for STOP	0.6	-	-	uS	
T _{BUF}	Bus free times between STOP and START condition	1.3	-	-	uS	

Notes

1. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
2. The maximum thd;DAT has only to be met if the device does not stretch the LOW period (tLOW) of the SCL signal.

SP5140 internal SPEC

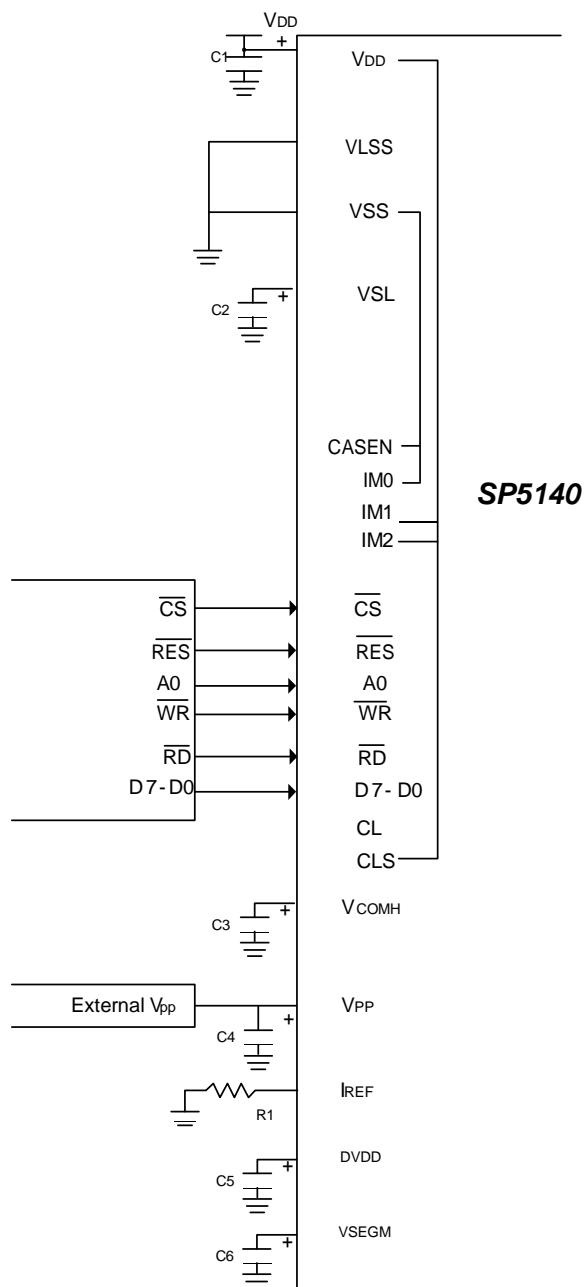
(6) Reset Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset time	-	-	100	us	
t_{RW}	Reset low pulse width	20.0	-	-	us	

Application Circuit (for reference only)

1. 8080 series interface:

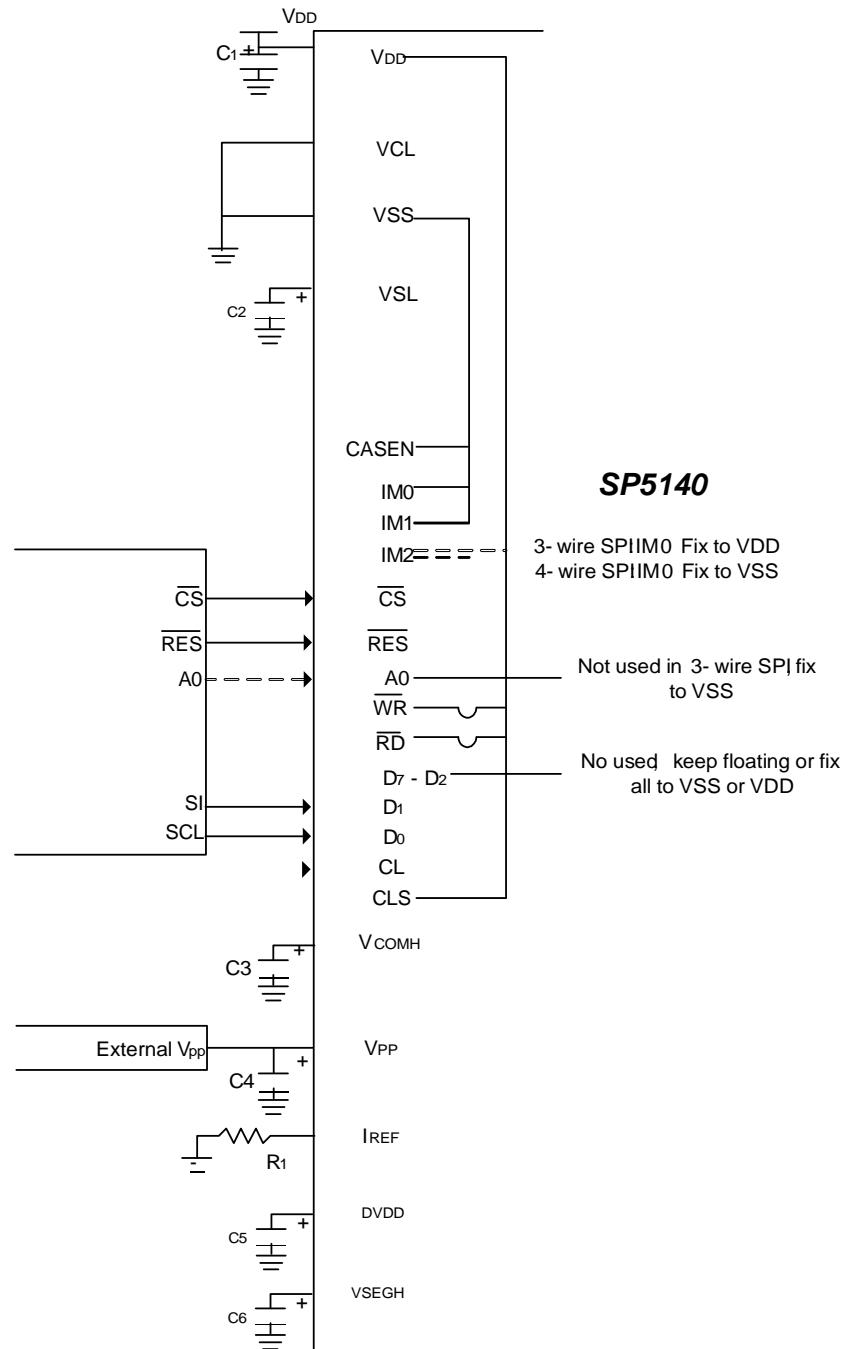


Note:

C1---C6: 4.7 μ F

R_1 : about 750K, $R_1 = (\text{Voltage at } I_{REF} - \text{GND}) / I_{REF}$, Voltage at $I_{REF} \approx V_{PP} - 2V$

2. Serial Interface (3-wire or 4-wire SPI):

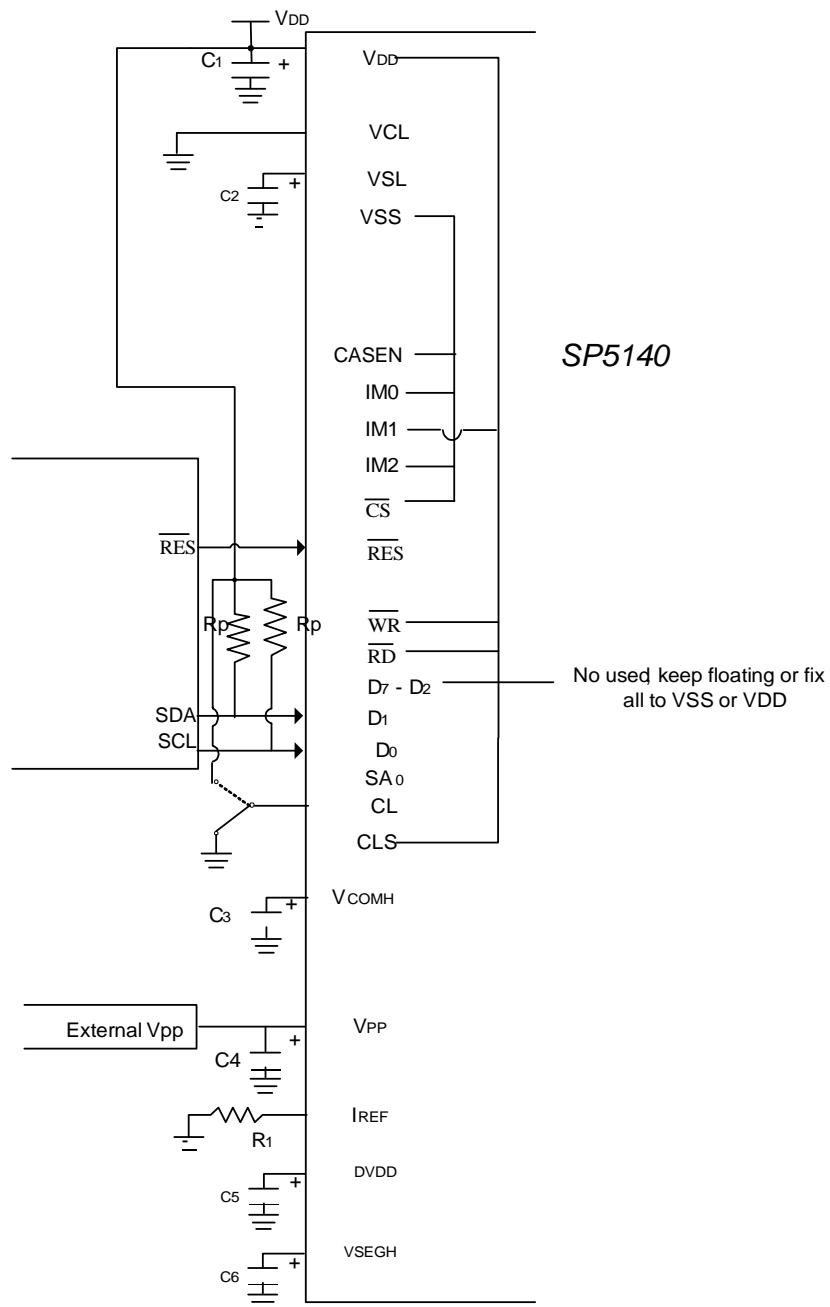


Note:

C1--C5: $4.7\mu F$

R1: about 750K, $R1 = (\text{Voltage at } I_{REF} - \text{GND}) / I_{REF}$, Voltage at $I_{REF} \approx V_{PP} - 2V$

3. I²C Interface



Note:

C1---C5: 4.7μF

R1: about 750K , R1 = (Voltage at I_{REF} - GND) / I_{REF}, Voltage at I_{REF} ≈ V_{PP} - 2V

The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(GND) or 1(VDD). WR and RD are not used in I²C mode, should fix to V_{SS} or V_{DD}.

CS can fix to V_{SS} in I²C mode.

The positive supply of pull-up resistor must equal to the value of VDD

Recommend the value of resistor Rp equal to 1.5KΩ

SP5140 internal SPEC

Ordering Information

Part No.	Package
SP5140	Gold bump on chip tray

SPEC Revision History

Version	Content	Date
0.0	Original	Dec.2018
0.1	1. Modify Set Discharge Period (D8H) 2. Modify tRw, tr 3. Add Note: 8080/6800 interface speed is less than oscillator frequency. 4. Modify Power on sequence 5. Modify Power down sequence 6. Modify Fosc and Ffrm 7. Modify 1 column/row scroll 8. Add note 2, 2Fh+delay+2Eh. 9. Add note, mono mode read and write. 10. Add dimming note. 11. Modify Toh start position. 12.Modify Figure 12 discription. 13.Add read RAM note. 14. Delete memory of CMD lock description. 15. Add dimming note 16. Add scroll valid command sequence 5 17. Add 1 column/row scroll note. 18. Modify Pad Location 19. Modify Alignment Mark Location 20. Modify Pad Description	Mar.2019
0.2	1. Modify Available in COG form, thickness: 250 um 2. Modify System buses Write characteristics 3 3. Delete IIC's Reading RAM function. 4. Modify IPP 1.5mA to 2.5mA 5. D0,D1 are not belong to Hz pad 6. When CLS = "L", CL pad is input and not used.	July.2019
0.3	1. Delete Command Protection function.	Nov.2019