Exercise for Final Exam

1. True/False

(1) Principle of locality is exploited to present the user with as much memory as is available in the cheapest technology at the speed offered by the fastest technology.(T)

(2) In the same size cache, miss rate goes up invariably while block size is increasing.

(3) Compared with direct mapped cache, fully associative cache can reduce the conflict miss and access time.

(4) If a cache has M blocks and N sets, an O-way set associative cache would be the same as a fully-associative cache.

(5) For a fixed size cache, each increase by a factor of two in associativity increases the tag size by 1 bit.

(6) Increasing associativity always benefits for better cache performance as it reduces the miss rate.

(7) Primary cache should focus on minimizing hit time in support of a shorter clock. As a result, L1 cache usually use direct mapped or low associative cache. (T)

2. Multiple Choice

(1) CISC computers:

(A) whose ISAs are difficult to design because they have complex instructions.

(B) whose CPUs are difficult to design because they have complex ALU.

(C) All of the above.

(D) None of the above.

(2) In unsigned binary representation, an overflow is indicated when two numbers are added and

(A) there is a carry out of the most-significant bit (MSB).

(B) there is a carry into the MSB.

(C) the carry into the MSB equals the carry out of the MSB.

(D) the carry into the MSB differs from the carry out of the MSB.

(3) Which of the following is *not* an advantage of the virtual memory used by operating system:

(A) increases the apparent amount of memory available to programs.

(B) provides memory protection between the operating system and programs.

(C) provides memory protection between programs.

(D) reduces the average memory access time.

(4) The data hazard in pipeline may be caused by executing _____ instructions.
(A) add (B) slt (C) lw (D) beq

(5) Suppose a program runs in 90 seconds with 80-second multiplying responsibility. Use Amdahl's Law to make it run 3 times faster by improve the multiplication speed if possible or indicate if it is impossible.
(A) possible, the multiplication needs an improvement factor 3.
(B) possible, the multiplication needs an improvement factor 4.
(C) possible, the multiplication needs an improvement factor 5.
(D) impossible.

3. Given a series of 16 memory address references given as word addresses:
1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6, 9, 17.
(a) Assume a direct-mapped cache with 16 one-word blocks that is initially empty, label each reference as a hit or miss and show the final content of cache, then find the hit rate.

(b) Repeat the question in (a) with a direct-mapped cache with four-word blocks and a total of 16 words that is initially empty.

4. Given a 32-bit address.
(a) How many total bits are needed for a direct-mapped cache with 64 Kbytes of data and one-word blocks.
(b) Repeat the question with a 4-way set associative cache(same block size and the number of blocks) to store the same amount of data.
(c) Repeat the question with a direct-mapped cache and eight-word blocks to store the same amount of data.

5. Suppose a CPU executes at Clock Rate = 200 MHz(5 ns per cycle) with a single level of cache.
Given: $CPI_{execution} = 1.1$, instruction mix: 50% arithmetic/logic, 30% load/store and 20% control. Assume a cache miss rate is 1.5% and miss penalty M = 50 cycles.

Find the CPI with stalls occurred.

6. Suppose a CPU uses separate level one (L1) caches for instructions and data with different miss rates for each of them.
Given: A cache hit incurs no stall cycles while a cache miss incurs 200 stall cycles for both memory reads and writes, $CPI_{execution} = 1.1$, and instruction mix: 50%

arithmetic/logic, 30% load/store and 20% control. Assume a cache miss rate is 0.5% for instruction fetch and a cache data miss rate is 6%.

Find the resulting stalls per access, AMAT and CPI using this cache.

7. Spot all data dependencies (including ones that do not lead to stalls). Draw arrows from the stages where data is made available, directed to where it is needed. Circle the involved registers in the instructions. (5-stage pipeline)
(1) Assume no forwarding.
(2) Forwarding provided.
(3) How many stalls will be added to the pipeline to resolve the hazards in (1).
(4) Repeat the question in (3) to resolve the hazards in (2).

```
addi $t0 $t1 100
lw $t2 4($t0)
add $t3 $t1 $t2
sw $t3 8($t0)
lw $t5 0($t6)
or $t5 $t0 $t3
```

8. Translate C code shown below to MIPS assembly code. Assume that the value i, A, B and S are in registers $t0, $s0, $s1, and $s3, respectively. Also, assume that register $s4 holds the base address of the array D. Note that each element of array D has 4-byte length.

```
S = 0; A = 0; i = 0;
while(i < 8){
        S += D[i];
        if(D[i] > 0) A+=D[i];
        i++;
}
```

9. Translate C code shown below to MIPS assembly code. Assume that the value a, b, i, and j are in registers $s0, $s1, $t0, $t1, respectively, and the base address of array D is in register $s2. Note that each element of array D has 4-byte length.

(1) for(i = 0; i < a; i++)
        a += b;
(2) for(i = 0; i < a; i++)
        for(j = 0; j < b; j++)
            D[4*j] = i + j;

10. Assume that there are two levels of cache.
L1 hit time = 1 cycle, L1 miss rate = 10%
L2 hit time = 3 cycles, L2 miss rate = *x*%, miss penalty = 100 cycles

Require that the AMAT $\leqslant$ 2 cycles, find the maximum value of *x*.

11. Suppose a processor
(1) has separate L1 instruction and data cache. CPI_{base} = 2 cycles, whereas memory accesses take 100 cycles. Instruction miss rate is 3% while data miss rate is 10%. 40% of instructions are loads or stores. Find the CPI.
(2) has added a L2 cache between L1 and memory. L2 cache has a hit time of 10 cycles and a global miss rate of 2%. Find the CPI.