Multicore Computers

Strathmore UNIVERSITY

Alternative Chip Organization

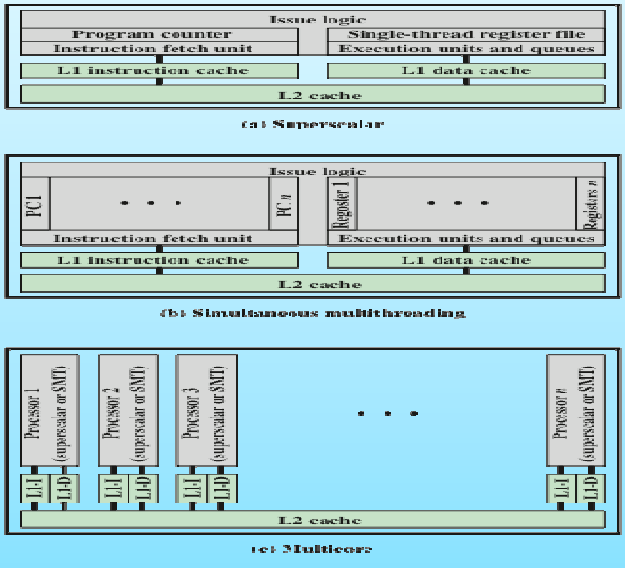
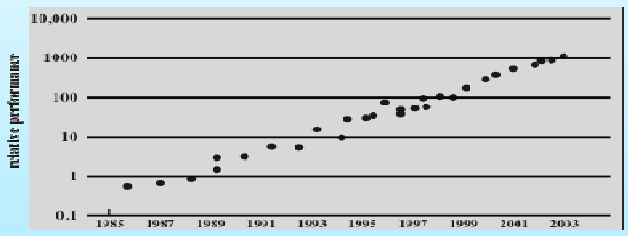


Figure 18.1 Alternative Chip Organizations

Intel Hardware Trends



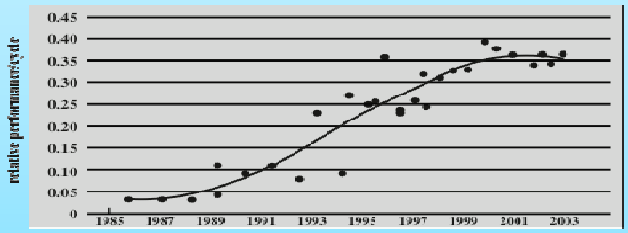


Figure 18.2 Some Intel Hardware Trends

Processor Trends

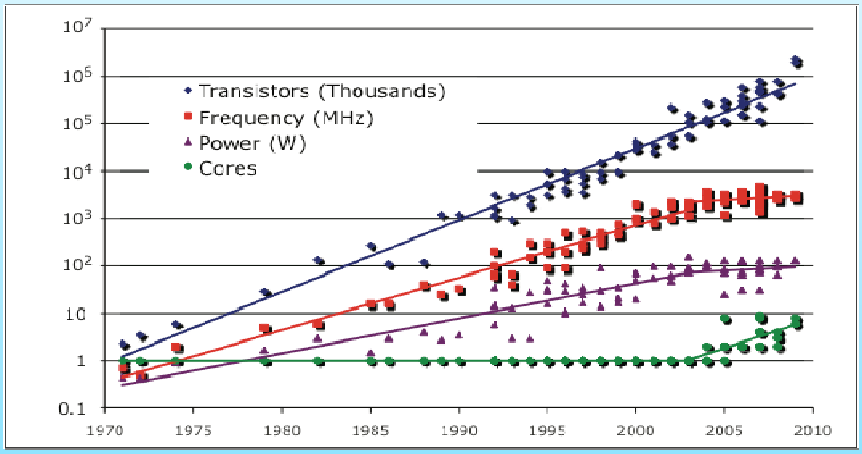


Figure 18.3 Processor Trends

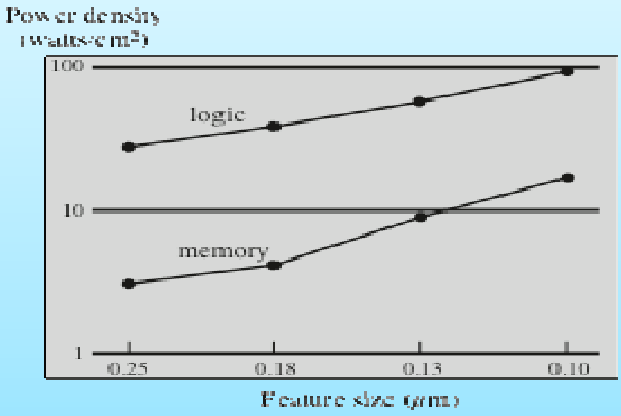


Figure 18.4 Power and Memory Considerations

Power Consumption

- By 2015 we can expect to see microprocessor chips with about 100 billion transistors on a 300 mm² die
- Assuming that about 50-60% of the chip area is devoted to memory, the chip will support cache memory of about 100 MB and leave over 1 billion transistors available for logic
- How to use all those logic transistors is a key design issue
- Pollack's Rule
  - States that performance increase is roughly proportional to square root of increase in complexity

Performance Effect of Multiple Cores

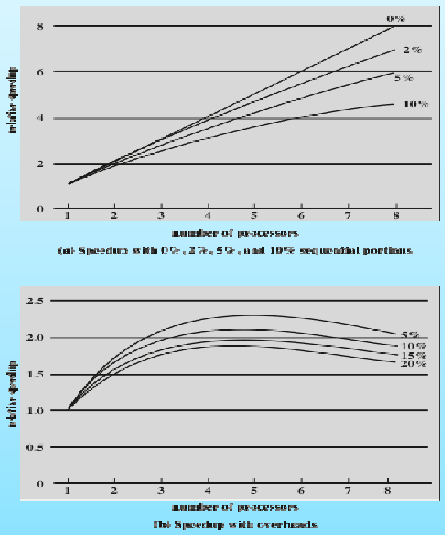


Figure 18.5 Performance Effect of Multiple Cores

Scaling of Database Workloads on Multiple-Processor Hardware

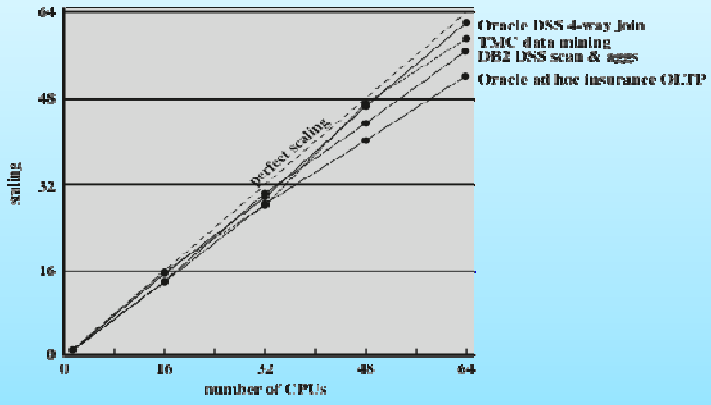


Figure 18.6 Scaling of Database Workloads on Multiple-Processor Hardware

Effective Applications for Multicore Processors

- **Multi-threaded native applications**
  - Characterized by having a small number of highly threaded processes
  - Lotus Domino, Siebel CRM (Customer Relationship Manager)
- **Multi-process applications**
  - Characterized by the presence of many single-threaded processes
  - Oracle, SAP, PeopleSoft
- **Java applications**
  - Java Virtual Machine is a multi-threaded process that provides scheduling and memory management for Java applications
  - Sun's Java Application Server, BEA's Weblogic, IBM Websphere, Tomcat
- **Multi-instance applications**
  - One application running multiple times
  - If multiple application instances require some degree of isolation, virtualization technology can be used to provide each of them with its own separate and secure environment

Hybrid Threading for Rendering Module

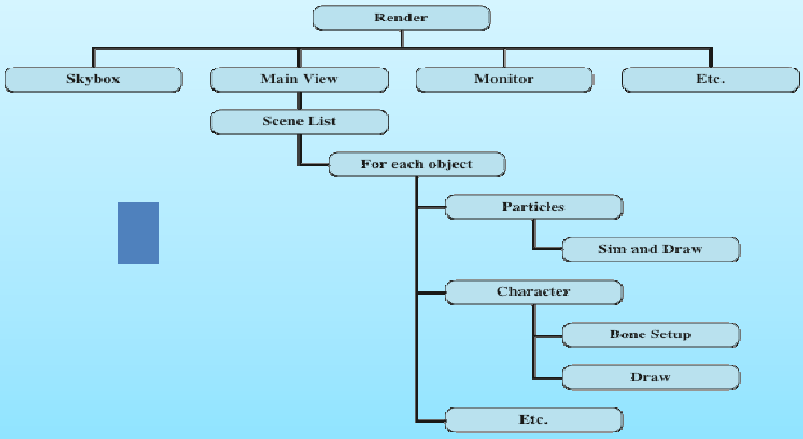


Figure 18.7 Hybrid Threading for Rendering Module

Multicore Organization Alternatives

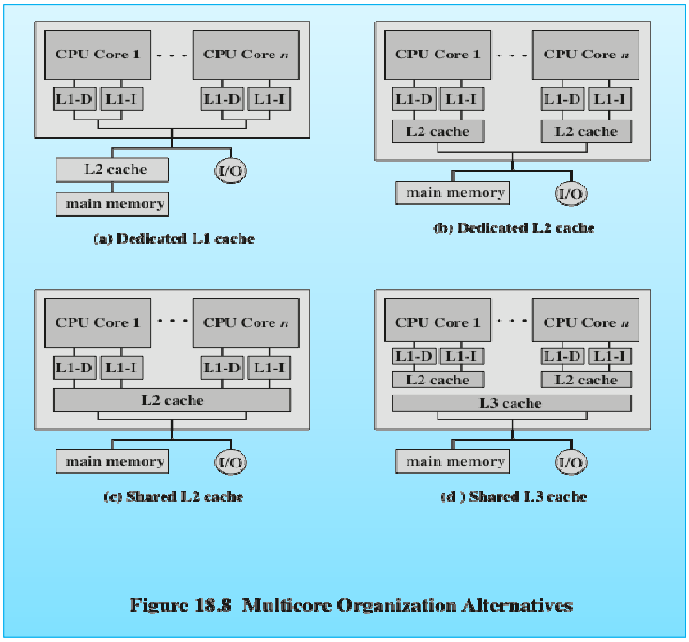


Figure 18.8 Multicore Organization Alternatives

Intel Core Duo Block Diagram

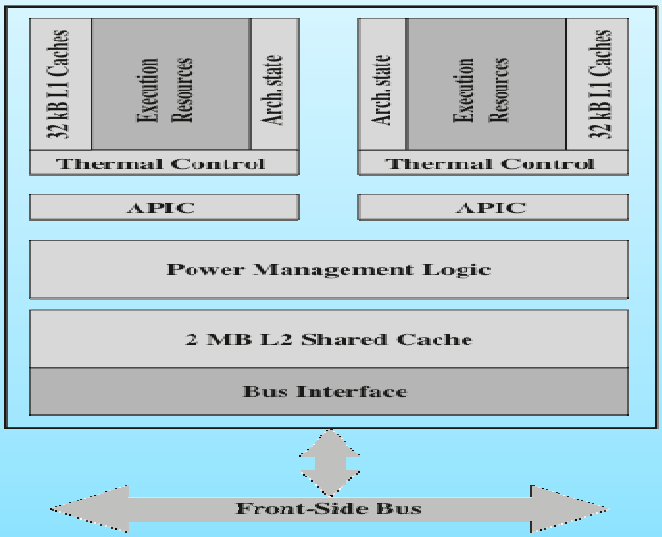


Figure 18.9 Intel Core Duo Block Diagram

Intel x86 Multicore Organization Core Duo

- **Advanced Programmable Interrupt Controller (APIC)**
  - Provides inter-processor interrupts which allow any process to interrupt any other processor or set of processors
  - Accepts I/O interrupts and routes these to the appropriate core
  - Includes a timer which can be set by the OS to generate an interrupt to the local core
- **Power management logic**
  - Responsible for reducing power consumption when possible, thus increasing battery life for mobile platforms
  - Monitors thermal conditions and CPU activity and adjusts voltage levels and power consumption appropriately
  - Includes an advanced power-gating capability that allows for an ultra fine grained logic control that turns on individual processor logic subsystems only if and when they are needed

Intel x86 Multicore Organization Core Duo

- **2MB shared L2 cache**
  - Cache logic allows for a dynamic allocation of cache space based on current core needs
  - MESI support for L1 caches
  - Extended to support multiple Core Duo in SMP
  - L2 cache controller allows the system to distinguish between a situation in which data are shared by the two local cores, and a situation in which the data are shared by one or more caches on the die as well as by an agent on the external bus
- **Bus interface**
  - Connects to the external bus, known as the Front Side Bus, which connects to main memory, I/O controllers, and other processor chips

Intel Core i7-990X Block Diagram

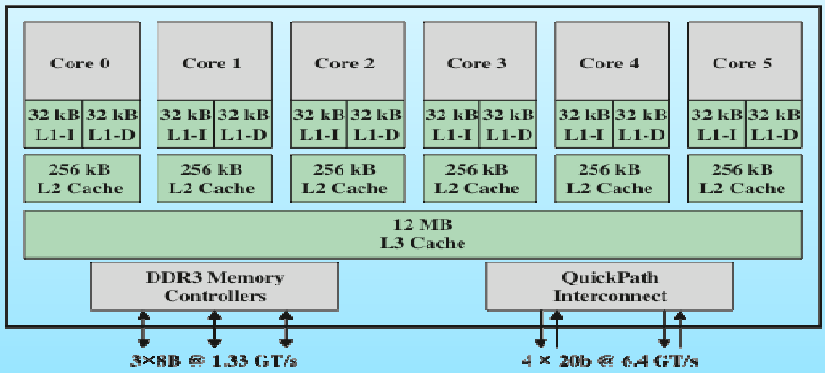


Figure 18.10 Intel Core i7-990X Block Diagram

Table 18.1: Cache Latency

CPU	Clock Frequency	L1 Cache	L2 Cache	L3 Cache
Core 2 Quad	2.66 GHz	3 cycles	15 cycles	—
Core i7	2.66 GHz	4 cycles	11 cycles	39 cycles

Table 18.1 Cache Latency (in clock cycles)

Table 18.2: ARM11 MPCore Configurable Options

Feature	Range of options	Default value
Processors	1 to 4	4
Instruction cache size per processor	16 KB, 32 KB, or 64 KB	32 KB
Data cache size per processor	16 KB, 32 KB, or 64 KB	32 KB
Master ports	1 or 2	2
Width of interrupt bus	0 to 224 by increments of 32 pins	32 pins
Vector floating point (VFP) coprocessor per processor	Included or not	Included

Table 18.2 ARM11 MPCore Configurable Options

ARM11 MP Core Processor Block Diagram

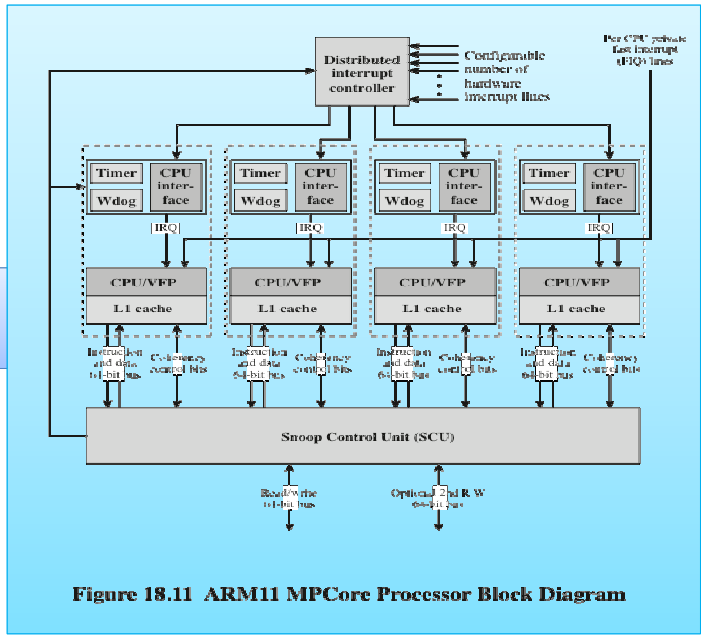


Figure 18.11 ARM11 MPCore Processor Block Diagram

Interrupt Handling

- Distributed Interrupt Controller (DIC) collates interrupts from a large number of sources
- It provides:
  - Masking of interrupts
  - Prioritization of the interrupts
  - Distribution of the interrupts to the target MP11 CPUs
  - Tracking status of interrupts
  - Generation of interrupts by software
- Is a single function unit that is placed in the system alongside MP11 CPUs
- Memory mapped
- Accessed by CPUs via private interface through SCU
- Provides a means of routing an interrupt request to a single CPU or multiple CPUs, as required
- Provide a means of interprocessor communication so that a thread on one CPU can cause activity by a thread on another CPU

DIC Routing

- The DIC can route an interrupt to one or more CPUs in the following three ways:
  - An interrupt can be directed to a specific processor only
  - An interrupt can be directed to a defined group of processors
  - An interrupt can be directed to all processors
- OS can generate interrupt to:
  - All but self
  - Self
  - Other specific CPU
- Typically combined with shared memory for inter-process communication
- 16 interrupt IDs available for inter-processor communication

Interrupt States

From the point of view of an MP11 CPU, an interrupt can be:

Inactive
- Is one that is nonasserted, or which in a multi- processing environment has been completely processed by that CPU but can still be either Pending or Active in some of the CPUs to which it is targeted, and so might not have been cleared at the interrupt source

Pending
- Is one that has been asserted, and for which processing has not started on that CPU

Active
- Is one that has been started on that CPU, but processing is not complete
- An Active interrupt can be pre-empted when a new interrupt of higher priority interrupts MP11 CPU interrupt processing

Interrupt Sources

- Inter-process Interrupts (IPI)
  - Private to CPU
  - ID0-ID15
  - Software triggered
  - Priority depends on target CPU not source
- Private timer and/or watchdog interrupt
  - ID29 and ID30
- Legacy FIQ line
  - Legacy FIQ pin, per CPU, bypasses interrupt distributor
  - Directly drives interrupts to CPU
- Hardware
  - Triggered by programmable events on associated interrupt lines
  - Up to 224 lines
  - Start at ID32

ARM11 MPCore Interrupt Distributor

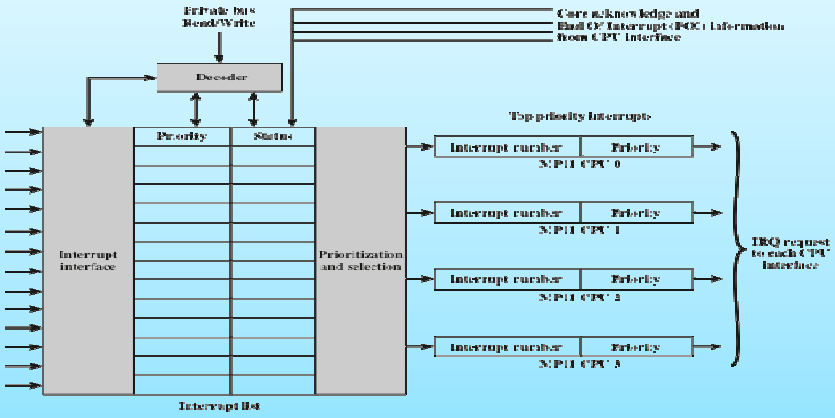


Figure 18.12 Interrupt Distributor Block Diagram

Cache Coherency

- Snoop Control Unit (SCU) resolves most shared data bottleneck issues
- L1 cache coherency scheme is based on the MESI protocol
- Direct Data Intervention (DDI)
  - Enables copying clean data between L1 caches without accessing external memory
  - Reduces read after write from L1 to L2
  - Can resolve local L1 miss from remote L1 rather than L2
- Duplicated tag RAMs
  - Cache tags implemented as separate block of RAM
  - Same length as number of lines in cache
  - Duplicates used by SCU to check data availability before sending coherency commands
  - Only send to CPUs that must update coherent data cache
- Migratory lines
  - Allows moving dirty data between CPUs without writing to L2 and reading back from external memory

IBM z196 Processor Node Structure

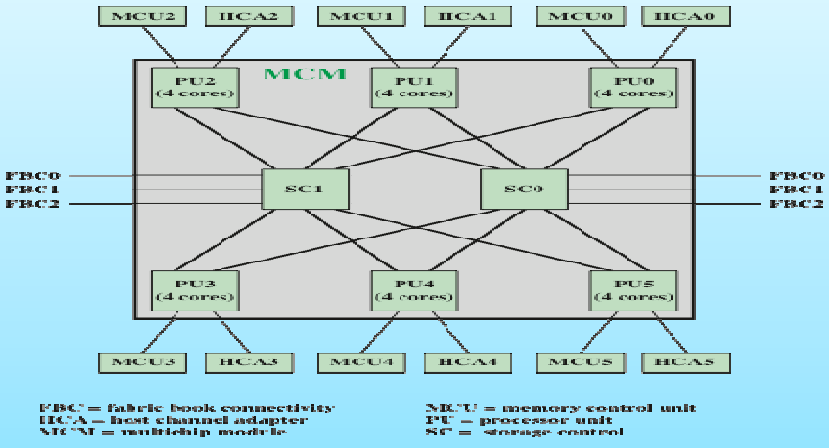


Figure 18.13 IBM z196 Processor Node Structure

IBM z196 Cache Hierarchy

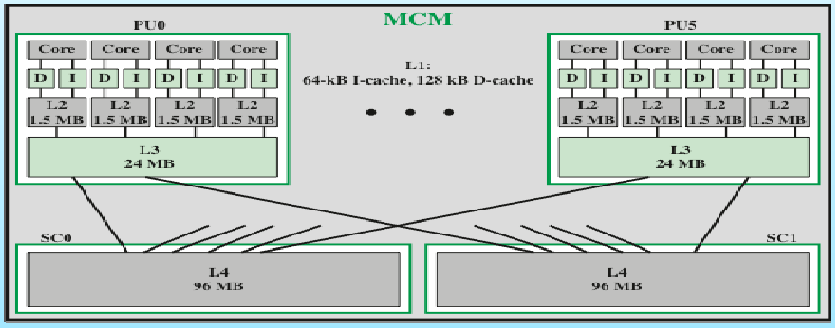


Figure 18.14 IBM z196 Cache Hierarchy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