**Module Descriptions**

✓***~~Register File:~~***

***Ports:***

***Inputs:***

* ~~Write Select~~
* ~~Write enable~~
* ~~3 read selects~~
* ~~Write Data~~
* ~~Clock~~

***Outputs:***

* ~~3 registers~~

***Details:***

32 registers, 64-bits each

There can be 3 reads *(2or3 64-bit registers can be read)* and 1 *write (1 64-bit value can be written when write enable is asserted)* each cycle.

*Data forwarding* must be used so that a write and read to the same register returns the new value for the read.

***Program Counter (Instruction Select)***

***Inputs:***

* Clock

***Output:***

* Instruction Address

***Decoder***

***Inputs:***

* 24-bit Instruction
* Clock

***Outputs***

* Depends (TBD)

***Instruction Memory***

***Ports:***

***Inputs:***

* Instruction Select (PC)
* Clock

***Outputs:***

* 24-bit Instruction

***ALU***

***Ports:***

***Inputs:***

* 3 (64-bit) Reg. Inputs
* Opcode (Size: TBD)
* Clock

***Outputs:***

* Data (Calculation) output