

Voltage Surge Estimation in Inverter-Cable High-Impedance Load System

Benjamin Egyin Wilson¹, Ebenezer Armah², Nutifafa Tsikata^{3*}

¹Department of Electrical Engineering, University of Energy and Natural Resources, Sunyani, Ghana

²Department of Electronics Engineering, Norfolk State University, Norfolk, Virginia, United States

³Department of Electrical Engineering, University of Mines and Technology, Tarkwa, Western Region, Ghana

*Correspondence: nutifafat@yahoo.com

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Abstract: This paper presents a theoretical analysis of inverter–cable–high-impedance load systems using transmission line theory. High-frequency inverters with short voltage rise times can induce severe voltage surges at the load terminal due to impedance mismatch and wave reflections. An analytical expression is derived to estimate the peak terminal voltage as a function of the inverter rise time and cable propagation delay. Simulation results obtained using MATLAB confirm that the peak voltage can surge up to twice the DC link value (300 V for a 150 V DC source) when the inverter rise time is less than three times the cable propagation delay. To mitigate this overvoltage, a dV/dt filter is designed for worst-case rise-time conditions (step input), enhancing surge suppression without requiring redesign across varying switching speeds. The proposed method offers a practical, cost-effective solution for long-cable applications in high-frequency inverter systems.

Keywords: load systems, voltage surge, transmission line theory

1. Introduction

The rapid advancements in power electronic switching devices have significantly improved the performance and efficiency of inverter-fed systems, particularly in applications such as pulse-width modulation (PWM) inverter-fed induction motor drives [1], [2]. Modern inverters, incorporating insulated gate bipolar transistor (IGBT) technology, enable high-frequency switching operations with rise times as low as 0.1 microseconds (μ s). However, while high switching frequencies improve power conversion efficiency and waveform quality, they also introduce unwanted problems, such as excessive voltage stress on connected loads. This problem is commonly severe when long cables connect the inverter to the load, as the combination of high switching frequencies and the distributed nature of cable parameters results in overvoltage generation at the load terminal [3], [4], [5].

Inverter-cable-high impedance load systems experience voltage reflections due to impedance mismatches between the inverter, cable, and load. These reflections contribute to voltage overshoot at the load terminal, sometimes reaching twice the DC link voltage. This phenomenon, worsened by high rate of change of voltage (dV/dt) values, can accelerate insulation degradation in loads such as induction motors and other high-impedance devices. The problem is more common in systems where the load is

located at a significant distance from the inverter, necessitating the use of long interconnecting cables [6]. The voltage waveforms in these cables behave similarly to traveling waves on transmission lines, where multiple voltage reflections can cause ringing effects and excessive overvoltage at the load terminal, leading to insulation failure, overheating, and reduced operational lifespan of the system components [7].

The rise time of the inverter pulse plays a crucial role in determining the magnitude of the overvoltage at the load terminal. Propagation delay in the cable influences the effectiveness of the inverter pulse, and when the rise time of the inverter is shorter than three times the cable propagation delay, voltage overshoot occurs at the load [8], [9]. This means that the voltage at the load terminal can exceed acceptable operational limits, leading to insulation stress and, in extreme cases, equipment failure. To reduce these effects, researchers have explored the relationship between inverter rise time and cable characteristics to establish optimal inverter switching parameters [10], [11]. By ensuring that the inverter rise time is sufficiently long relative to the cable propagation delay, it is possible to reduce transient overvoltage effects at the load. However, while modifying inverter switching parameters is an effective approach, it is not always feasible in applications that require high-frequency operation. Various voltage suppression techniques have also been developed to minimize overvoltage effects in inverter-cable-high impedance load systems.

Different methods have been proposed to suppress overvoltage in long-cable inverter-fed systems. Among the most effective solutions is the installation of an impedance-matching filter at the load terminal [12], [13], [14]. This technique involves terminating the cable with components that match its characteristic impedance, thereby reducing voltage reflections. The three primary types of terminating filters include parallel resistor termination, a first-order filter consisting of a series capacitor-resistor network, and a second-order filter made up of a resistor, capacitor, and inductor. The parallel resistor termination method places a resistor in parallel with the load to absorb reflected voltage waves. However, the major drawback of this approach is the high active power loss associated with the resistor, which can significantly reduce system efficiency. A more refined approach involves using a capacitor-resistor (C-R) network, which helps attenuate high-frequency voltage spikes while minimizing energy loss. The most effective of the terminating filters is the resistor-capacitor-inductor (R-C-L) network, which provides improved attenuation of transient overvoltage by damping high-frequency oscillations [15]. However, designing such filters requires precise tuning to match the cable's impedance characteristics [16].

While these terminating filter techniques can be highly effective in reducing overvoltage stress at the load, they also present practical implementation challenges [17]. For instance, submarine motors and deep-well submersible pumps require long cables, making it extremely difficult to install and maintain terminating filters due to a lack of accessibility [18]. In such cases, alternative suppression techniques must be considered. Given the limitations of traditional impedance-matching filters, researchers have proposed various inverter output filter designs to mitigate overvoltage effects. One notable method is the cascaded inverter output filter, which consists of multiple dV/dt filters installed at the inverter output. This technique enhances overvoltage suppression by providing double attenuation compared to a single dV/dt filter [19]. Studies have shown that using cascaded filters effectively reduces overvoltage at the cable-end terminal by increasing the rise time of the switching pulses. However, the major drawback of this technique is the high cost associated with implementing multiple filter stages [20].

A more cost-effective and efficient approach to overvoltage suppression is the use of a single dV/dt filter, optimized for worst-case scenarios. The proposed dV/dt filter in this study is designed based on a step voltage source with a rise time of 0 seconds, representing the most extreme transient condition. By designing the filter for this worst-case scenario, it ensures that the same dV/dt filter can be applied across different inverter rise times without the need for constant redesign and replacement. The proposed dV/dt filter presents several advantages over traditional suppression methods. Since it is designed for the worst-case step voltage condition, the filter can be applied across a wide range of inverter rise times without modification. Unlike cascaded filters, which require multiple filter stages, a single optimized dV/dt filter reduces implementation costs while achieving similar levels of overvoltage suppression. Unlike terminating resistors, which dissipate significant active power, the dV/dt filter minimizes power losses while effectively controlling transient voltage spikes. Additionally, unlike terminating filters that require installation at the load terminal, the dV/dt filter can be placed at the inverter output, making it more accessible and easier to maintain [21].

The increasing use of high-frequency switching in inverter-fed systems has led to significant challenges related to overvoltage generation, particularly when long cables are used to connect inverters to high-impedance loads. Excessive overvoltage at the load terminal can cause severe insulation degradation, reduced system lifespan, and increased electromagnetic interference. Traditional mitigation techniques, such as terminating filters, provide effective voltage suppression but suffer from high power losses, accessibility challenges, and cost constraints [22]. A significant research gap exists in the mitigation of overvoltage effects in inverter-fed cable systems, particularly in high-frequency switching environments. While various methods have been proposed, including dV/dt filters and impedance-matching termination techniques, existing solutions often present critical limitations such as increased power losses, high implementation costs, and practical constraints in specialized applications like deep-sea or underground systems.

Several studies have investigated the overvoltage effects in inverter-fed cable systems and proposed different mitigation techniques. Research by [23] explored the impact of high-frequency switching on long cable systems and demonstrated how transmission line effects contribute to voltage overshoot at the load terminals. Their findings emphasized the need for dV/dt filters in reducing voltage stress on motor windings, but the study primarily focused on short cable lengths, leaving a gap in the analysis of long-distance transmission effects. A study by [24] analyzed the performance of impedance-matching termination networks for inverter-fed cables. Their work highlighted that while passive termination can effectively suppress overvoltage, the associated power losses in the terminating resistor pose efficiency challenges. They suggested an optimized design approach but did not address the adaptability of the method for varying inverter rise times, which is crucial in practical applications where switching characteristics may change.

In [25], the authors introduced a cascaded dV/dt filter for overvoltage suppression, which employed a dual-stage attenuation mechanism. Their experimental results demonstrated that cascading filters could effectively double the suppression capacity compared to single-stage designs. However, they noted that the additional components increased cost and system complexity, making it less feasible for low-budget applications. The study did not compare the method with other alternatives, leaving room for further investigation into cost-effective designs. The researchers in [26] conducted a comparative analysis of various voltage suppression techniques, including snubber circuits, dV/dt

filters, and active damping methods. Their review provided insights into the advantages and drawbacks of each approach, concluding that dV/dt filters offered the best trade-off between effectiveness and implementation feasibility. However, they also pointed out that existing filter designs were mostly static and required reconfiguration when inverter switching parameters changed, underscoring the need for adaptive solutions.

Recent research by [27] explored the integration of machine learning algorithms for adaptive dV/dt filter tuning in inverter-cable-load systems. Their study proposed an intelligent control system that dynamically adjusted filter parameters based on real-time voltage measurements. Although their preliminary simulations showed promising results, the approach required further validation through hardware implementation to confirm its reliability in practical applications. Current studies extensively discuss the impact of fast-switching inverters on cable overvoltage but lack a comprehensive analysis on designing adaptive dV/dt filters that dynamically adjust to varying inverter rise times. Most proposed filters are designed for specific switching conditions, requiring redesign and replacement when the inverter characteristics change [28], [29]. Additionally, while transmission line theory is used to model wave propagation, limited work has been done on integrating real-world system constraints, such as long cable installations with complex load behaviors, into filter optimization strategies. The proposed dV/dt filter offers a more practical and cost-effective solution, as it is designed for worst-case transient conditions, ensuring broad applicability across different inverter rise times.

2. Methods

The electrical characteristics of a cable can be effectively analyzed using transmission line theory, which provides a mathematical framework for understanding wave propagation, impedance matching, and voltage reflection phenomena in long cable systems. Transmission line theory describes the behavior of electrical signals as they travel along a conductor, taking into account parameters such as resistance, inductance, capacitance, and conductance per unit length. These parameters play a crucial role in determining how voltage and current waves propagate through the cable and how they interact with connected loads. By applying equations derived from transmission line theory, key cable characteristics can be extracted and analyzed to assess their impact on system performance.

In this study, a two-wire cable configuration is considered. The two-wire cable model is commonly used in power electronic applications due to its simplicity and effectiveness in representing fundamental wave propagation effects. For the purposes of this analysis, the effect of electromagnetic coupling between the conductors is neglected. This assumption simplifies the mathematical modeling process while still providing meaningful insights into the voltage and current behavior along the cable. Electromagnetic coupling, which includes mutual inductance and capacitance effects between adjacent conductors, can introduce additional complexities that require more advanced modeling techniques. However, in applications where the coupling effect is minimal or where an initial approximation is sufficient, neglecting these interactions allows for a more straightforward analytical approach.

To facilitate the analysis, the cable is modeled using an elementary section representation rather than a fully distributed network model. This approach, illustrated in Figures 1 and 2, provided a simplified yet accurate depiction of the cable's electrical behavior. The elementary section consists of small, discrete segments that approximate the distributed nature of the cable, making it easier to apply transmission line equations for parameter extraction. This method is particularly useful in studying voltage

reflections, propagation delays, and overvoltage effects in inverter-fed systems. By breaking the cable into smaller sections, each with defined electrical properties, it becomes possible to analyze the transient response of the cable under different switching conditions. Equations (1)-(4) show how voltage and current change along a transmission line.

Figure 1. Transmission line equivalent circuit.

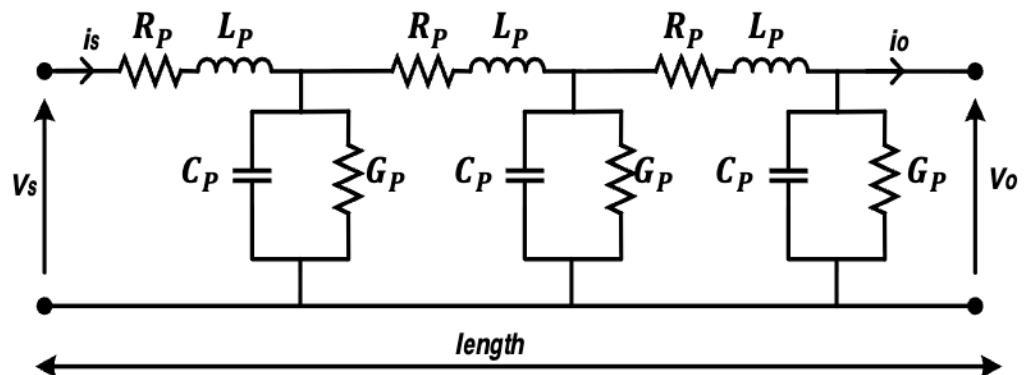
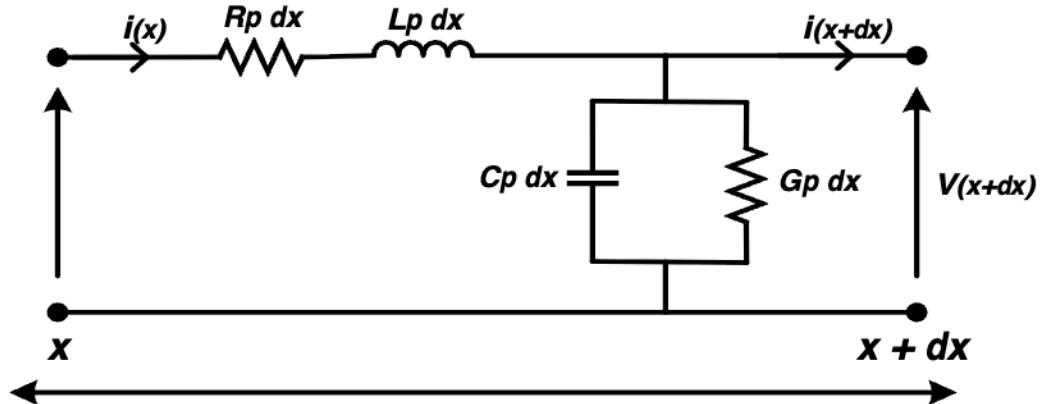


Figure 2. Elementary transmission line section.



$$\frac{\partial V}{\partial x} = -(R_p + j\omega L_p)I \quad (1)$$

$$\frac{\partial I}{\partial x} = -(G_p + j\omega C_p)V \quad (2)$$

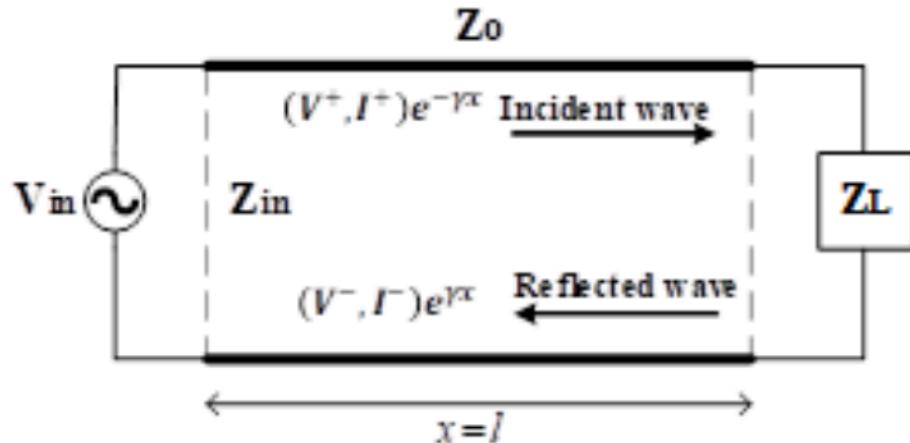
$$V(x) = V^+ e^{-\gamma x} + V^- e^{\gamma x} \quad (3)$$

$$I(x) = \frac{V^+}{Z_c} e^{-\gamma x} - \frac{V^-}{Z_c} e^{\gamma x} \quad (4)$$

where G_p is the per-unit-length conductance, C_p is the capacitance, j is the imaginary unit, R_p is the per-unit-length resistance, L_p is the inductance, I and V are the current and voltage at position x , respectively.

Figure 3 illustrates that the cable model can also be defined by its secondary parameters as characteristic impedance Z_c (ohms) and propagation constant γ (m^{-1}). The propagation constant defines the phase shift and attenuation of voltage and current waveforms of the cable. As shown in Figure 2, the elementary line section of the cable is made up of primary parameters, which are given as R_p , L_p , G_p , and C_p . They are the per-unit length resistance (Ω/m), inductance (H/m), conductance (S/m), and capacitance (F/m) of the cable. The secondary parameters related to the primary parameters are shown in equations (5)-(7).

Figure 3. Voltage reflection mechanism in a transmission line.



$$\gamma = \sqrt{(R_p + j\omega L_p)(G_p + j\omega C_p)} \quad (5)$$

$$Z_c = \frac{R_p + j\omega L_p}{\gamma} \quad (6)$$

$$Z_c = \sqrt{\frac{R_p + j\omega L_p}{G_p + j\omega C_p}} \quad (7)$$

where ω is the angular frequency in rad/s.

The primary parameters can also be extracted from the secondary parameters by using the following expressions, as seen in equations (8)-(9).

$$R_p + j\omega L_p = Z_c \gamma \quad (8)$$

$$G_p + j\omega C_p = \frac{\gamma}{Z_c} \quad (9)$$

2.1. Lossless Transmission Line

To simplify the analysis, several modeling assumptions are made. The inverter is modeled as an ideal voltage source with zero source impedance, and the switching device is assumed to be ideal, exhibiting instantaneous switching and no conduction loss. The cable is treated as a lossless transmission line, meaning the resistance R and conductance G per unit length are considered negligible. This allows the attenuation constant to be assumed zero, focusing the analysis on the characteristic impedance and propagation delay. The load is modeled as an open terminal, representing an infinite impedance condition, which maximizes voltage reflection and helps evaluate the worst-case surge scenario. The propagation constant γ (m^{-1}) of the cable is a complex parameter that is composed of attenuation constant α (Np/m) as the real part and phase shift β (rad/m) as the imaginary part. For a lossless transmission line model, the effect of cable resistance R_p and conductance G_p are considered to be negligible; therefore, the attenuation constant becomes zero [6]. Using the lossless transmission line condition, the propagation delay and characteristic impedance can be deduced as equations (10)-(11).

$$\gamma = \sqrt{(R_p + j\omega L_p)(G_p + j\omega C_p)} = \alpha + j\beta \quad (10)$$

$$R_p \ll \omega L_p, G_p \ll \omega C_p$$

$$\gamma = \alpha + j\beta = j\omega \sqrt{L_p C_p} \quad (11)$$

$$\alpha = 0, \beta = \omega \sqrt{L_p C_p}$$

Propagation velocity v (m/s) is determined by finding the ratio of angular velocity and phase shift as in equation (12).

$$v = \frac{\omega}{\beta} = \frac{\omega}{\omega \sqrt{L_p C_p}} = \frac{1}{\sqrt{L_p C_p}} \quad (12)$$

Propagation delay t_d (s) is then deduced from the ratio of cable length l (m) and propagation velocity, as seen in equation (13). Finally, characteristic impedance can be expressed as equation (14).

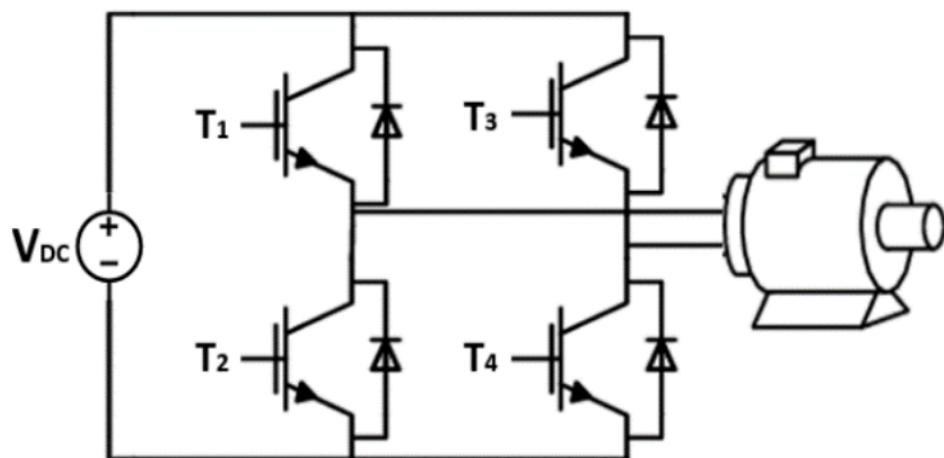
$$t_d = \frac{1}{v} = l \sqrt{L_p C_p} \quad (13)$$

$$Z_c = \sqrt{\frac{R_p + j\omega L_p}{G_p + j\omega C_p}} = \sqrt{\frac{L_p}{C_p}} \quad (14)$$

2.2. Voltage Surge Generation in Transmission Line

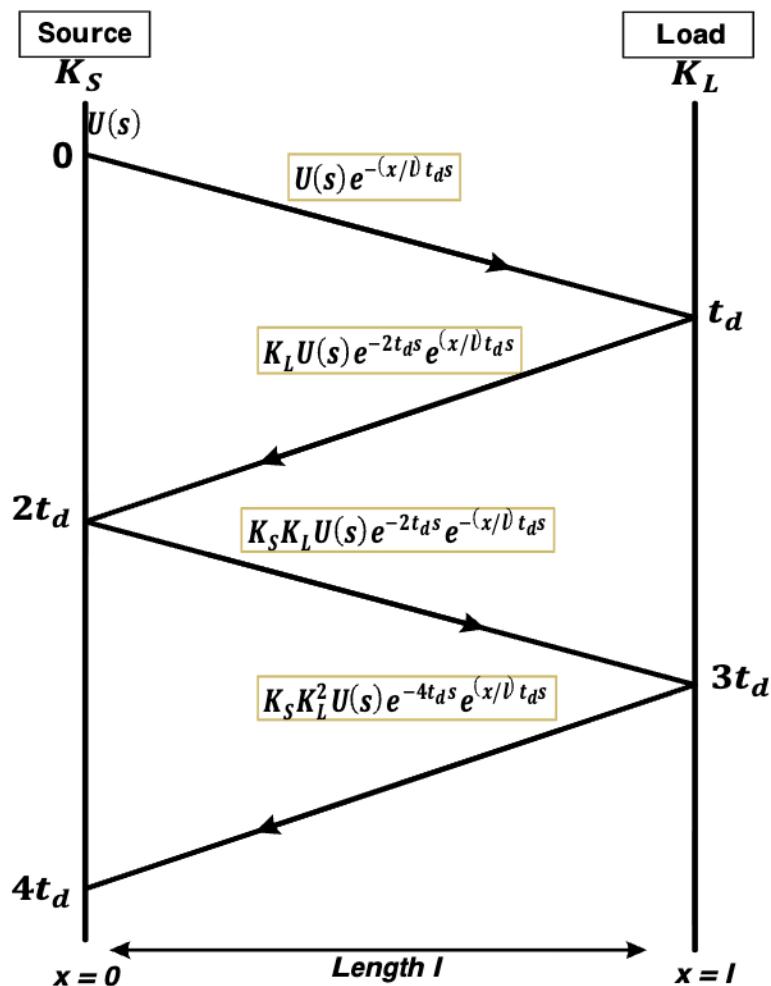
Voltage waves travel along a cable from a source to a load at a particular velocity. A typical example of a voltage source-cable-load system is an inverter motor drive system. The characteristic impedance and propagation delay were derived using standard per-unit-length parameters for two-wire cables, selected to reflect long-cable scenarios common in motor drives and submersible pump systems. A 44 ns propagation delay and 150 V DC link voltage were used to simulate high dV/dt conditions typical of real inverter-fed applications. Figure 4 shows the inverter-cable-motor system.

Figure 4. Inverter-cable-motor system.



The behavior of PWM pulses from an inverter to a high impedance load is similar to traveling waves on transmission lines. Voltage wave propagation can be demonstrated using a ladder diagram, as shown in Figure 5. The ladder diagram is used to illustrate voltage wave propagation in a power cable. The progress of the voltage waves in the ladder diagram is represented as a function of time and position. The position of the voltage wave in the cable is represented as x . Therefore, the location for the source and the load is represented as $x = 0$ and $x = l$, respectively. The injected voltage from the source is denoted as $U(s)$. The first propagating voltage wave at a distance x from the source is denoted by $v_1(x, t)^+$. Since $U(s)$ is delayed by $(x/l)t_d$ at position x , the first incident voltage wave at the load terminal can be expressed as equation (15).

Figure 5. Ladder diagram.



$$V_1(x, s) = U(s)e^{-(x/l)t_d} \quad (15)$$

All the voltage waves moving from the source to the load are denoted as "+" and are referred to as the forward traveling voltage wave. The forward propagating voltage wave is reflected and travels back to the source terminal upon reaching the load terminal. Voltage reflection occurs at the load terminal due to impedance mismatch between cable characteristics impedance and the load. The first reflected voltage at the load terminal can be expressed as equation (16).

$$V_1(l, s)^- = K_L V_1(l, s)^+ = K_L U(s)e^{-t_d} \quad (16)$$

Voltage waves traveling from load to source are denoted as “-” and are referred to as the backward traveling waves. At the source side, another reflection reoccurs. The reflected voltage at the source side can also be expressed as equation (17).

$$V_2(0,s)^+ = K_S V_1(0,s)^- = K_S K_L U(s) e^{-2t_{ds}} \quad (17)$$

Voltage reflection coefficient at the load and source side are given as equation (18).

$$K_L = \frac{Z_L - Z_c}{Z_L + Z_c}; K_S = \frac{Z_S - Z_c}{Z_S + Z_c} \quad (18)$$

When the load terminal is much larger compared to the cable characteristics impedance, the load reflection coefficient is approximated to 1. On the other hand, when the source impedance is much smaller compared to the characteristic impedance, then the source reflection coefficient can be approximated to -1. Load reflection coefficient of $K_L = 1$ indicates a full voltage reflection at the load terminal without a phase change, while the source reflection coefficient of $K_S = -1$ indicates a full reflection at the source side with a 180° phase change. The voltage reflection cycles in the inverter-cable-load system continue infinitely. As a result, the voltage on the cable is represented as the sum of the infinite voltage wave reflections. The total voltage reflection series in the inverter-cable-load system is determined by adding the forward traveling voltage waves and backward traveling waves. The sum of all the forward traveling waves is denoted as $V(x,s)^+$ while the sum of all the backward traveling waves is represented as $V(x,s)^-$, as shown in equations (19)-(22).

$$V(x,s)^+ = U(s) [e^{-(x/l)t_{ds}} + K_L K_S e^{-((2l+x)/l)t_{ds}} + K_L^2 K_S^2 e^{-((4l+x)/l)t_{ds}} + \dots] \quad (19)$$

$$V(x,s)^+ = \frac{U(s) e^{-(x/l)t_{ds}}}{1 - K_L K_S e^{-2t_{ds}}} \quad (20)$$

$$V(x,s)^- = U(s) [K_L e^{-((2l-x)/l)t_{ds}} + K_L^2 K_S e^{-((4l-x)/l)t_{ds}} + K_L^3 K_S^2 e^{-((6l-x)/l)t_{ds}} + \dots] \quad (21)$$

$$V(x,s)^- = \frac{U(s) K_L e^{-((2l-x)/l)t_{ds}}}{1 - K_L K_S e^{-2t_{ds}}} \quad (22)$$

The sum of forward $V(x,s)^+$ and backward traveling voltage $V(x,s)^-$ can be used to find voltage at any point x of the cable, as seen in equation (23)-(24).

$$V(x,s) = V(x,s)^+ + V(x,s)^- \quad (23)$$

$$V(x,s) = U(s) \frac{e^{-(x/l)t_{ds}} + K_L e^{-2t_{ds}} e^{(x/l)t_{ds}}}{1 - K_L K_S e^{-2t_{ds}}} \quad (24)$$

As shown in the ladder diagram voltage at the inverter output is a sum of even propagation delayed voltage waves while load terminal voltage is the sum of odd propagation delayed voltage waves. Voltage value at the inverter output is determined when distance $x = 0$ while load peak voltage is deduced for distance $x = l$. Therefore, inverter output voltage $V(0,s)$ and load terminal voltage $V(l,s)$ can be obtain by substituting the value of x in equation (25).

$$V(0,s) = U(s) \frac{1 + K_L e^{-2t_{ds}}}{1 - K_L K_S e^{-2t_{ds}}}; V(l,s) = U(s) \frac{(1 + K_L) e^{-t_{ds}}}{1 - K_L K_S e^{-2t_{ds}}} \quad (25)$$

3. Results and Discussion

The effect of inverter rise time on cable terminal voltage is demonstrated through simulation analysis. The source has zero impedance while cable end terminal is left open to create an infinite load. Therefore, reflection coefficients for the source and load can be expressed as $K_S = -1$ and $K_L = 1$, respectively. With a DC link voltage of 150 V and propagation delay of 44 ns cable peak voltages corresponding to a given inverter rise time and a propagation delay relation can be computed. The rise time is defined as t_r relative to the propagation delay t_d of the cable. The inverter's step voltage input results in multiple voltage reflections, and the peak voltage depends on how many full wavefronts have arrived at the load within the rise time. Each reflected wave adds constructively at the load terminal if timed appropriately.

- For $t_r \leq 2t_d$ (Figure 6,7), cable peak voltage can be calculated in equation (26).

$$V_{peak} = V_{dc}(1 + K_L) \quad (26)$$

hence, the V_{peak} is obtained at 300 V.

Figure 6. Inverter rise time less than propagation delay.

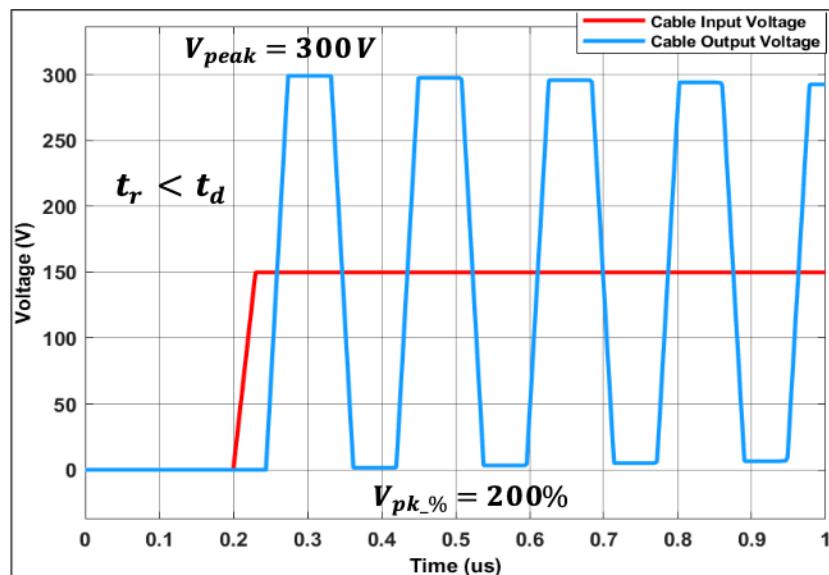
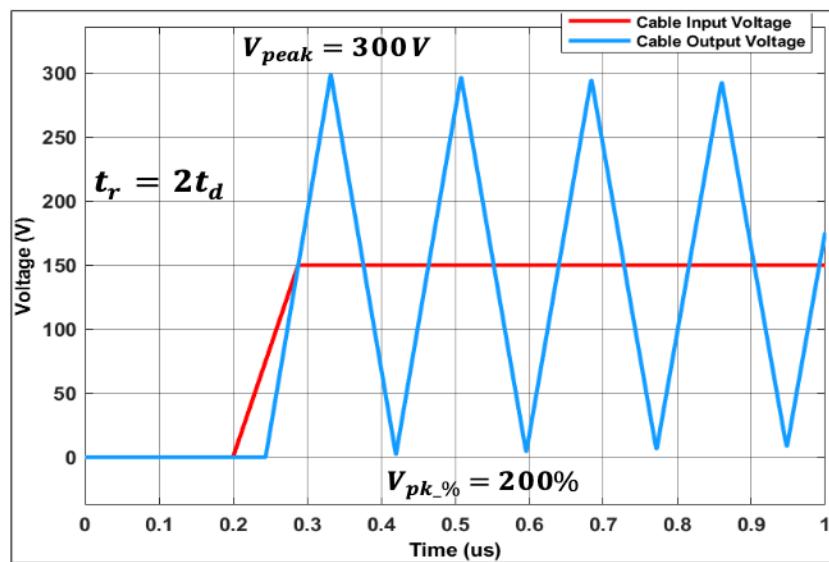


Figure 7. Inverter rise time equals twice propagation delay.

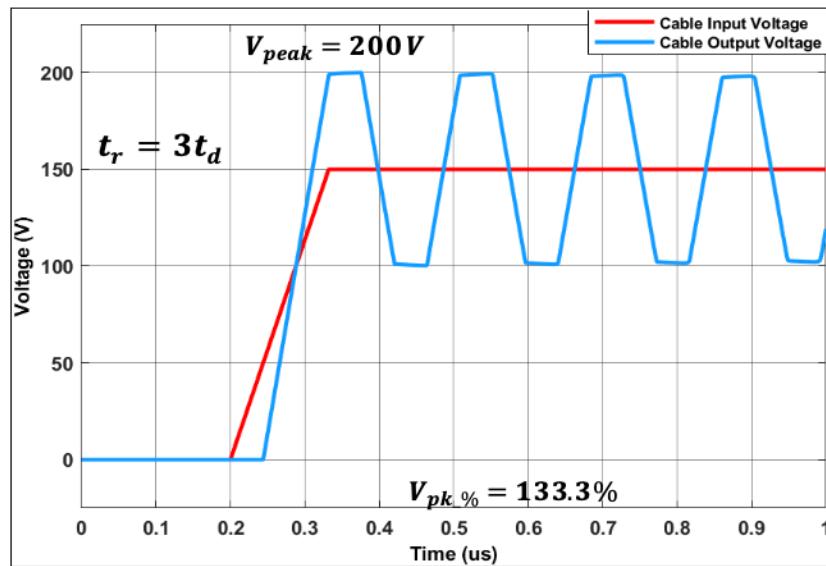


- For $t_r = 3t_d$ (Figure 8), the peak voltage is calculated using equation (27).

$$V_{peak} = (1 + K_L) \left(\frac{3t_d \times V_{dc}}{t_r} \right) + (K_L K_S + K_L^2 K_S) \left(\frac{t_d \times V_{dc}}{t_r} \right) \quad (27)$$

hence, the V_{peak} is obtained at 200 V.

Figure 8. Inverter rise time equals three times propagation delay.



Load peak voltage as shown in Figure 6-8 is highly dependent on the inverter rise time t_r and cable propagation delay t_d . Full voltage reflection occurs at the load terminal when inverter rise time is less or same as twice the delay ($t_r \leq 2t_d$).

An expression for computing load peak voltage for inverter rise time and propagation delay relation have been deduced in this paper. If the inverter rise time is an odd multiple of the cable propagation delay, the load peak voltage can be defined as equation (28).

$$t_r = m \cdot t_d; \quad m = 1, 3, 5, \dots$$

$$t_r = t_d, 3t_d, 5t_d, \dots$$

$$V_{peak} = \frac{V_{dc}(1 + K_L)}{t_r} \sum_{x=0}^{\frac{m-1}{2}} (K_L^x K_S^x)(m - 2x)t_d \quad (28)$$

$$x = 0, 1, 2, \dots, \frac{m-1}{2}$$

On the other hand, if inverter rise time is an even multiple of the cable propagation delay, the load peak voltage can be determined as equation (29).

$$t_r = m \cdot t_d; \quad m = 2, 4, 6, \dots$$

$$t_r = 2t_d, 4t_d, 6t_d, \dots$$

$$V_{peak} = \frac{V_{dc}(1 + K_L)}{t_r} \sum_{x=0}^{\frac{m-2}{2}} (K_L^x K_S^x)(m - 2x)t_d \quad (29)$$

$$x = 0, 1, 2, \dots, \frac{m-2}{2}$$

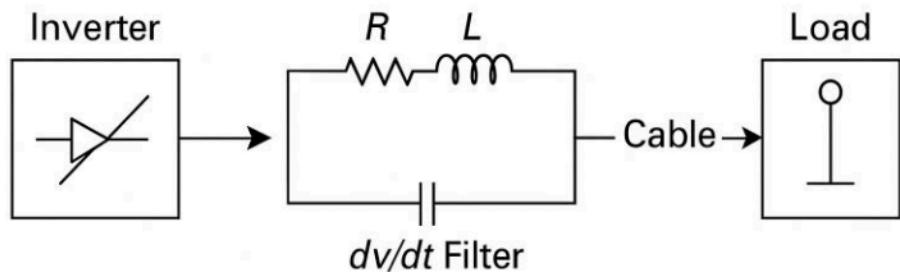
3.1. Proposed dV/dt Filter Design

To mitigate the worst-case voltage surge, a single-stage dV/dt filter is designed based on the worst-case rise time condition (step input: $t_r=0$). The filter consists of an R-L-C low-pass network designed to attenuate high-frequency components of the voltage step before reaching the cable. The cutoff frequency is chosen as equation (30).

$$f_c = \frac{1}{2\pi\sqrt{LC}} < \frac{1}{2t_d} \quad (30)$$

This ensures attenuation of the highest frequency components that cause steep voltage transitions. A schematic of the proposed filter is shown in Figure 9.

Figure 9. dV/dt filter.



The simulation results confirm the analytical prediction that the inverter rise time has a strong impact on peak load voltage. As shown in Figure 6-8, when the inverter rise time is shorter than the cable's propagation delay ($t_r < t_d$), the load voltage surges to approximately twice the DC link voltage (300 V for a 150 V source). This occurs due to overlapping reflections at the load terminal. As the rise time increases to two or three times the propagation delay (Figures 7 and 8), the peak voltage gradually reduces. When $t_r = 2t_d$, the peak voltage is around 1.5 times the DC link value. At $t_r = 3t_d$, the overvoltage reduces to 1.25 times, indicating a significant reduction in reflection severity. Figure 10 and table 1 summarizes this relationship between rise time and peak voltage.

Figure 10. Inverter rise time and cable propagation delay.

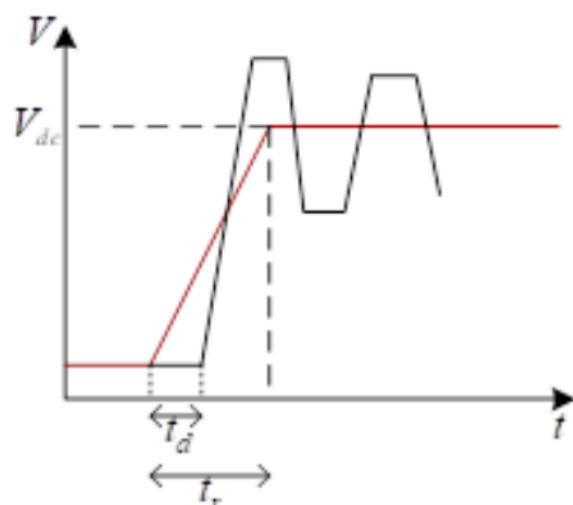


Table 1. Load peak voltage for different inverter rise times.

Inverter Rise Time (ns)	Relation to Propagation Delay	Load Peak Voltage (V)
10	$t_r < t_d$	300.0
44	$t_r = t_d$	300.0
88	$t_r = 2t_d$	300.0
132	$t_r = 3t_d$	225.0
176	$t_r = 4t_d$	187.5

3.2. Sensitivity Analysis

To evaluate the robustness of the analytical model, a parameter sweep was conducted to assess how variations in cable length and inverter rise time affect the peak voltage at the load terminal. The propagation delay t_d was varied by adjusting the cable length from 10 m to 50 m, while the inverter rises time t_r ranged from 10 ns to 200 ns. The DC link voltage was fixed at 150 V in all cases. Table 2 illustrates how peak voltage responds to changes in the t_r/t_d ratio. As shown, when $t_r < 3t_d$, the load voltage exceeds 225 V and can reach up to 300 V (i.e., twice DC link voltage). As the rise time increases beyond this threshold, the voltage begins to stabilize, approaching the DC link value. This confirms that the model is highly sensitive to short inverter rise times and that even modest increases in t_r can significantly suppress voltage surges. Additionally, cable length variations had a linear impact on propagation delay, affirming the theoretical relationship and validating the practical adaptability of the model across various installation scales. These results demonstrate that the proposed model remains reliable across a wide range of system configurations, reinforcing its value in practical inverter-cable-load scenarios.

Table 2. Peak voltage response to changes in t_r/t_d ratio.

Cable Length (m)	Propagation Delay (ns)	Inverter Rise Time (ns)	Peak Load Voltage (V)
10	8.8	10	300
20	17.6	44	300
30	26.4	88	262.5
40	35.2	132	225
50	44.0	176	187.5

4. Conclusions

The results show that when the inverter rise time is shorter than three times the cable propagation delay, voltage reflections occur along the transmission path, leading to a significant amplification of the voltage at the load terminal, which can reach up to twice the DC link voltage. This phenomenon poses serious risks to insulation integrity, system reliability, and overall equipment lifespan. Excessive voltage stress can accelerate insulation degradation in cables and motor windings, cause premature failure of semiconductor components, and increase electromagnetic interference, potentially disrupting nearby electronic devices and control systems. To mitigate these risks, it is essential to design inverters with controlled rise times to ensure smoother voltage transitions that minimize reflections and voltage surges. Additionally, implementing voltage suppression techniques such as dV/dt filters, RC snubbers, and active switching control strategies can help regulate transient overvoltage and enhance system stability.

dV/dt filters limit the rate of voltage change, reducing reflections and mitigating voltage spikes, while RC snubbers absorb excess energy to prevent sudden voltage jumps.

Furthermore, adaptive switching techniques, where inverter switching characteristics dynamically adjust based on cable and load conditions, can offer a more robust solution to overvoltage issues. This method is particularly suitable for high-frequency inverter-fed systems used in deep-well submersible pumps, off-shore oil platform motors, and electric submersible pumps used in water supply and petroleum extraction. These systems often involve long, inaccessible cable runs where conventional surge protection techniques like load-end filters are impractical. Implementing the proposed dV/dt filter at the inverter output can provide a cost-effective and maintenance-friendly solution in such constrained environments. Future pilot studies could be carried out in desalination plants using deep-sea pumps or geothermal energy extraction setups, where long cable lengths and harsh environments necessitate robust overvoltage protection. Future research should focus on refining dV/dt filter designs, optimizing adaptive inverter switching strategies, and experimentally validating the theoretical models to confirm their real-world applicability. The research will focus on the experimental validation of the proposed analytical model and dV/dt filter design using real-time simulation and hardware-in-the-loop platforms. Specifically, platforms such as dSPACE, OPAL-RT, or Typhoon HIL will be employed to emulate inverter-cable-load systems under varying switching conditions. These platforms offer real-time testing capabilities and allow integration of physical inverter hardware with virtual cable and load models.

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