

GROUP 3
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The diagram illustrates a 1028-bit adder-subtractor circuit. It features three main input registers: **3B** (1026 bits), **B** (1024 bits), and **M** (1024 bits). The **in_a** input is split into **a_mux** (1026 bits) and **A[1023:2]** (2 bits). The **in_b** input is split into **B** (1024 bits) and **B, 1'b0** (1027 bits). The **in_m** input is split into **M** (1024 bits) and **M, 1'b0** (1027 bits). The circuit uses a series of multiplexers (**a_mux**, **b_mux**, **m_mux**, **c_mux**) and adders (**A**, **B**, **M**, **C**) to perform the operation. The final result is stored in a 1028-bit register **C**. The diagram is labeled with "GROUP 3", "Arnaud Van Mieghem", "Wim Kunnen", and "Yrjo Koyen".