# SCμM-V23: Towards A Crystal-Free System-On-Chip For IoT In 16nm

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***Abstract*—We present progress on the Single-Chip Micro Mote V (SCμM-V), a crystal-free system-on-chip (SoC) for internet-of-things (IoT) and microrobotic applications. The SoC includes a 32-bit RISC-V "Rocket" processor generated using the Rocket Chip generator and the Chipyard framework, a custom crystal-free 2.4 GHz transceiver that was designed to be standards-compatible with IEEE 802.15.4 PHY and Bluetooth Low Energy (BLE) 1M PHY but is known not to work, crystal-free clock generation, on-chip power management, a μV-precision ADC, and a 90 GHz FMCW radar transmitter, all of which are still in the process of being brought up and characterized. SCμM-V was designed and taped out in one semester in the Intel 16 process by nine undergraduate and eleven graduate students as part of the spring 2023 iteration of the "Tapeout" class at UC Berkeley. In this paper, we discuss the design and architecture of SCμM-V, present preliminary measurements of its RF, power, clock, and digital blocks, and consider implications for deploying SCμM-V in a wireless sensor network.**

***Index Terms*—crystal-free system-on-chip, wireless sensor node, internet of things, tapeout class**

## I. Introduction

As wireless sensor networks and the internet-of-things (IoT) become increasingly relevant for applications such as infrastructure monitoring, biomedical devices, and agriculture and environmental sensing, there is a need for a maximally integrated SoC able to meet the low size, weight, power, and cost (SWaP-C) requirements. The Single-Chip Micro Mote (SCμM) project seeks to build a low-cost, low-power, wireless sensor mote. The elimination of an external crystal as a frequency reference allows SCμM to operate as a fully integrated, chip-scale system with a power budget in the hundreds of μW and a 10x to 100x reduction in size and power over typical commercial wireless devices.

Previous work on the SCμM project has demonstrated the feasibility of this concept. Maksimovic *et al.* presented SCμM-3C, a $2 \times 3 \times 0.3$ mm$^3$ crystal-free SoC in TSMC's 65 nm process [1] featuring an Arm Cortex-M0 microprocessor, a standards-compatible 2.4 GHz transceiver, and an optical bootloader [2]. The crystal-free oscillators' performance was characterized in [3].

The tapeout class was introduced at UC Berkeley in spring 2017 with the goal of introducing undergraduate and junior graduate students to the tapeout process [4]. The spring 2021 iteration of the tapeout class taped out a standards-compatible 2.4 GHz radio transmitter with a RISC-V microprocessor in TSMC 28 nm that used an external crystal reference [5] and successfully demonstrated wireless transmission of a BLE advertisement packet to a commercial receiver [6]. Recent iterations of the tapeout class, including the spring 2023 iteration, have been developing SCμM-V, a crystal-free SoC with a 2.4 GHz transceiver, in the Intel 16 process.

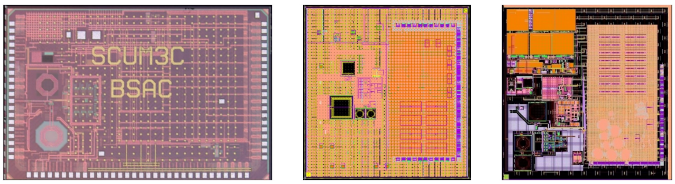


Fig. 1: From left to right: SCμM-3C [1], SCμM-V22, and SCμM-V23.

SCμM-V has been through two revisions: SCμM-V22, originally taped out in spring 2022, and SCμM-V23, taped out in spring 2023. SCμM-V23 has the following key features, as shown in Figure 2:

- 32-bit RISC-V core capable of up to 200 MHz
- On-chip 256 kB SRAM, 8 kB I-cache, and 8 kB D-cache
- Crystal-free BLE and IEEE 802.15.4 fully custom analog front-end and digital baseband-modem processor.
- Crystal-free on-chip clock generation
- On-chip power management with voltage and current references, low-dropout voltage regulators, and a DC-DC switched capacitor converter.
- Cryptography accelerators (AES-128, ECC, and SHA-256)
- μV-precision ADC
- 90 GHz FMCW radar transmitter

Additionally, the SCμM-V23 chip exposes two GPIO pins, a single UART bus, a QSPI flash bus, JTAG, and a capture and compare interface for the crystal-free RTC.

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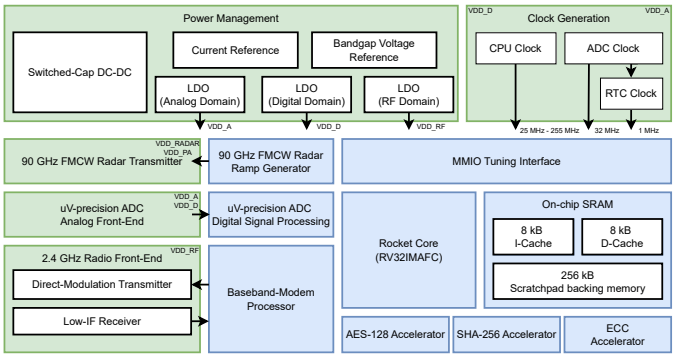


Fig. 2: System diagram of SCμM-V23.

## II. Digital Core

SCμM-V23 includes a 32-bit Rocket, which has a high-performance single-issue in-order execution pipeline, with a peak sustainable execution rate of one instruction per clock cycle [7]. The core supports Machine and User privilege modes as well as standard Integer, Multiply, Atomic, Floating-Point and Compressed RISC-V extensions (RV32IMAFC).

The digital core has been successfully brought up using the serialized TileLink interface, one of three available boot methods. The other available boot methods include tethered boot via JTAG and self-boot via QSPI flash. The core has been demonstrated to run at frequencies from 200 kHz to 100 MHz with further testing ongoing.

Significant improvements in the digital core's power consumption were made from SCμM-V22 to SCμM-V23. Leakage power was reduced from 36 mW to 0.045 mW in post-tapeout testing despite a 3% increase in area utilization from one generation to the next. This was accomplished through use of lower power SRAM macros. As shown in Figure 4, benchtop dynamic power consumption testing of SCμM-V23 indicated approximately 61.69 μA/MHz for the CPU clock domain and 49.16 μA/MHz for the ADC clock domain. The Rocket Core, memory, and accelerators reside in the CPU clock domain while the baseband-modem processor and μV-precision ADC DSP are in the ADC clock domain.

## III. Cryptography Accelerators

As secure and low-power wireless links continue to be a focus for wireless sensor networks [8], cryptography accelerators and coprocessors help alleviate the CPU bandwidth burden from these computationally intense tasks. SCμM-V includes AES-128, ECC and SHA-256 accelerators to enable efficient encryption, decryption, and hashing. These accelerators were adapted from open source Verilog implementations in [9] and wrapped into the Chipyard ecosystem as Rocket coprocessors (RoCC).

The AES accelerator is exposed to software running on the core by software interrupts. The process involves loading the encryption key and message, initiating the encryption or decryption process, and optionally utilizing diagnostic tools to monitor cycle time for computation completion. The implementation was verified before submission through C testbenches and validated with third-party online software tools. Simulations showed on average 6 cycles per word, which equates to about 10 ns per byte for AES operations.

The SHA-256 accelerator combines multiple hash functions for its operation. It divides data into eight 16-bit chunks, denoted as A to H, and performs bitwise XOR, AND, and bit-shifting operations on these chunks. It shares similar implementation and capabilities with the AES accelerator, with the exception of its hashing functionality. Functionality was similarly verified through C testbenches prior to tapeout, and these testbenches showed approximately 107 cycles to process 256 bits of data, equivalent to approximately 70 ns per byte for hash computations.

## IV. IEEE 802.15.4 and BLE Baseband-Modem Processor

A first version of the custom digital baseband-modem processor was originally presented in [6], where it was shown to successfully transmit BLE 1M PHY standards-compliant packets. Since then, the baseband-modem has been expanded to add a second mode that aims for IEEE 802.15.4 2.4 GHz PHY standards compliance as well as several unique features to enable crystal-free radio operation. The baseband-modem handles BLE packets at a rate of 1 Msym/s and IEEE 802.15.4 packets at a rate of 2 Msym/s.

The CPU provides packet payloads for transmission to the baseband processor using direct memory access (DMA). In receive mode, incoming packets will trigger several interrupts and provide the packet to the core via DMA. Additionally, the baseband-modem exposes an interface for software to read and write configuration and tuning bits to the radio front-end.

The architecture of the baseband-modem, shown in Figure 5, is organized into three distinct functional areas: the BLE baseband, the IEEE 802.15.4 baseband, and a "unified" modem. In this work, the "baseband" refers to the implementation of PHY and link layer packet and payload standards definitions. The BLE and IEEE 802.15.4 basebands handle the packet assembly on transmission and packet disassembly on receipt.

The modem is unified to the extent allowed by differences in the BLE and IEEE 802.15.4 PHY definitions. In the modem's transmit chain, modulation for BLE packets is done by sampling a modulation LUT with the output of a Gaussian FIR filter driven by the whitened BLE packet bitstream. For IEEE 802.15.4, the modulation LUT is sampled by an FSM that leverages O-QPSK and MSK equivalence as demonstrated in [10].

The baseband-modem includes both an LO/32 counter and an IF counter to support the SoC's crystal-free design. The IF counter calculates the time elapsed for N rising edges in the received 2 MHz IF signal by taking the difference between the accumulated 32 MHz clock count before and after N rising edges are identified. This can then be used to determine the IF frequency and tune the LO. As long as the 32 MHz clock has an error of less than 4%, an IF frequency error of $< 4\%$

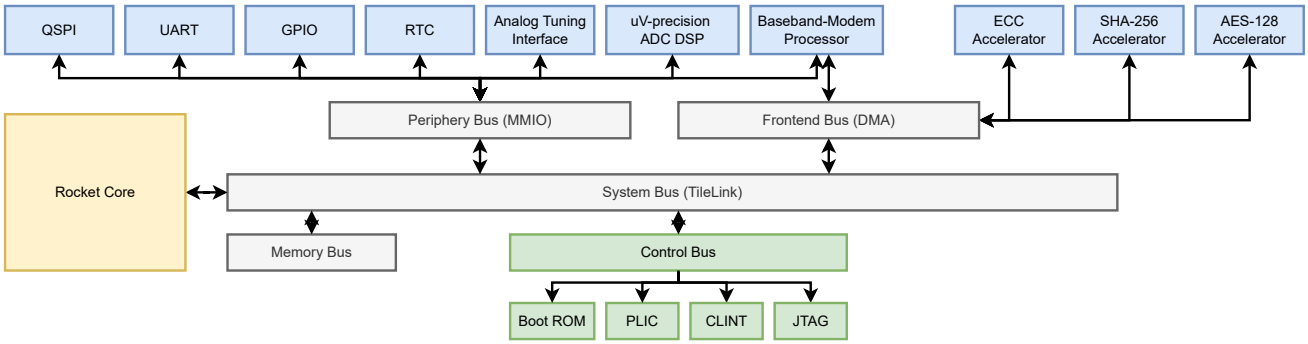


Fig. 3: Overview of the Chipyard-generated digital core.

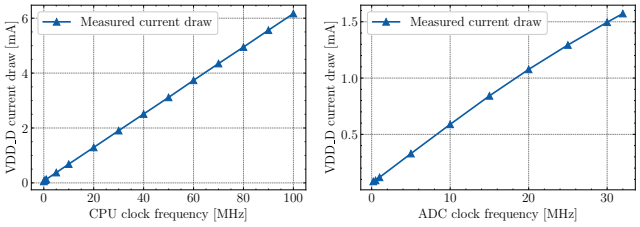


Fig. 4: VDD_D current draw during dynamic power consumption testing of the CPU and ADC clock domains.

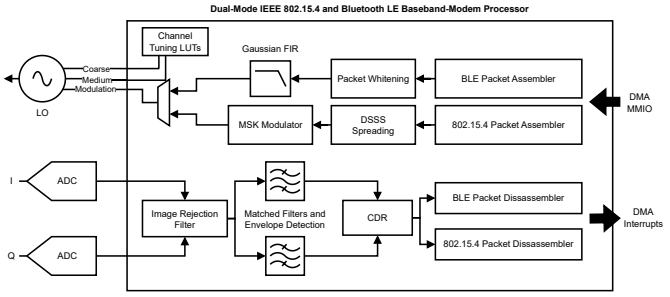


Fig. 5: Dual-mode IEEE 802.15.4 and BLE baseband-modem processor system overview.

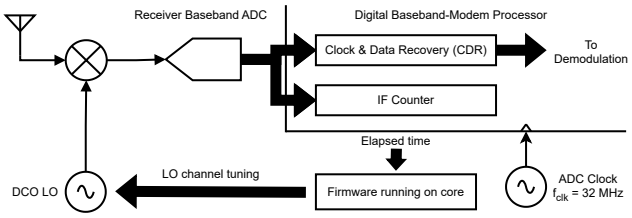


Fig. 6: The zero-crossing IF counter can be used to tune the LO, creating a feedback loop that controls the drift of the crystal-free local oscillator [11].

TABLE I: Target Link Budget Analysis.

| Block | Gain [dB] | NF | IIP3 | Tot. IIP3 | Tot. SNR |
|---|---|---|---|---|---|
| Ant. | 0.00 | 0.00 | – | – | 30.00 |
| LNA | 20.00 | 6.00 | –10.00 | –10.00 | 24.00 |
| Mixer | –3.00 | 3.00 | –10.00 | –30.04 | 23.99 |
| VG-TIA | 10.00 | 6.64 | 30.00 | –30.04 | 23.91 |
| BPF | 0.00 | 1.00 | – | –30.04 | 23.91 |
| VGA | 40.00 | 20.00 | 30.00 | –30.05 | 23.65 |
| ADC | 0.00 | 0.00 | – | –30.05 | 23.65 |

results in an LO frequency error less than the 40 ppm limit imposed by IEEE 802.15.4.

This feedback loop created by the IF counter feature between crystal-referenced ambient radio traffic and the LO can be used to achieve higher accuracy and reduce drift, as described in Figure 6. Another major advantage is that the resulting 32 MHz counter output, after the feedback system has stabilized, will approach real-time accuracy.

## V. Crystal-Free 2.4 GHz Radio Front-End

While the on-chip custom radio front-end was found to be largely non-functional during bring-up testing, it was designed to operate in the 2.4 GHz ISM band from 2.4 GHz to 2.4835 GHz, covering the forty 2 MHz BLE channels and the sixteen 5 MHz IEEE 802.15.4 channels. The architecture is shown in Figure 7a.

The crystal-free transmitter uses a direct modulation architecture based on [11], where the digitally controlled LO, implemented as a class B LC tank at 4.8 GHz with cross-coupled inverters, is tuned using the 10-bit coarse and 6-bit medium control bits and then modulated using the 8-bit modulation control bits, as shown in Figure 7b. The medium and modulation capacitive DACs implement the capacitive degeneration technique presented in [12] and were designed to have a tuning bandwidth of 20% of the center frequency with a tuning resolution smaller than 192 kHz to meet the strictest 40 ppm frequency requirements of IEEE 802.15.4 and BLE. The DCO is followed by a buffer that prevents kickback from the 2x frequency divider that then produces the desired 2.4 GHz tone.

The receiver implements a low-IF architecture and was designed to function over an input power range from –70 dBm to –10 dBm As part of the initial link budget estimations, a BER of 0.1%, which corresponds to an SNR of 12.5 dB, was targeted over several in-band and out-of-band interference conditions for a –67 dBm input signal. This target link budget is shown in Table I.

The receiver supports automatic gain control based on

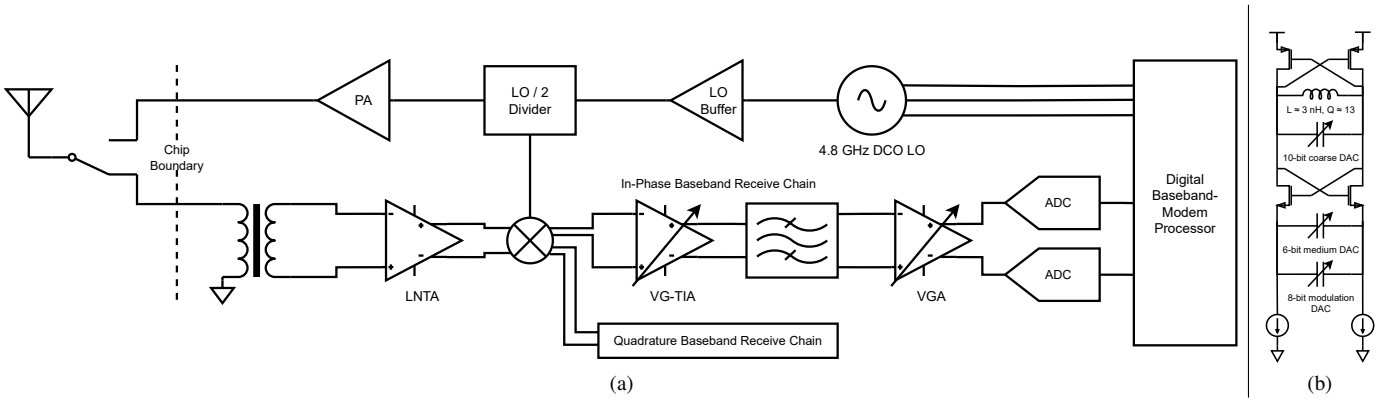


Fig. 7: (a) Custom 2.4 GHz crystal-free radio front-end. (b) Class B crystal-free 4.8 GHz DCO based on [11] with cross-coupled inverters and a tunable LC tank, consisting of an on-chip inductor and a widely tunable 24-bit capacitive DAC.

tuning the VGA and VG-TIA stages as well as DC offset correction (DCOC) via tuning of the current DAC at the input of the final VGA stage. A pseudo-differential SAR ADC at 32 MHz terminates the custom analog receive chain. This SAR ADC was designed in and generated by the Berkeley Analog Generator (BAG), with both schematic and layout phases of design heavily automated [13].

## VI. Clocks

SCμM-V features two clocks: the ADC clock and the CPU clock. The ADC clock, generated in the analog power domain with a designed frequency of 32 MHz, is routed to several blocks, including the 2.4 GHz radio front-end's ADC, the digital baseband-modem processor, and the μV-precision ADC, where precise tuning resolution is critical to providing an accurate sampling rate for digital signal processing. The CPU clock, generated in the digital power domain with a tunable frequency between 25 MHz and 255 MHz, is the primary clock for the digital core, including the Rocket Core, data buses, and peripherals without digital signal processing.

### A. ADC Clock

The ADC clock, shown in Figure 8a, was designed to run at a frequency of 32 MHz and is generated by an RC ring oscillator based on [14] with a tunable 16-bit capacitive DAC consisting of a binary 12-bit capacitive DAC from 0.138 fF to 111.34 fF, a 4-bit capacitive DAC, each controlling 0.138 fF, and a fixed 1.56 fF capacitor.

The tuning range of the ADC clock as a function of the 16-bit capacitive DAC code was measured and is plotted in Figure 9. Bench-top testing showed the oscillator missed the intended clock frequency of 32 MHz, and measurements of the 4-bit capacitive fine DAC allowed for a tuning resolution of around 10 kHz/LSB, exceeding the minimum 2.56 kHz/LSB specification to meet the strictest ±40 ppm timing requirement of IEEE 802.15.4 and BLE. Furthermore, we measured the phase noise of the ADC clock on a spectrum analyzer at an offset of 10 kHz, 100 kHz, and 1 MHz, and calculated an RMS jitter of around 1 ns, equivalent to around 32 ms of jitter over 1 s or around 0.13 ms within a single 127-byte 802.15.4 packet.

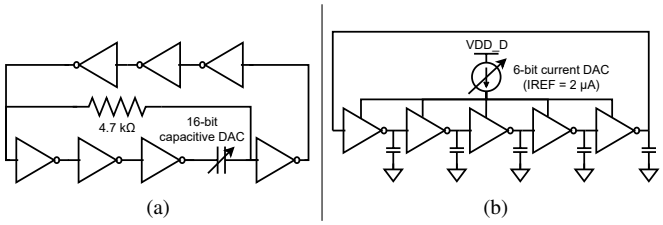


Fig. 8: (a) RC ring oscillator with a 16-bit capacitive DAC to generate the 32 MHz ADC clock. (b) Current-starved RC ring oscillator with a current DAC to adjust the CPU clock frequency.

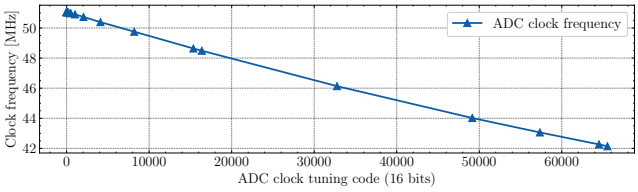


Fig. 9: Measured ADC clock tuning range with the 16-bit capacitive DAC.

The 1 MHz RTC is derived from the ADC clock with a 32x clock divider and is exposed to the firmware on the digital core by capture and compare registers to enable applications that require precise timing. Deriving the RTC from the ADC clock implies that the RTC inherits the ADC clock's precision and accuracy as the ADC clock is typically tuned to ambient true references as shown in Figure 6.

### B. CPU Clock

The CPU clock is generated by a current-starved RC ring oscillator consisting of five inverter stages, each with a 4.16 fF capacitor at its output, as shown in Figure 8b. The speed of the CPU clock can be controlled using the 6-bit current DAC with a reference current of 2 μA. The CPU clock was designed for tunable operation between 25 MHz, to support QSPI self-boot at a maximum clock frequency of 50 MHz, and 255 MHz.

## VII. Supply

The SoC has multiple power domains that isolate functionally similar blocks and allow for low-power operation by turning off select power domains when not in use.

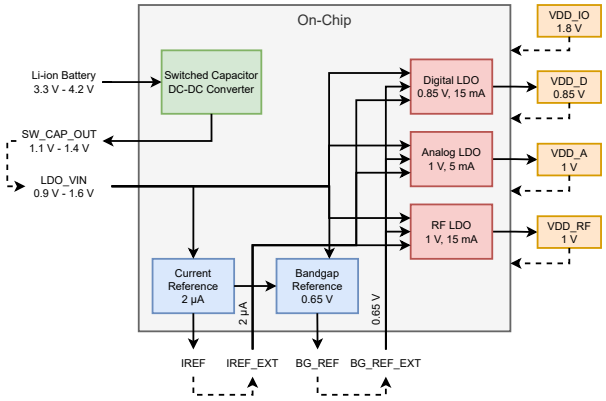


Fig. 10: Supply diagram of SCµM-V23.

### A. Switched-Capacitor DC-DC Converter

An on-chip switched-capacitor DC-DC converter was designed to step down the higher voltages of lithium-based batteries (3.3 V – 4.2 V) to the same voltage range of alkaline batteries (0.9 V – 1.6 V). The switched-capacitor converter design uses a 3:1 ladder topology but is also reconfigurable for 2:1 and 3:2 in order to utilize the full battery voltage range. A current-starved ring oscillator provides the nominally 100 MHz switching clock to the switched-capacitor circuit.

In benchtop testing, the DC-DC converter was tested in the 3:1 and 2:1 configurations, as shown in Figure 11. In the 3:1 configuration, the converter produced a regulated voltage capable of supplying the on-chip LDOs for load currents of up to 16 mA when supplied with 4.2 V. The 2:1 configuration displayed a higher load current limit before failure than the 3:1 configuration.

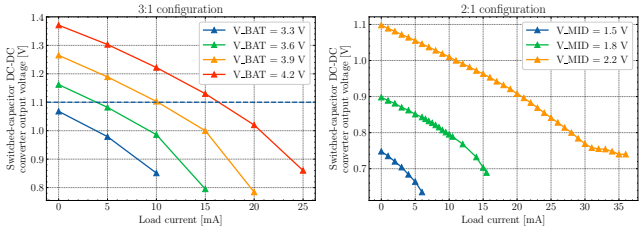


Fig. 11: Output voltage of the DC-DC converter as a function of the load current in the 3:1 and 2:1 configurations. $V_{BAT}$ and $V_{MID}$ are the inputs for the 3:1 and 2:1 configurations, respectively.

### B. Low-Dropout (LDO) Voltage Regulators

SCµM-V23 features three LDO voltage regulators to supply the analog, digital, and RF blocks, as shown in Figure 10. All regulators are designed for an input voltage between 1.1 V and 1.8 V with a bandwidth of 35 MHz, a phase margin of 60°, and a PSRR of 26 dB. The maximum output current of the RF and digital LDOs is 15 mA while the analog LDO is designed to output up to 5 mA.

The LDOs were characterized by providing an input voltage of 1.5 V and connecting the regulated output to a Keithley SMU to measure the regulated voltage as a function of the load current, which is shown in Figure 12. Compared to simulations, all of the LDOs are unable to regulate their output voltage when supplying their maximum current.

### C. Current Reference

The on-chip current reference generation circuit aims to output a temperature- and supply-independent 2 µA current source when supplied with a 0.9 V to 1.6 V alkaline battery It includes a start-up circuit and is used with a custom utility current DAC to distribute reference currents to other analog designs on the SoC.

The current source is created by subtracting two beta-multiplier supply-dependent reference circuits to create a supply-independent output current. Each beta-multiplier circuit includes resistors trimmed at design-time for a nominal temperature of 27 °C.

The current reference was characterized with a Keithley SMU by measuring the variation in the generated reference current as a function of the load voltage at the IREF pin. As shown in Figure 13, the measurements matched the simulations well, and for an output voltage between 0.8 V and 1.6 V, the reference current varied by no more than 10 nA. Nominally, for a current of 2 µA, we expect IREF to be at around 1.1 V.

### D. Bandgap Voltage Reference

The bandgap voltage reference circuit was based on [15] and contains two 5-bit resistive DACs, one to tune the temperature coefficient and the other to adjust the output voltage. The nominal bandgap voltage was designed to be 650 mV when $V_{BAT}$ = 1.6 V with a simulated power consumption of around 1.8 mW at 27 °C. Simulations showed a PSRR of 58 dB at a frequency of 1 MHz.

The bandgap reference voltage was characterized (1) as a function of the input voltage by sweeping the bandgap supply from 0 V to 1.6 V and (2) as a function of the voltage control bits for the output voltage DAC, as shown in Figure 14. For a temperature control DAC code of `5b'10101` and a voltage control DAC code of `5b'01100`, we measured a bandgap reference voltage of 0.655 V that varied by less than 5 mV for an input voltage between 1 V to 1.6 V.

## Conclusion

We continue to make progress toward a next generation of crystal-free systems-on-chip with notable improvements from SCµM-V22 to SCµM-V23 in power consumption, system functionality, and the overall SoC feature set. Compared to previous generations of SCµM, SCµM-V has realized a higher performance RISC-V core, expanded on-chip memory, and a wider range of efficient power management options. However,

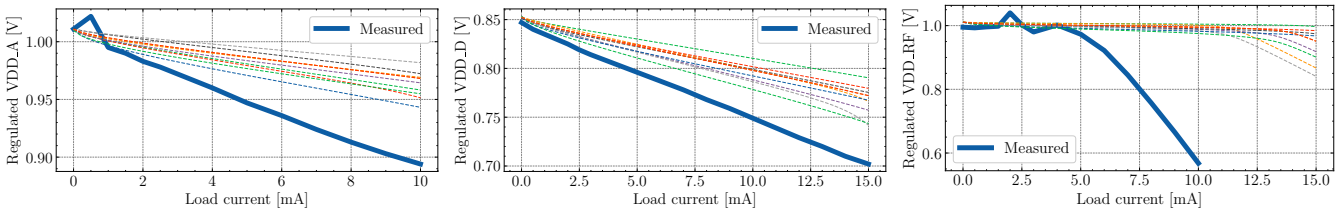


Fig. 12: Measured (bold) LDO regulated voltages for the analog LDO (left), digital LDO (center), and RF LDO (right) vs. simulated regulated voltages across all process corners (dashed).

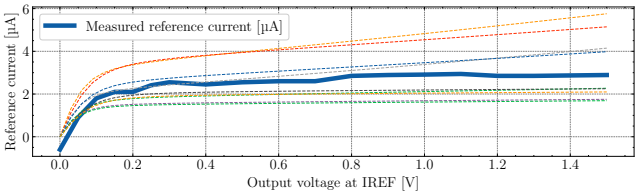


Fig. 13: Measured on-chip current reference (bold) vs. simulated reference current at all process corners (dashed).

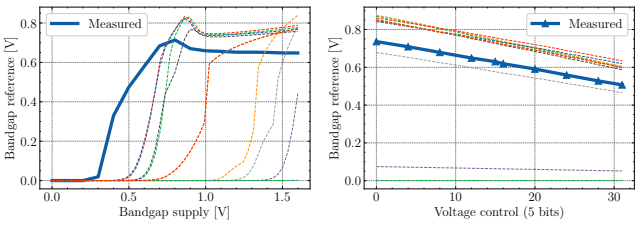


Fig. 14: Measured (bold) and simulated (dashed) bandgap reference voltage vs. the input voltage (left, voltage control = `5b'01100`) and vs. the 5-bit voltage control bits (right, supply voltage = 1.5 V).

SCµM-V23 lacks critical functionality in its on-chip radio and did not realize several other key specifications in its clock and power management systems.

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