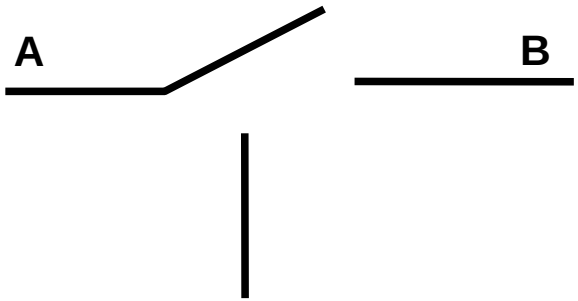
GC03
Logic gates and Transistors

Peter Rounce

p.rounce@cs.ucl.ac.uk

Electronic switch



Switch Control active - switch closed

Resistance between A and B is very small

Resistance ~ 0

Voltage at V = Voltage at B

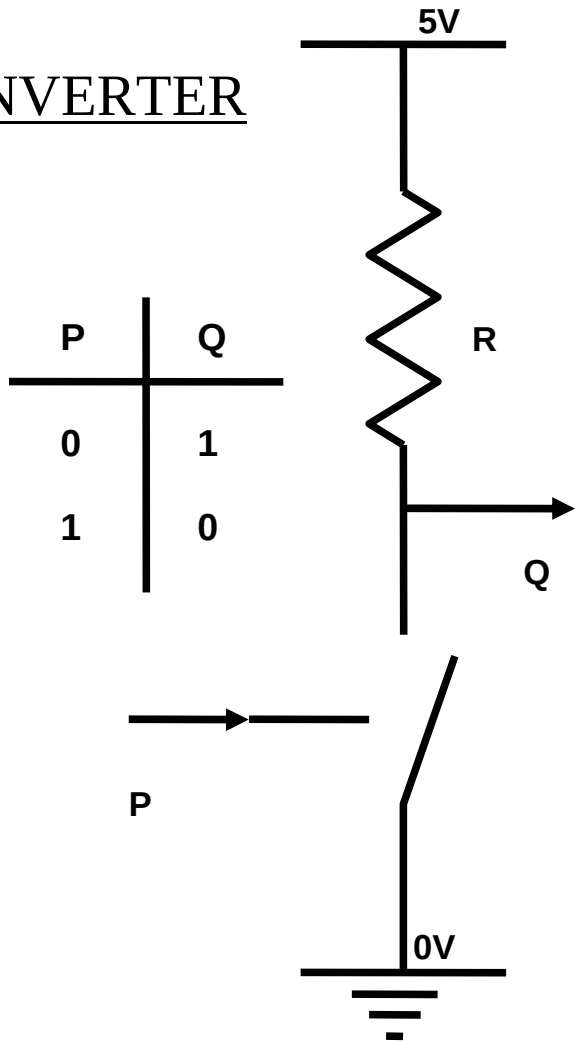
Switch Control inactive - switch open

Resistance between A and B is very large

Current cannot flow between A and B.

Voltage at A not related to voltage at B.

INVERTER



P	Q
0	1
1	0

If P is at '0', switch is open and Q is at '1'.

No current can flow through switch, and therefore there is no current through resistance.
Thus, Ohm's law (V = IR) gives a voltage drop of 0V (V=IR=0.R) across resistance
and since one side of switch is at 5V, Q must be at 5V.

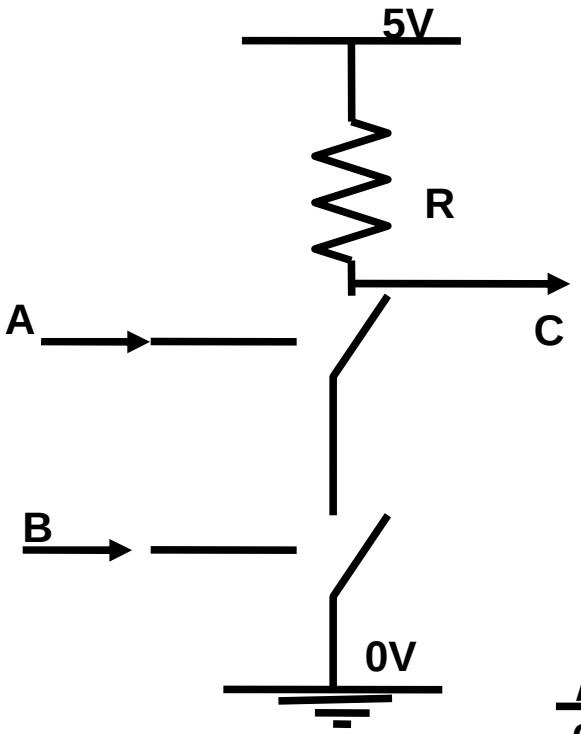
If P is at '1', switch is closed, and Q is at '0'.

There can be no voltage across switch, since R ~ 0 and one side of switch is connected to 0V.
All of voltage from power supply appears across R.
R just limits current flow and prevents a short circuit.

Let 5V on P close switch, and 0V open switch.
Let '1' represent 5V, and '0' represent 0V.

2-INPUT NAND

Let switches close when switch control is '1'.



When both switches are closed (A = B ='1'), current can flow through circuit and C is at 0V, since there is no voltage change between 0V and C.

When either switch is open (A = '0' or B = '0') no current can flow through R and C is at '1'.since now there is no voltage change between 5V & C.

$C = \overline{A.B}$

Truth Table

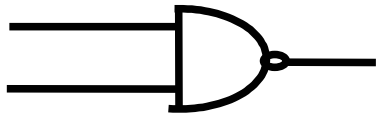
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

Truth table for nand

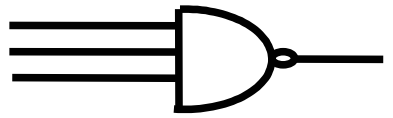
A	B	A.B	$\overline{A.B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Circuit symbol for

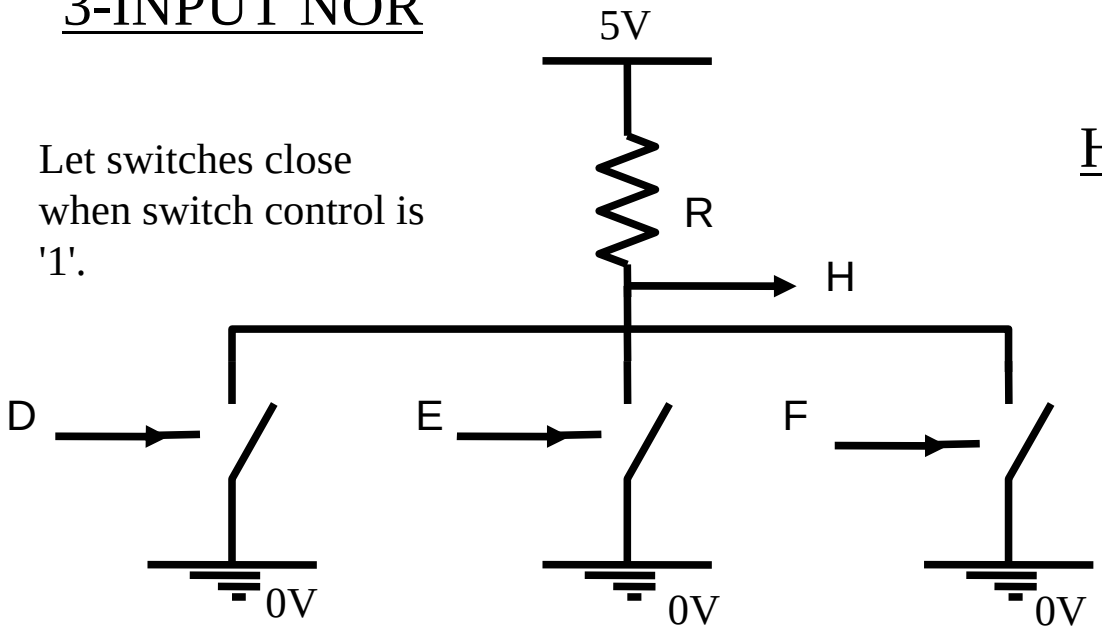
2-input nand



3-input nand



3-INPUT NOR



Let switches close when switch control is '1'.

$$\underline{H = \overline{D + E + F}}$$

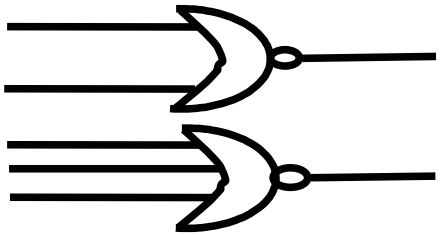
Truth Table

D	E	F	H
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

If D or E or F is'1', at least one switch is closed and a current flows through R and H is at '0'.

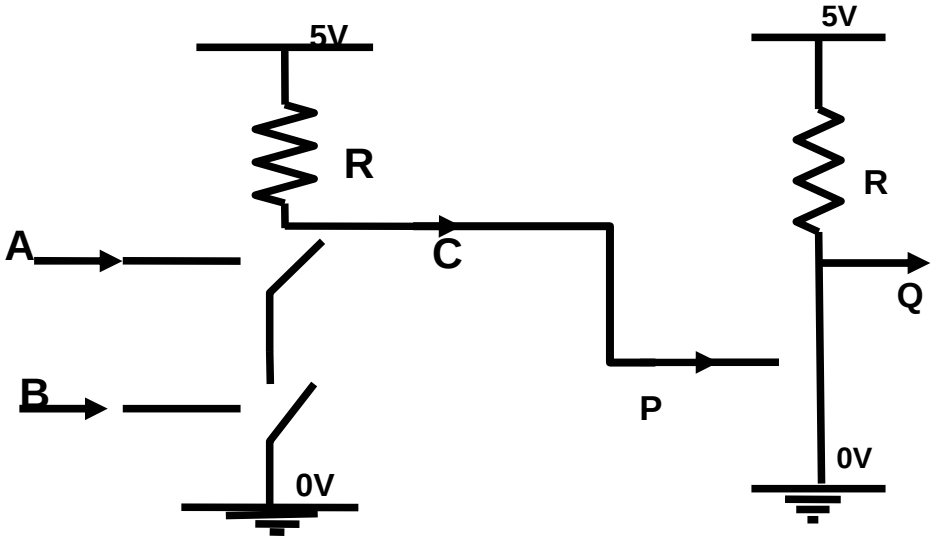
Only if D = E = F = '0' are all switches open and then no current flows through R, and H is '1'.

Circuit symbol for



Notes:

- The NAND, NOR, and NOT (inverter) circuits are most the basic logic gates.
- The form presented with the resistor between the switch and the positive power supply terminal is identical to NMOS transistor logic gates discussed later.
- Logically AND and OR logic gates could be built by placing the resistor between the switches and the negative power supply terminal. For electrical reasons, this cannot be done in NMOS transistor circuits, and AND and OR and other non-inverting circuits are built by inverting versions with the output passed through a NOT-gate, e.g.



AND circuit

Materials

Metals - an electron is released by each metal atom to form a free electron `soup'.
Applying an electric field across metal moves free electrons: a current flows.

Insulators - atoms in insulators keep all their electrons firmly attached.
No electron 'soup' is created,
and no current will flow in response to an applied electric field.

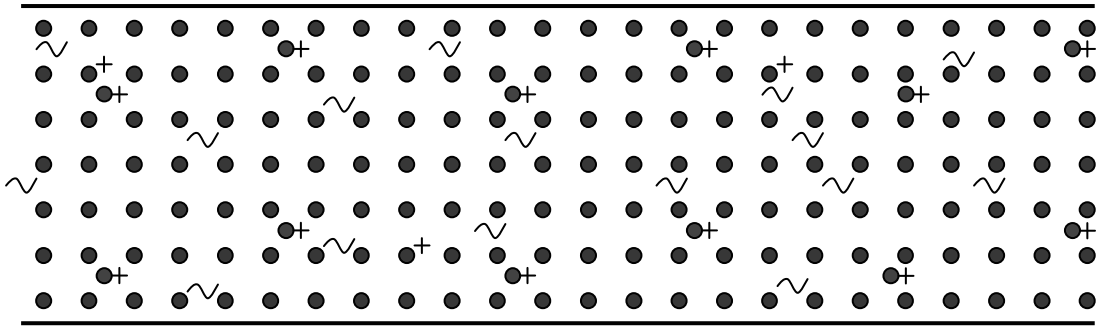
Semiconductors: these are normally weakly conducting when pure,
conduction can be increased by 'doping': adding other materials.

Silicon doped with phosphorus atoms produces an n-type material:
n-types semiconductors: electrons carry current.

Silicon doped with boron atoms produces a p-type material:
p-type semiconductors: 'holes' carry current.

N-type semiconductor, doped with Phosphorus

Section of a single silicon crystal

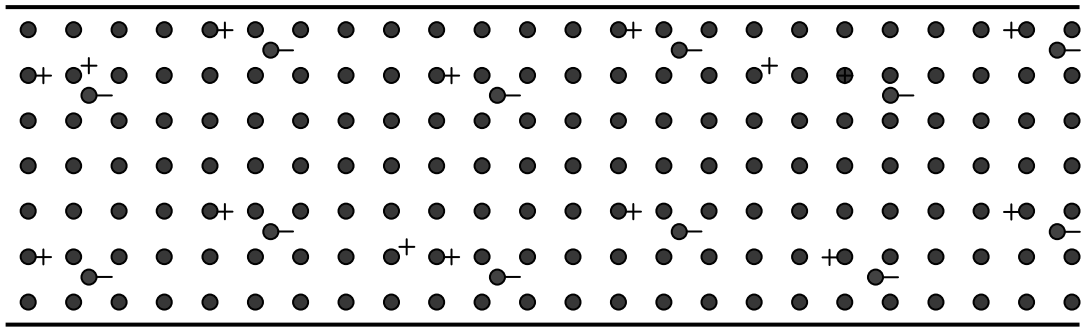


- Neutral silicon atom
- $^{+}$ Positively charged silicon atom which has released an electron into the material – only a tiny percentage of silicon atoms free an electron.
- ~ Free electron from silicon atom – number density low, ~10^{23} electrons/m^3
- phosphorus atom
- $^{+}$ Positively charged phosphorus atom has releases an electron into the material – each phosphorus atom frees an electron!
- ~ Free electron from phosphorus atom

Add 1% Phosphorus and get ~10^{27} electrons/m^3 - good conductor

P-type semiconductor, doped with Boron

Section of a single silicon crystal



- Neutral silicon atom
- $^{+}$ Positively charged silicon atom which has released an electron into the material – only a tiny percentage of silicon atoms free an electron.
- Boron atom
- $^{-}$ negatively charged boron atom has grabbed a free electron or an electron from a neighbouring silicon atom.

  Each boron atom grabs one electron, creating a large number of positively charged silicon atoms. No free electrons left. Current is carried by holes – each positively charged silicon atom is a ‘hole’: hole moves by grabbing an electron from a neighbouring neutral silicon atom.

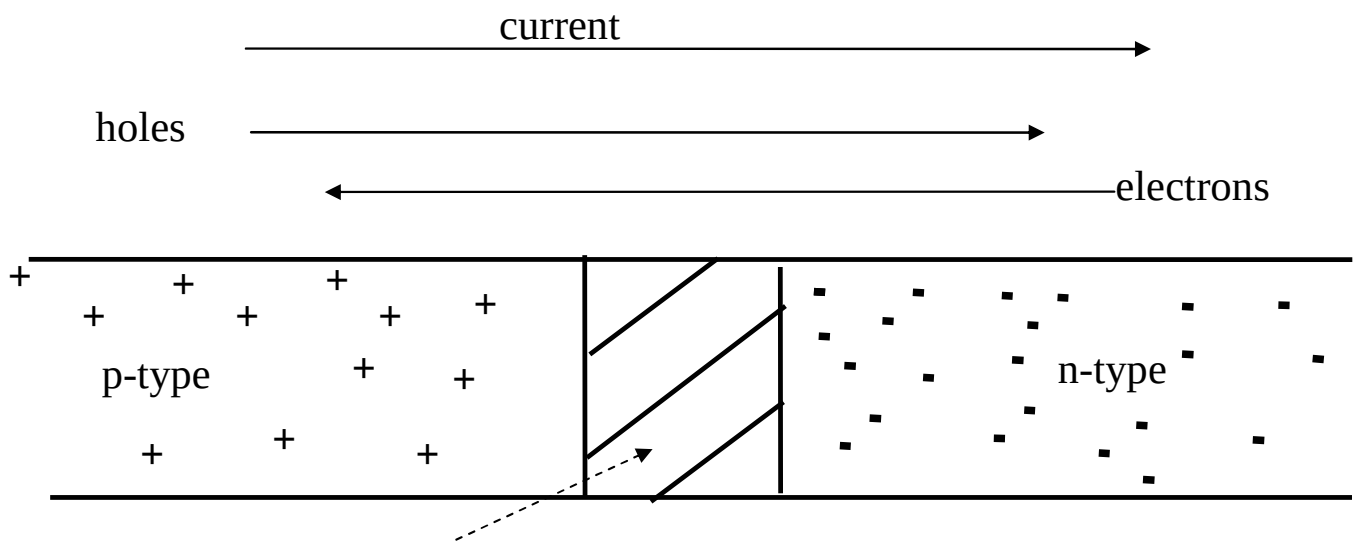
Add 1% Boron and get ~10^{27} holes/m^3 - good conductor

Silicon Diode:

Allows current flow in only one direction!

Electrons can be made to flow from n-type to p-type where they combine with holes, while holes can move from p-type to n-type where they combine with electrons: this will only happen if p-type region is more positive than n-type.

It is very difficult to make electrons and holes flow the other way.

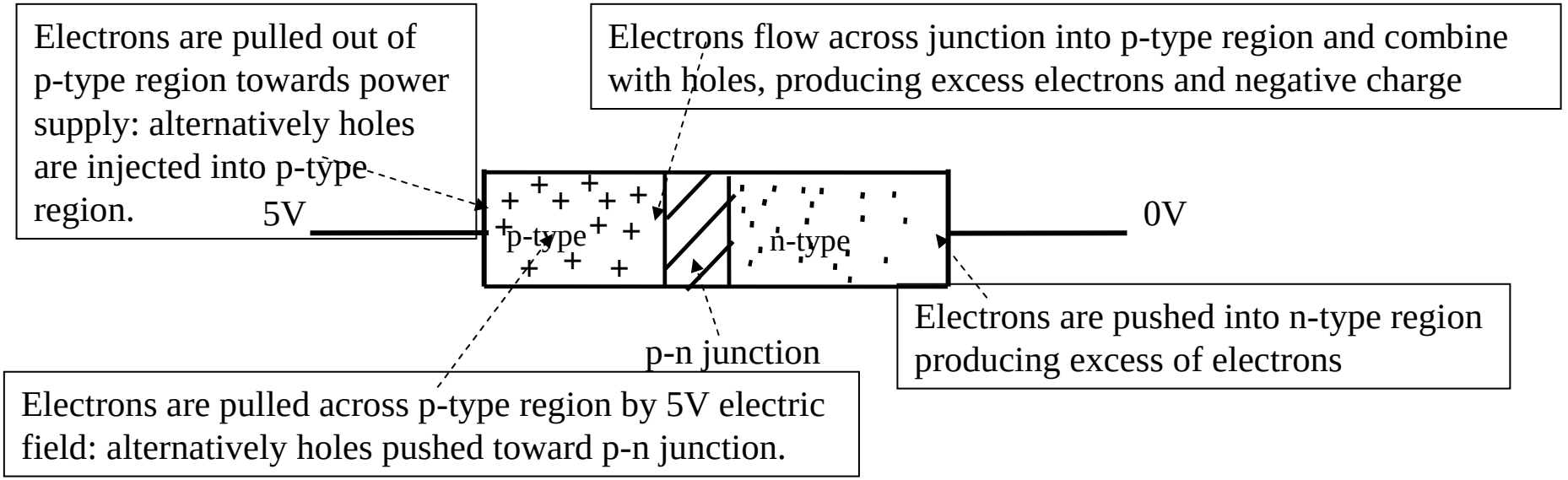


Region of overlap – material moves from p-type on left side to n-type on the right side of the junction

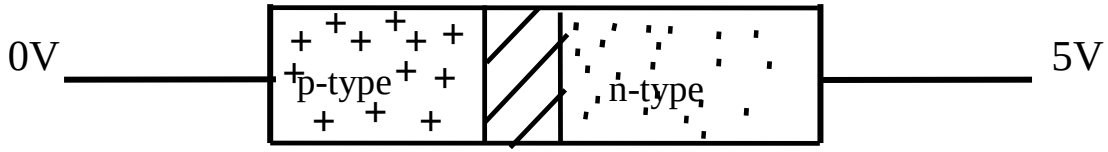
p-n junction

p-n junction has quantum mechanical properties that mean electrons can only flow as shown.

Forward-biased p-n junction: p-type more positive than n-type



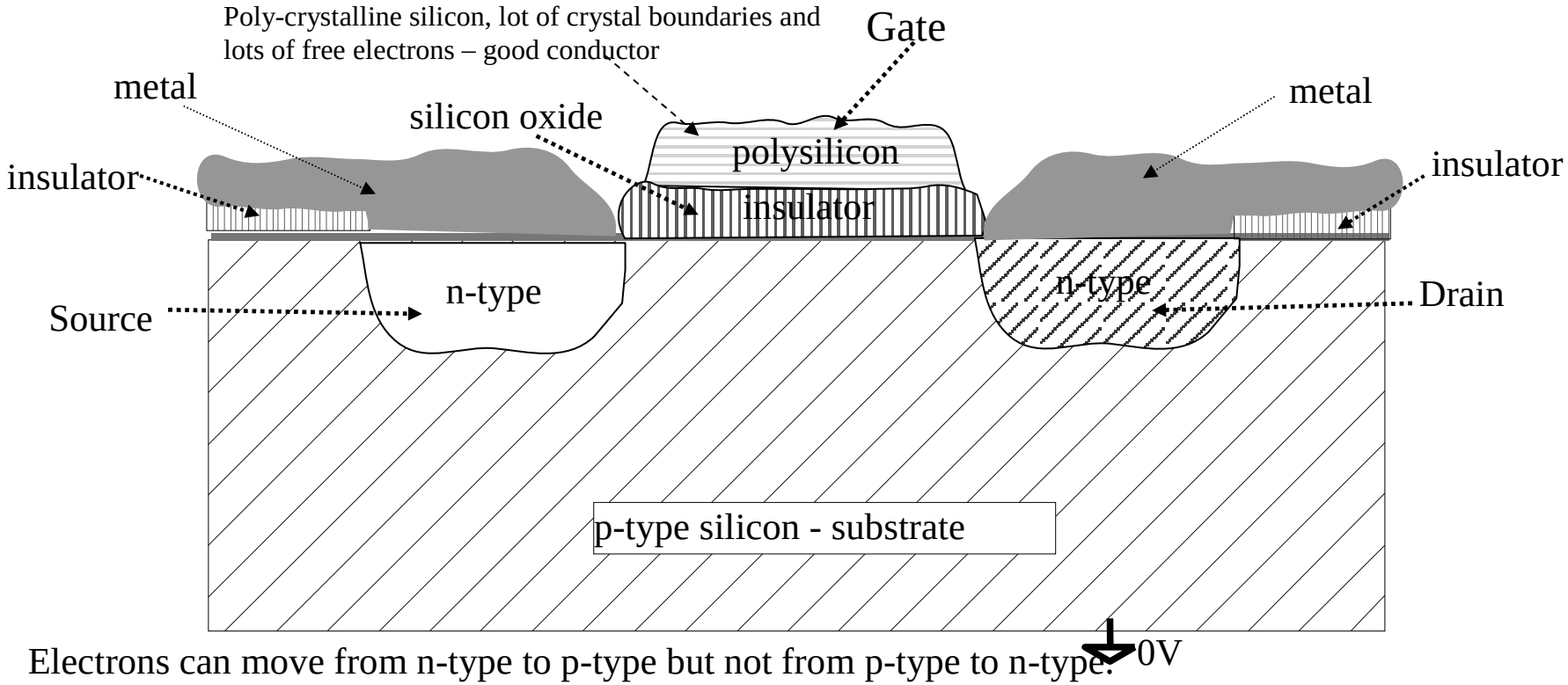
Reverse-biased p-n junction: n-type more positive than p-type



p-n junction

No current flow! No simple explanation! Need quantum mechanics. Basically need to move electrons from p-type region to n-type region, but there is large energy barrier to movement.

METAL-OXIDE-SILICON (MOS) n-p-n transistor. (n-transistor)

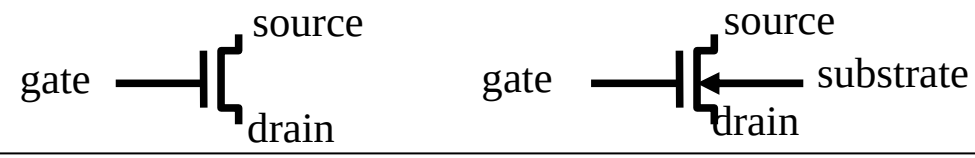


Electrons can move from n-type to p-type but not from p-type to n-type.

Thus would not expect current to flow from source to drain or drain to source.

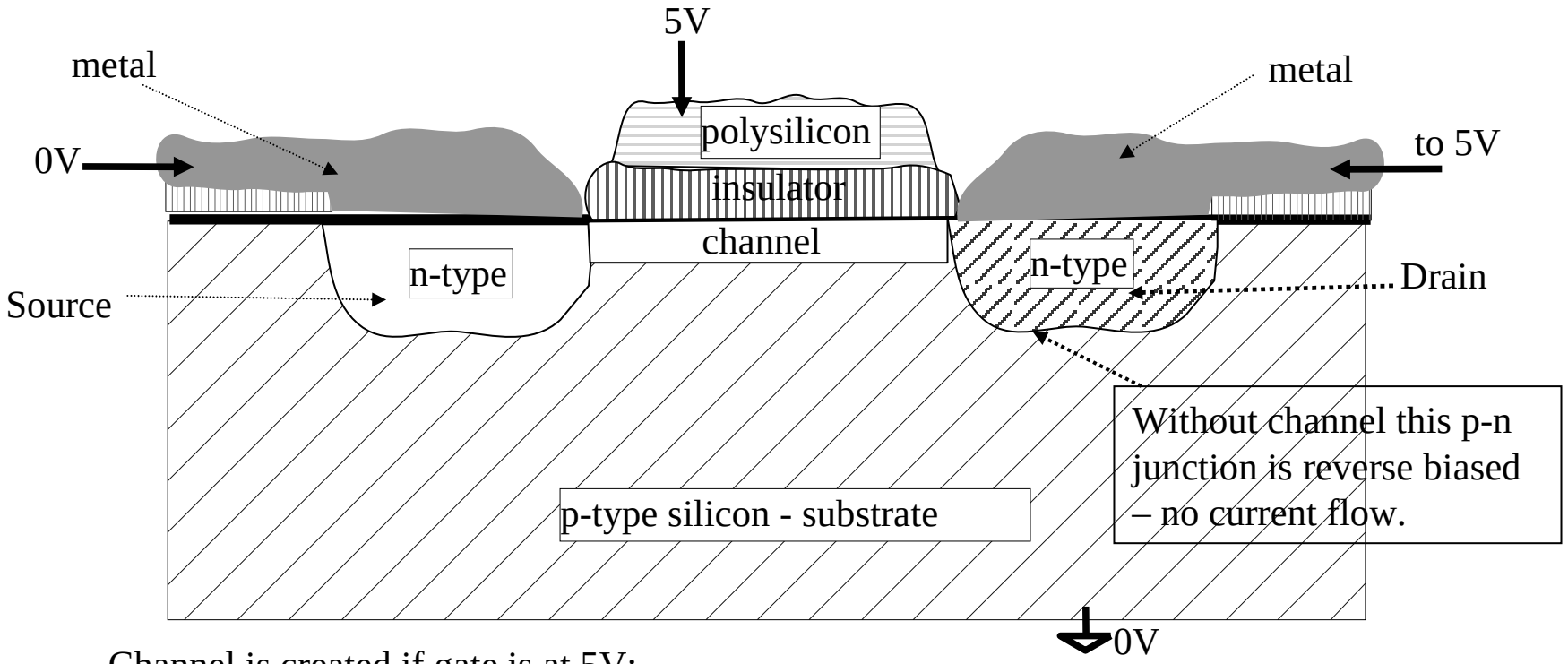
Current will flow if can make n-type region (the channel) between source/drain.

Symbols for an n-transistor :-



substrate is ~1000 microns deep / n-type diffusions are 0.2- 1 microns deep/ (1 millimetre = 1000 microns)

METAL-OXIDE-SILICON (MOS) n-p-n transistor.

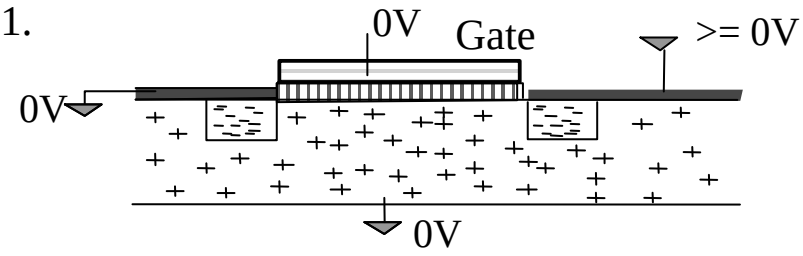


Channel is created if gate is at 5V:
electric field pulls electrons out of left-hand n-type into the region under the insulator, making channel region n-type. Current can now flow between source and drain - 'switch' closed.

When the gate is at 0V, there is no electric field across insulator to hold extra electrons in the Channel region and the Channel disappears:
current can no longer flow - channel region is now p-type - 'switch' open.

Operation of n-p-n transistor (n-channel or n-transistor)

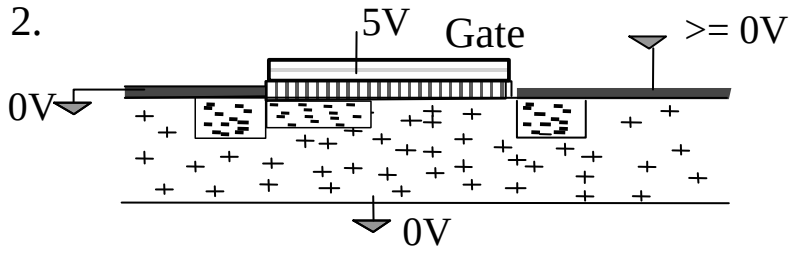
1.



Offstate of device with Gate at 0V.
No electrons flow between left n-region into substrate across p-n junction, because both sides of junction are at 0V.

No electrons flow between right n-region and substrate because p-n junction is *reversed biased*:
voltage on n-region is either same or greater than substrate - a voltage lower than substrate is needed on n-region to get electrons out of it into p-region.

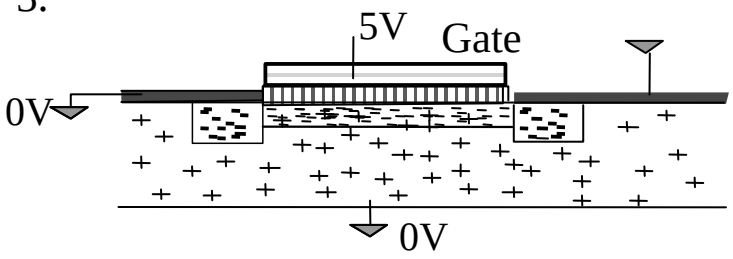
2.



When Gate is put to 5V, the electric field effectively puts 5V on the substrate below the gate. This voltage pulls electrons from the left n-region to create a n-type channel.
(channel is partially formed in this diagram)

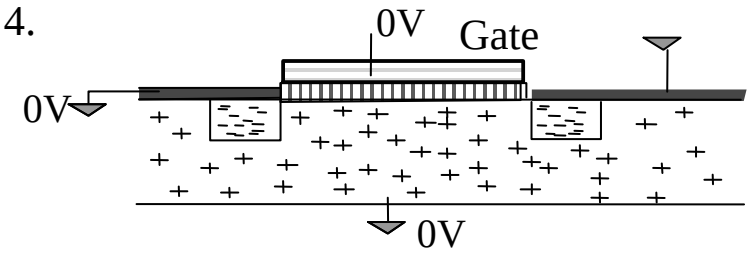
Operation of n-p-n transistor (n-channel or n-transistor)

3.



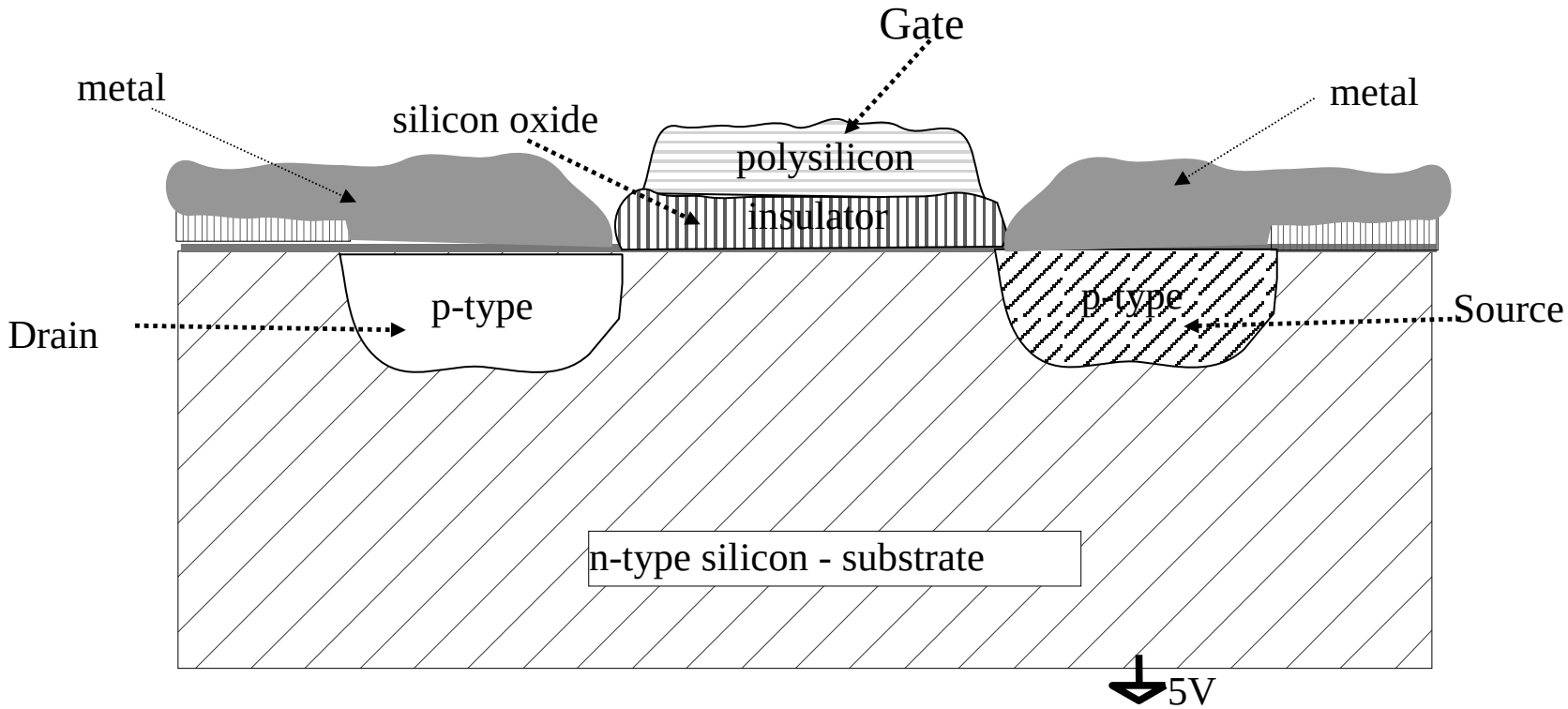
Eventually (~100ps) the n-type channel reaches the right n-region, and the electrons in the channel screen the substrate from the electric field.
The voltage in the channel is 0V.
At this stage, electrons can flow through the channel.

4.



When the gate is put back to 0V, the n-channel with its excess electrons appears to be at less than 0V (due to excess negative charge), and the greater voltage (0V) on the n-regions and substrate attracts the electrons and the channel disappears.

METAL-OXIDE-SILICON (MOS) p-n-p transistor. (p-transistor)



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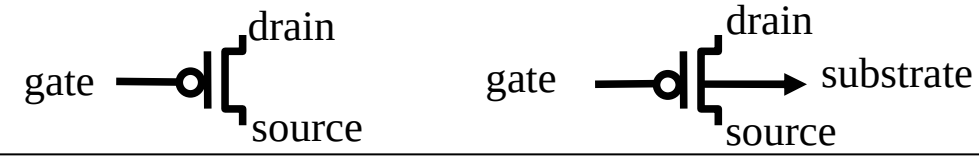

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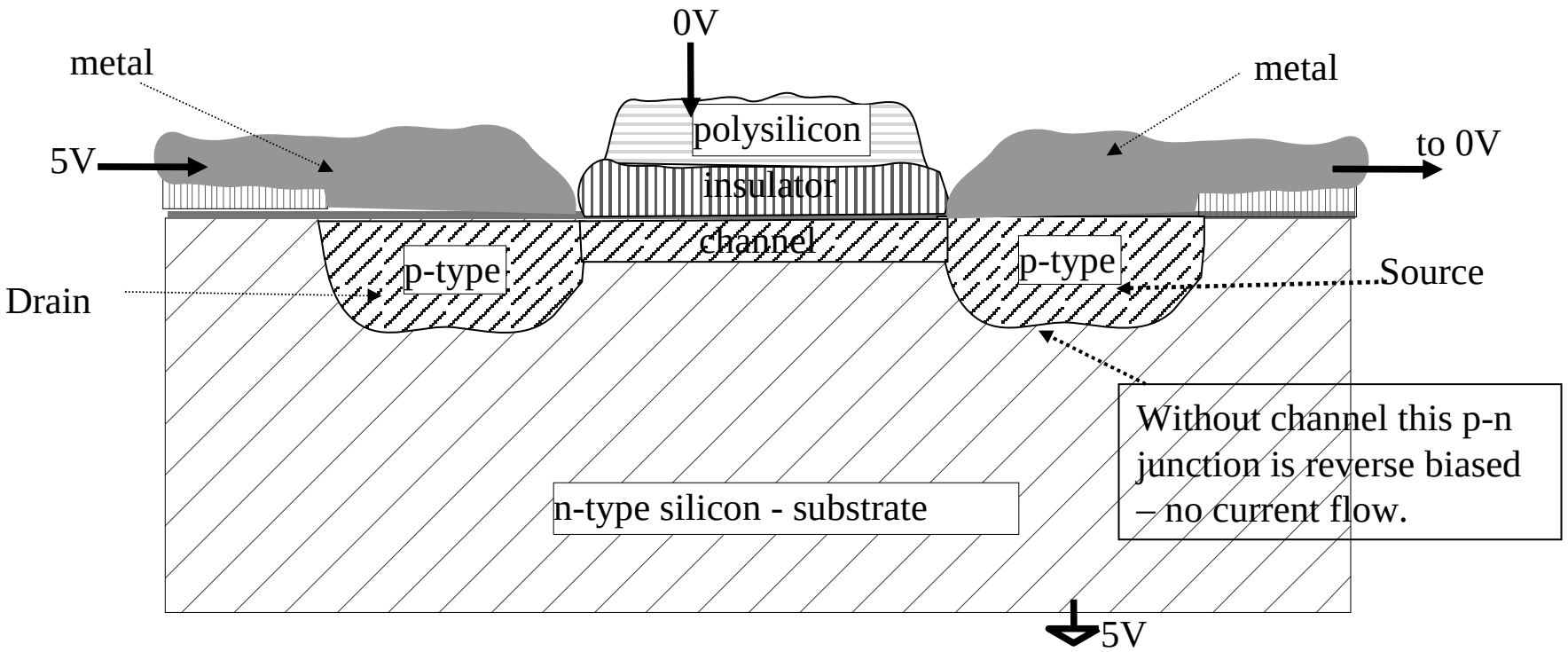
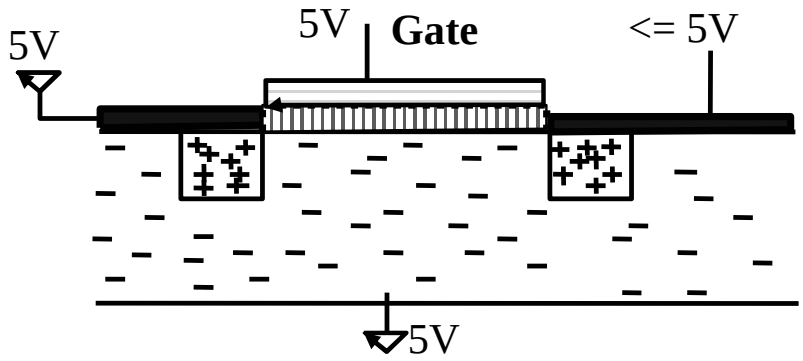


Channel is created if gate is at 0V:
electric field pulls holes into the region next to the insulator, making channel region p-type. Current can now flow between source/drain - 'switch' closed.

When the gate is at 5V, there is no electric field across insulator to hold extra holes in the Channel region and the Channel disappears:
current can no longer flow - channel region is now n-type - 'switch' open.

Operation of p-n-p transistor (p-channel or p-transistor)



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No electrons flow into left p-region from substrate across p-n junction because both sides of junction are at 5V.

No electrons flow between right p-region and substrate because p-n junction is *reversed biased*:
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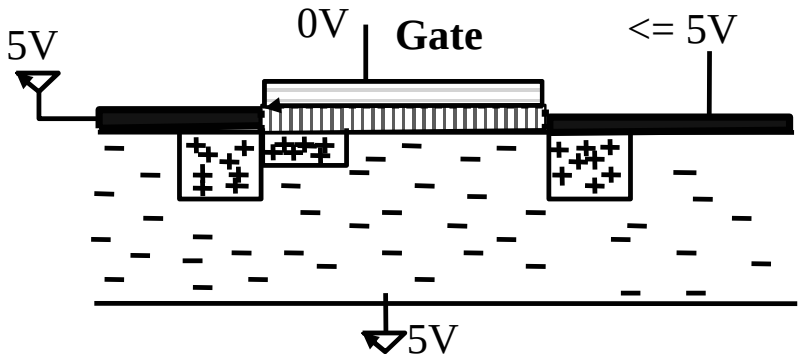
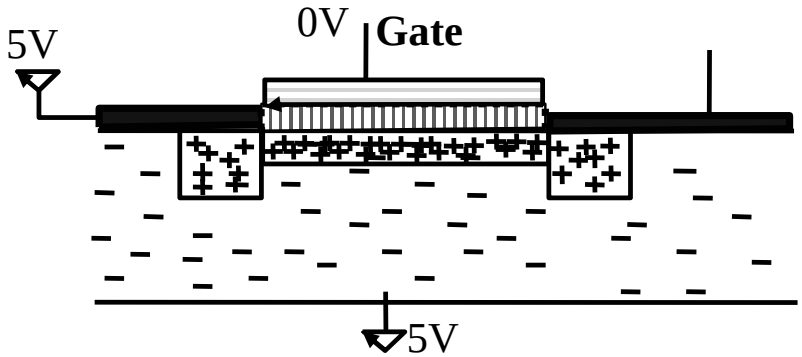


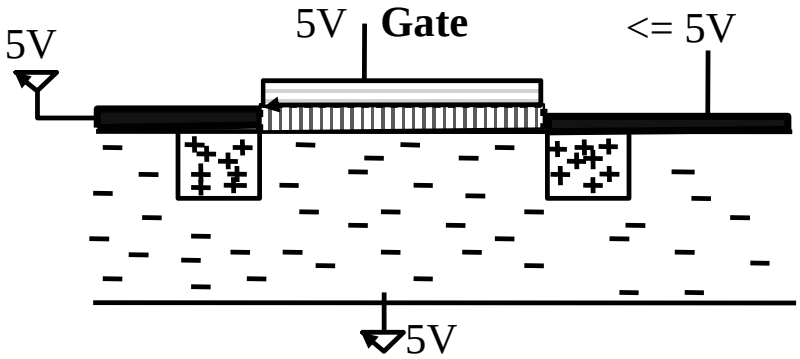
When Gate is put to 0V, the electric field effectively puts 0V on the substrate below the gate. This voltage pulls holes from the left p-region to create a p-type channel, i.e. electrons are pulled out of the channel into the left p-region. (channel is partially formed in this diagram)

Operation of p-n-p transistor (p-channel or p-transistor)



Eventually (~500ps) the p-type channel reaches the right p-region, and the lack of electrons in the channel screens the substrate from the electric field.
The voltage in the channel is 5V.

At this stage, any voltage on the right p-region lower than 5V will pull holes through the channel from the left p-region, i.e. electrons flow in the opposite direction.

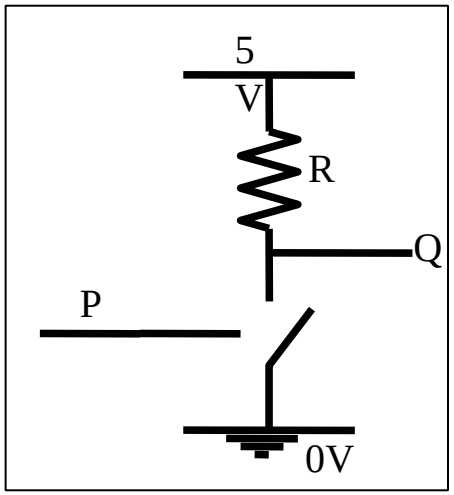


When the gate is put back to 5V, instantaneously the p-channel with its lack of electrons appears to be at greater than 5V (due to excess positive charge), and this will attract electrons from the p-regions and substrate and the channel disappears.

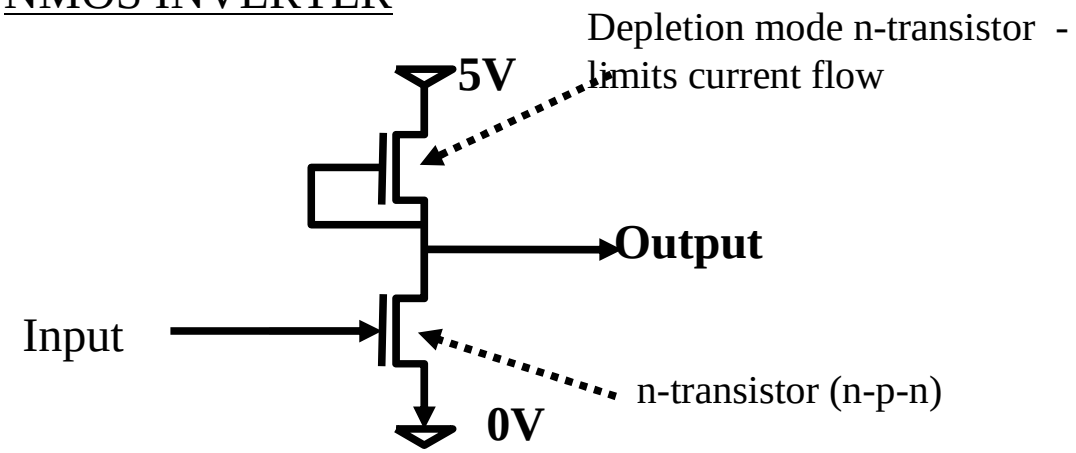
NMOS Logic

This consists of only n-transistors (n-p-n) :
transistor conducts when gate is at 5V
transistors is not-conducting when gate is at 0V

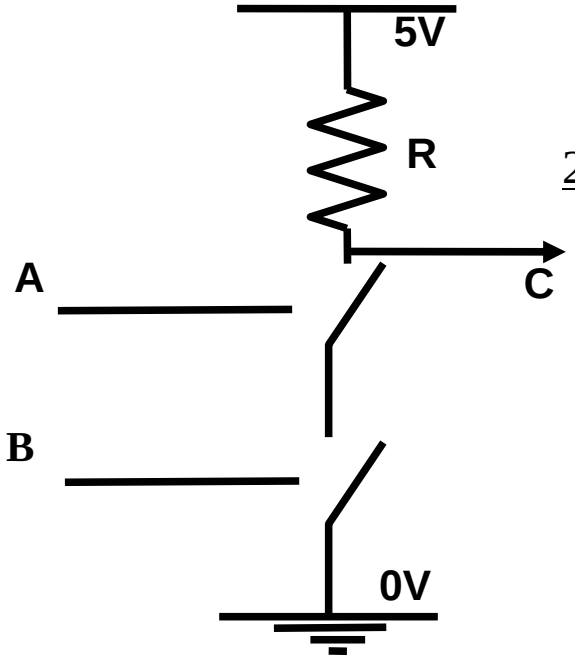
Inverters, nand and nor gates can be made in the same way as our electronic switch circuits except that, since simple resistors take up very large areas, special weakly-conducting transistors are used.
These have the same function as resistors: they limit the current flow when the circuit outputs a '0'.



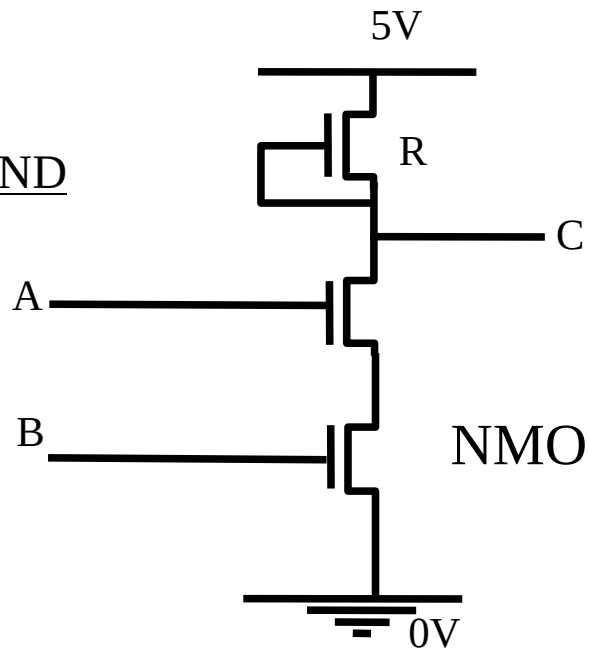
NMOS INVERTER

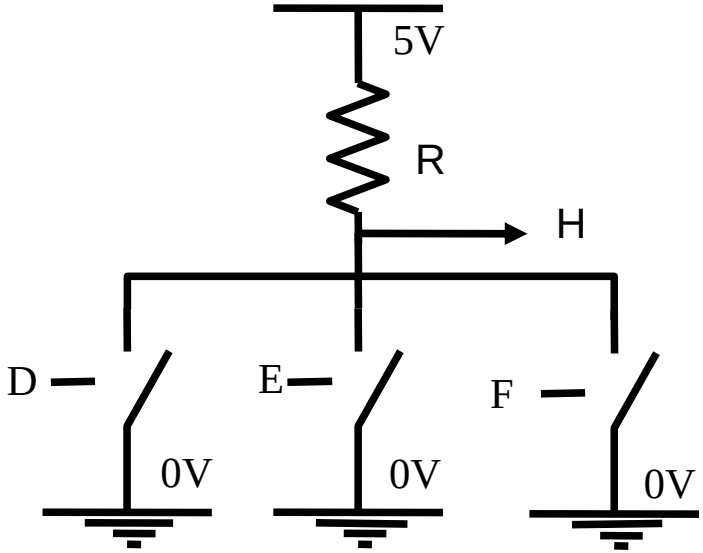


While lower transistor is conducting, current flows and power consumed . It takes longer to go from '0' to '1' than from '1' to '0', because better conductivity from 0V to output across switch than across resistor from output to 5V.

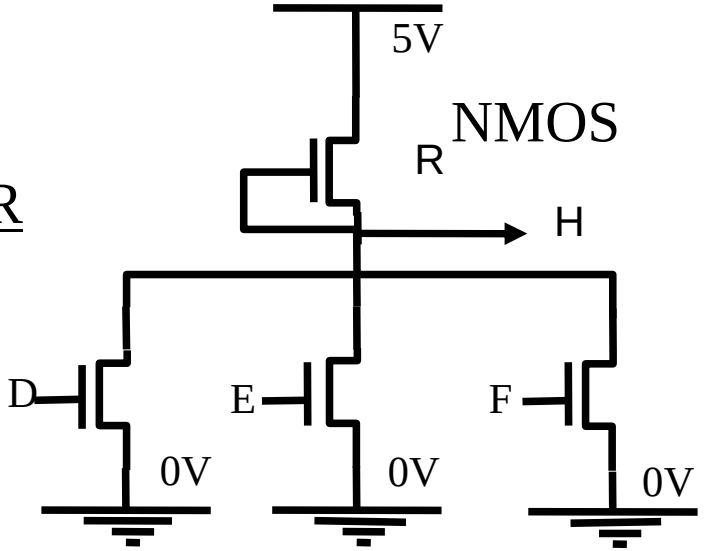


2-INPUT NAND





3-INPUT NOR



Problems of NMOS logic:-

1) When output voltage is 0V, there is a circuit through the logic gate from the 0V to the 5V power supply terminals and power is consumed. Need to keep resistance from output connection to 5V power supply high during this time to limit power consumption.

2) Asymmetric switching times when output voltage changes:-

A change of output from 5V to 0V occurs when a good conducting pathway through the transistors is made. Electrons move quickly across this pathway rapidly bringing the output to 0V.

A change of output from 0V to 5V occurs when the pathway through the transistors is broken. Electrons are pulled more slowly through the resistor out of the output wire and the output voltage increases more slowly to 5V than when it falls to 0V. Need low resistance to 5V power supply terminal to decrease switching time – opposite of requirement in (1).

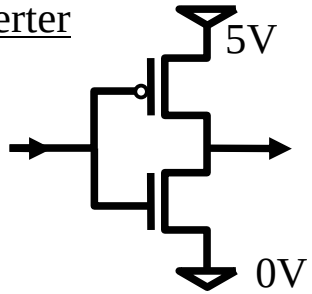
The slow 'rise' time from 0V to 5V reduces the speed of operation of the logic. When a change occurs in the output of a logic gate, this change will propagate through a series of other gates. The time it takes for this sequence of changes to complete is determined by the rise and fall times of the output signals. The slower rise time of the output voltage of NMOS gates from 0V to 5V reduces the operational speed of these circuits.

The depletion mode transistor is a standard n-p-n transistor except that the channel region is made weakly p-type, so that it always poorly conducts. While the gate is at 0V, the channel acts as a resistor, limiting the current flow and the power consumption. When the output connection switches from 0V to 5V, the gate voltage will rise as the output voltage rises, and the channel will at some point become a good conducting pathway, decreasing the 0V to 5V switching time.

CMOS Logic - Complimentary MOS

Uses both n-p-n and p-n-p transistors

Inverter



Either upper p transistor is conduction or lower n-type, but not both: 'complimentary' operation

When input is 5V, there is path from 0V through the n-transistor to output

When input is 0V, there is a path from 5V through the p-transistor to output

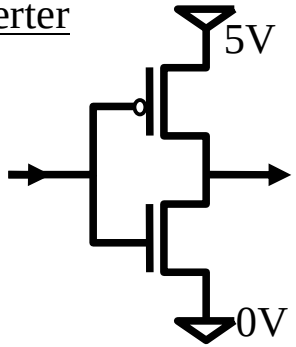
In steady state, the output is connected either to 0V or to 5V by conducting transistors, but not to both.
This is complimentary action.
There is never a good conducting path from 5V to 0V, i.e. a short-circuit condition never exists.
There is also no steady-state current through the transistors.

The output rise and fall times can be made the same, as there is no resistive element!

You can consider that the input signal determines which power supply terminal, 0V or 5V, is connected to the output connection!

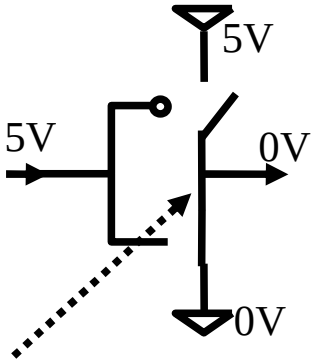
CMOS Logic - Complimentary MOS

Inverter



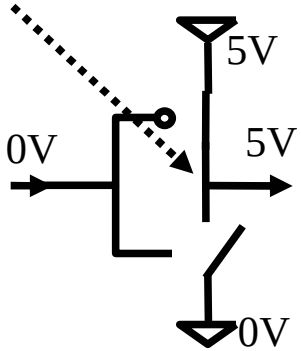
Uses both n-p-n and p-n-p transistors

Either upper p transistor is conduction or lower n-type, but not both: 'complimentary' operation



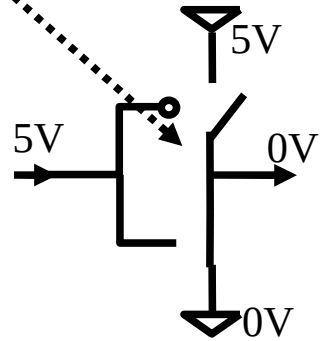
Excess electrons at output make output 0V

Excess +ve charge at output make output 5V



Excess electrons went to 5V supply terminal

Excess electrons at output make output 0V



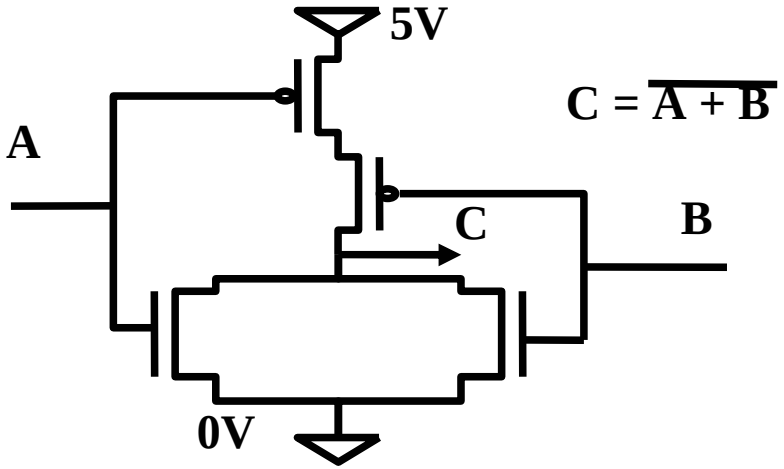
Excess electrons come from 0V supply terminal

As circuit switches, electrons move first from 0V supply to gate output and second from gate output to 5V supply.

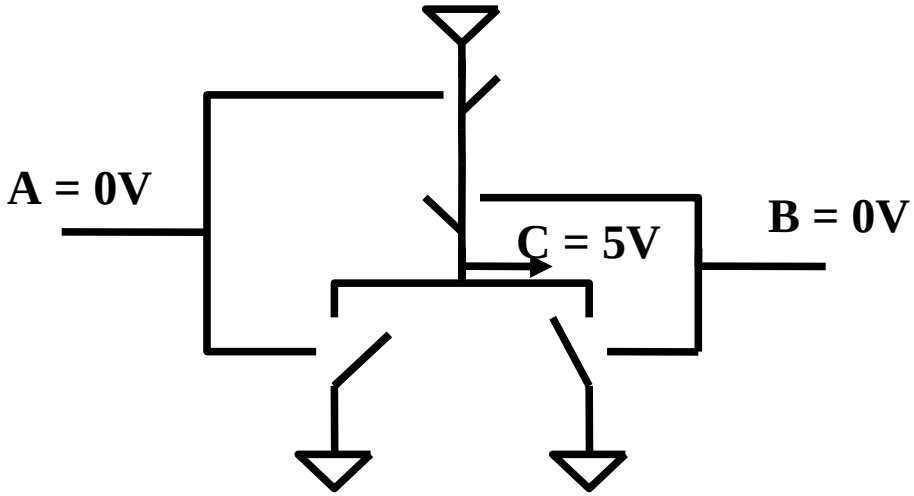
On each output cycle (0 → 1 → 0 →), a bunch of electrons move from 0V to 5V and power is consumed from the power supply. Therefore power is consumed only when circuit switching. These are low power circuits, power increases with operating frequency. If stop switching output voltage, negligible power consumption.

CMOS switches output very fast in both directions, because good conducting paths to 0V and 5V.

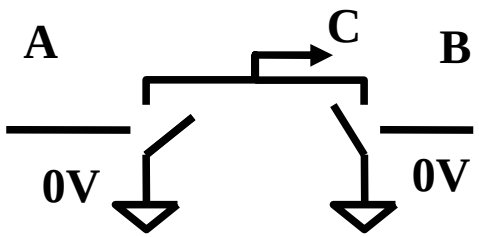
2-Input NOR gate in CMOS



'Switch' Model with A = B = 0V



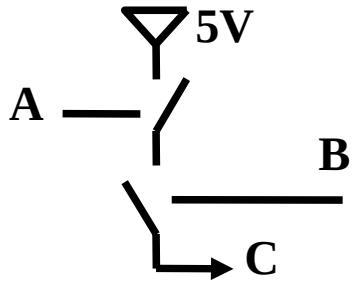
Bottom section of circuit generates zero outputs



$C = \overline{A + B}$

These 2 equations are the same by deMorgan's

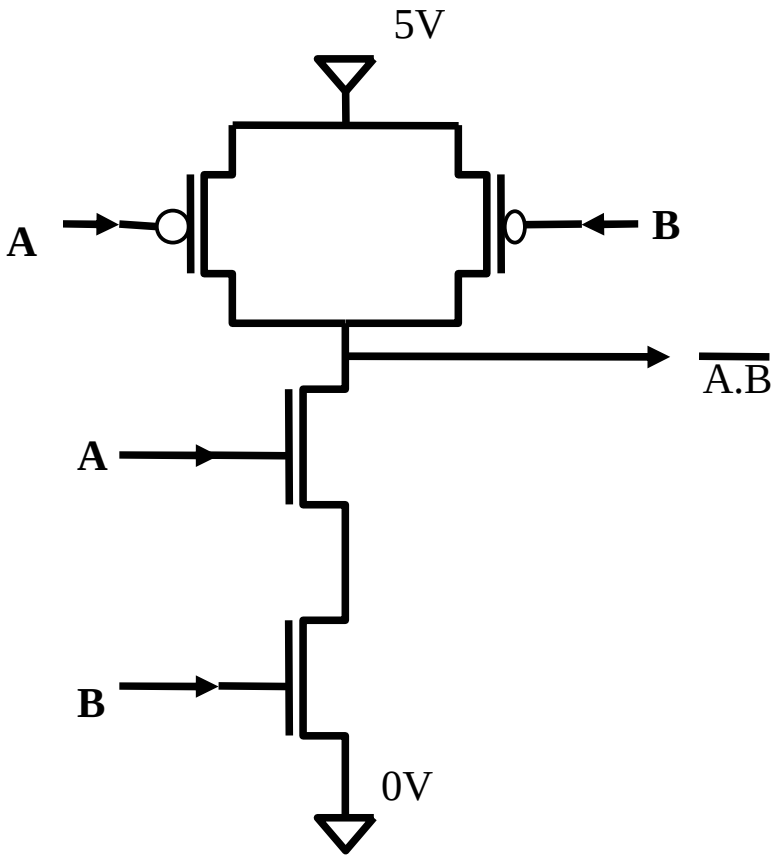
Top section of circuit generates 5V outputs



$C = \overline{A} . \overline{B}$

Top section generates 1s in truth table; bottom section generates 0s

2-input NAND

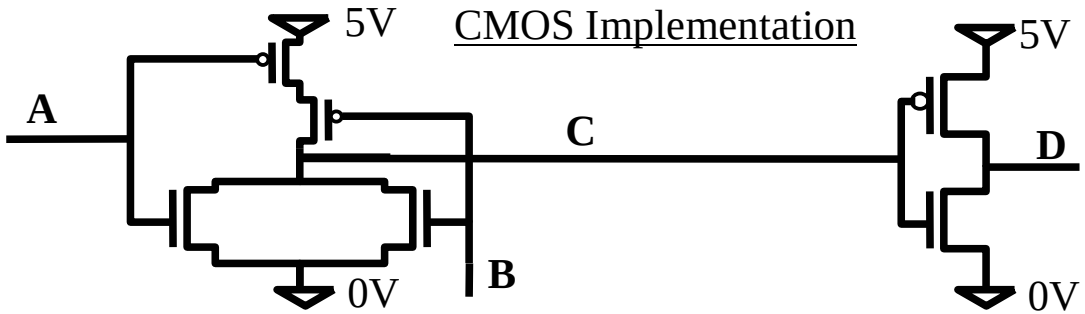


Only when both A & B are 5V, is there path through n-types to output

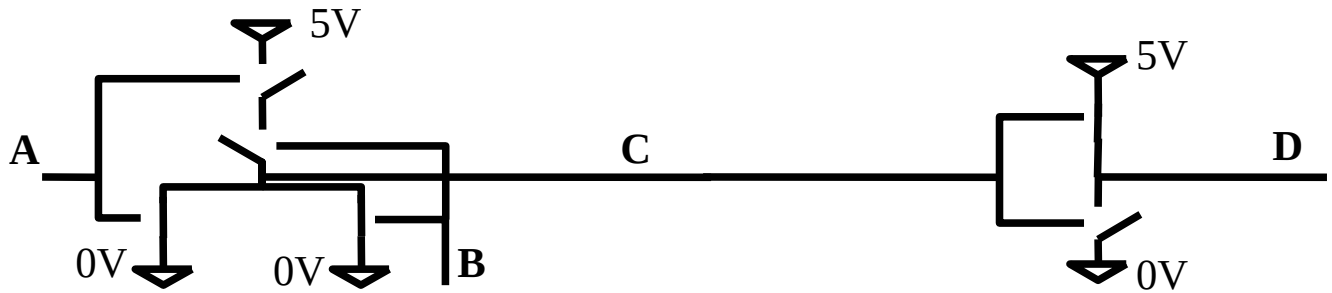
When either A or B is 0V, there is a path to 5v but no path to 0V.

2-INPUT OR circuit from 2-INPUT NOR and INVERTOR

CMOS Implementation



Switch' representation for A = B = 5V

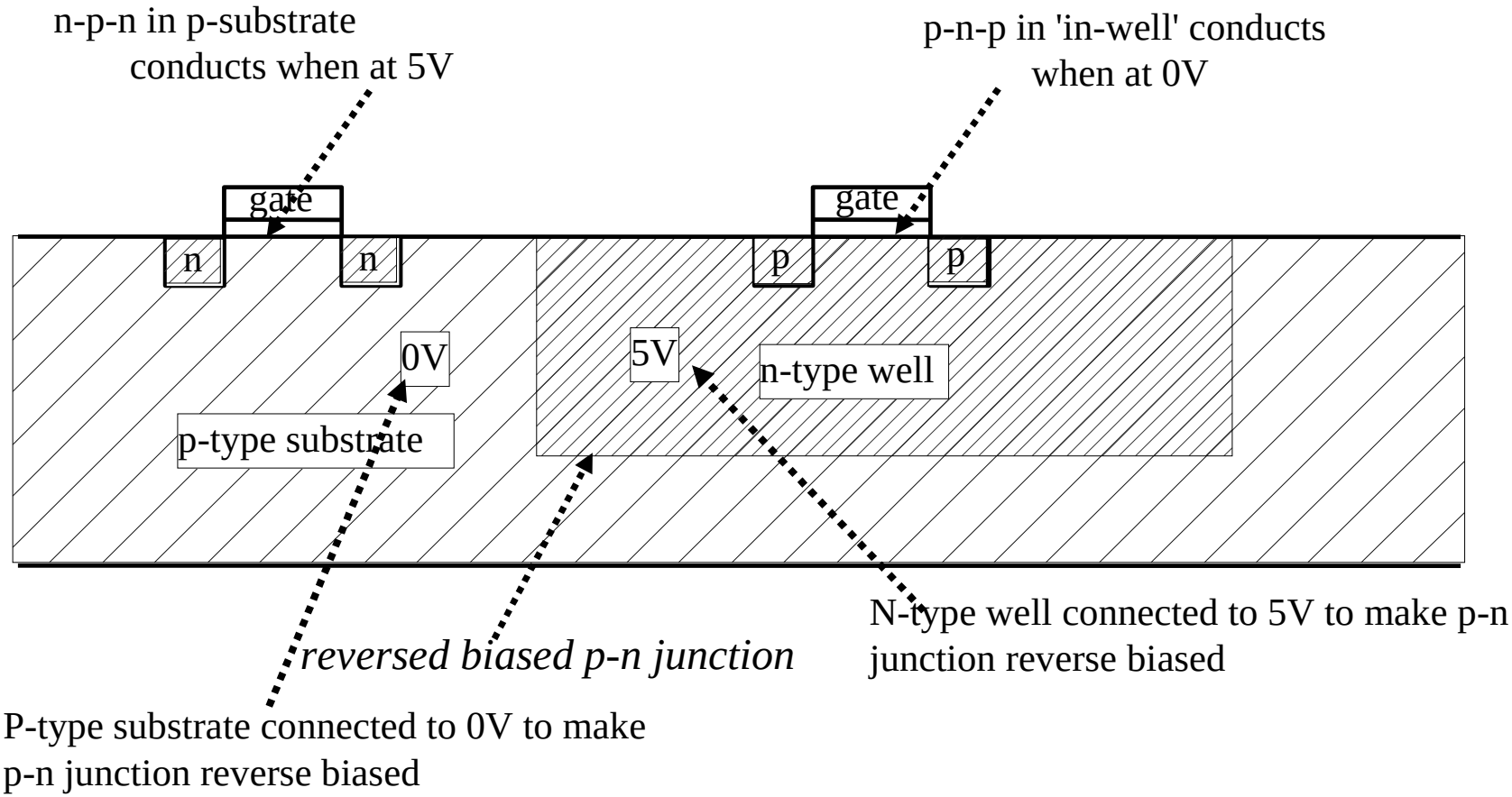


Note: There is no conducting pathway between the NOR circuit and the transistors of the INVERTOR along the output wire C. C affects the operation of the transistors of the INVERTOR by means of the electric field of the voltage on C across the gate insulator: no continuous current flows along wire C at any time: get only transient current flows when voltage changes.

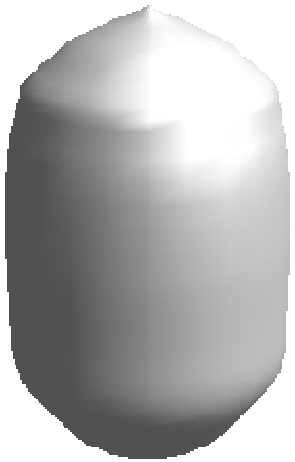
CMOS Logic - Complimentary MOS

CMOS uses both type of transistor (n-p-n) and (p-n-p) on same substrate.

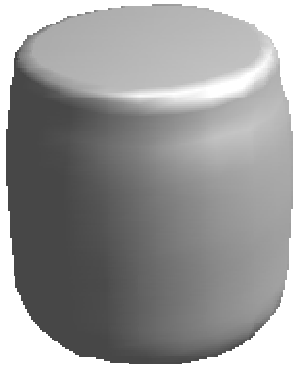
How ? By building an n-type well in p-type substrate.



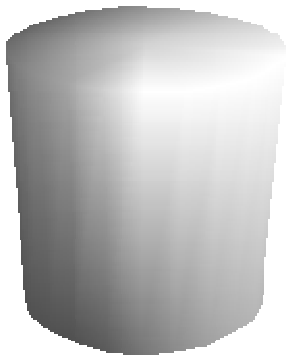
Wafer production



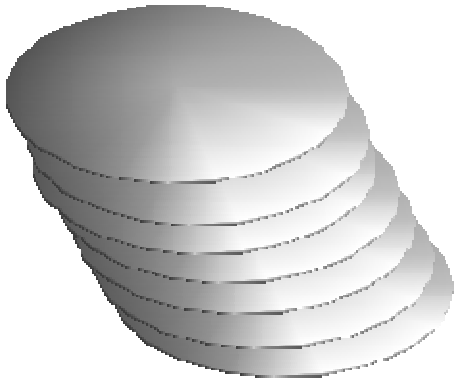
Large single crystal grown



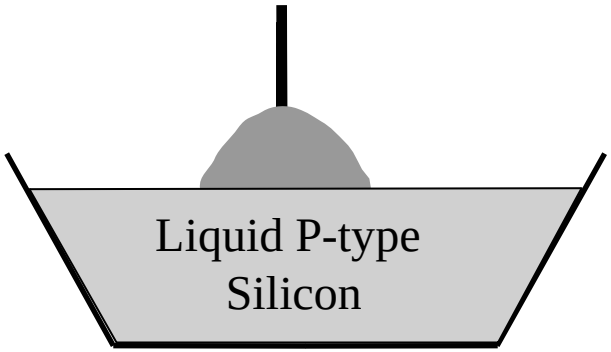
Cut to cylinder shape.....



... and sliced into wafers

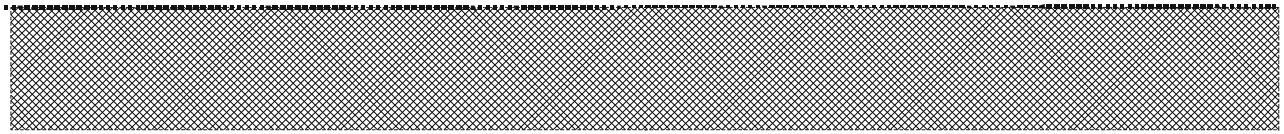


12 or 20 cm diameter wafers

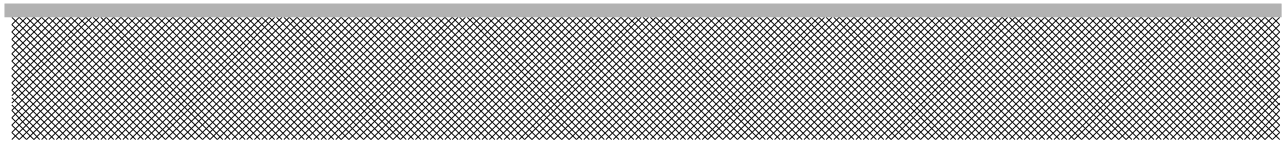


Vat of p-type silicon held at melting point. Rod tipped with tiny crystal of silicon touched against surface of liquid. Crystal grows and rod is lifted, producing large crystal – 20cms across.

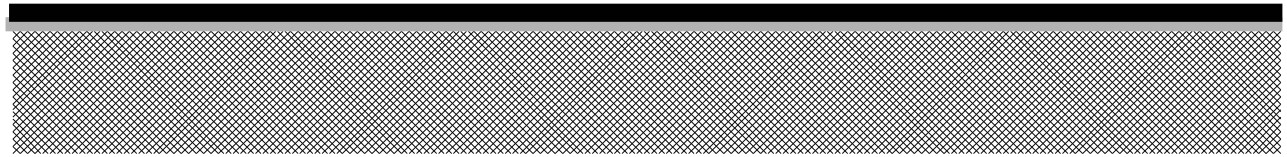
Surface of p-type wafer



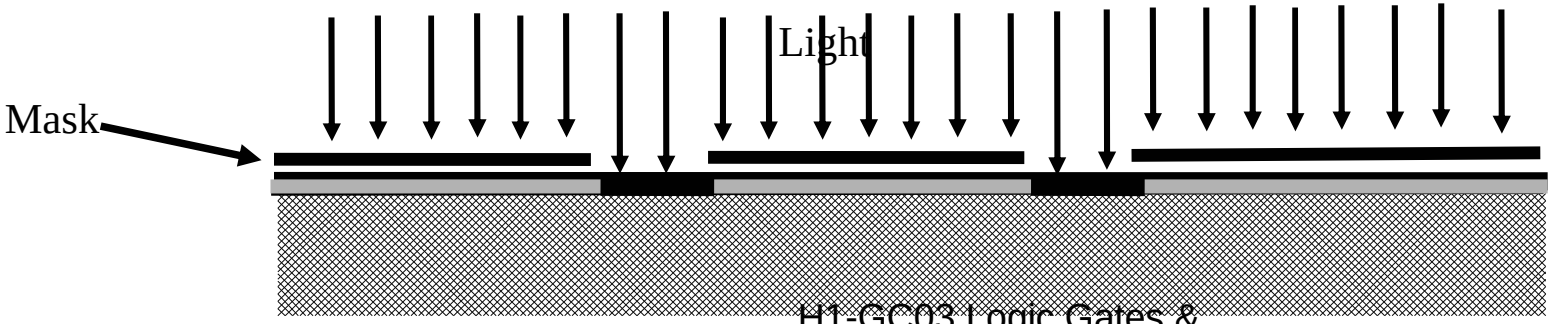
Surface exposed to oxygen - Silicon Oxide Layer forms on surface



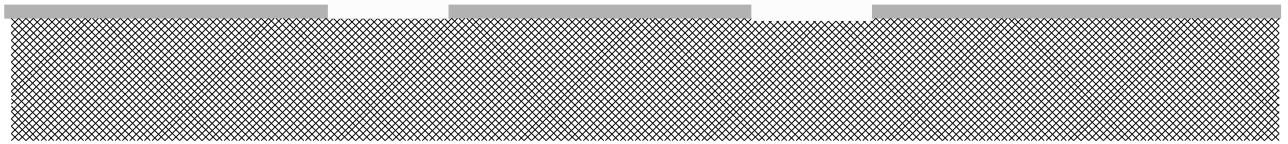
Surface coated with photo-sensitive material

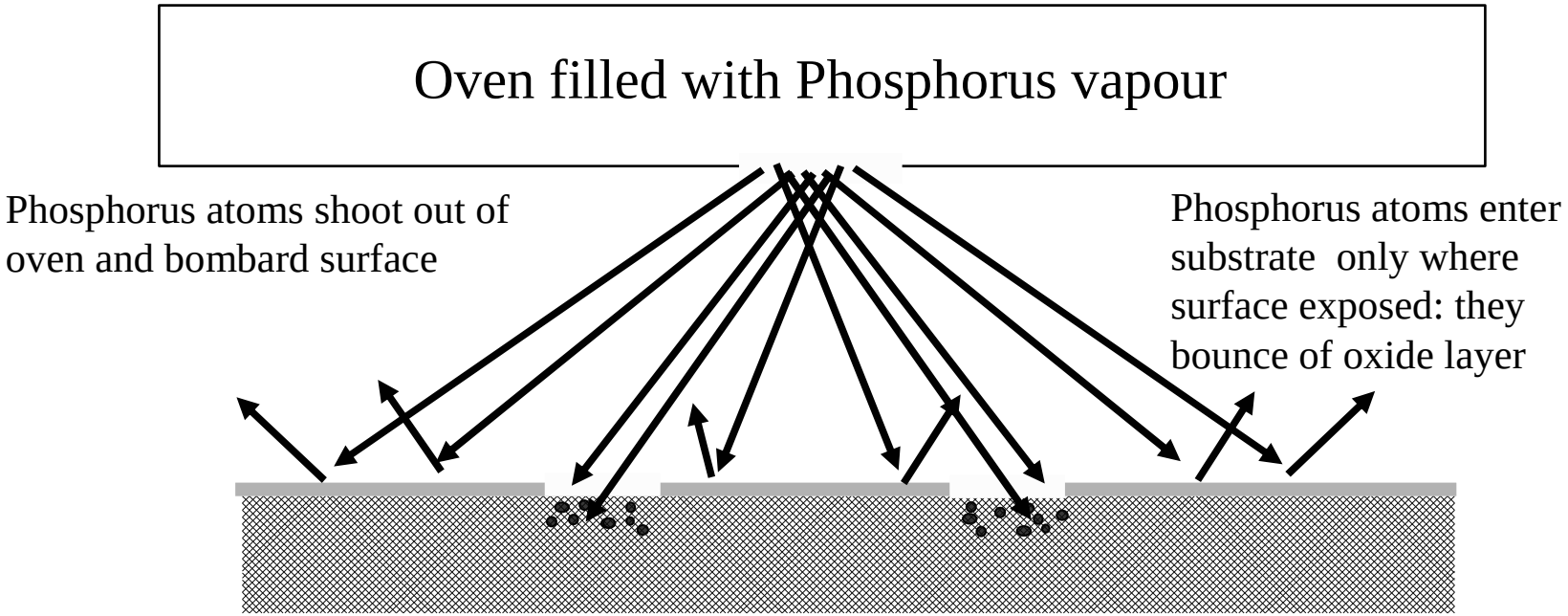


Surface is covered by a photographic mask and exposed to light



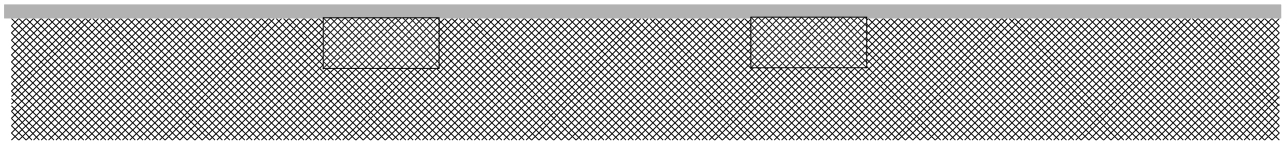
Surface is etched with acid exposing surface where special layer has been exposed to light.



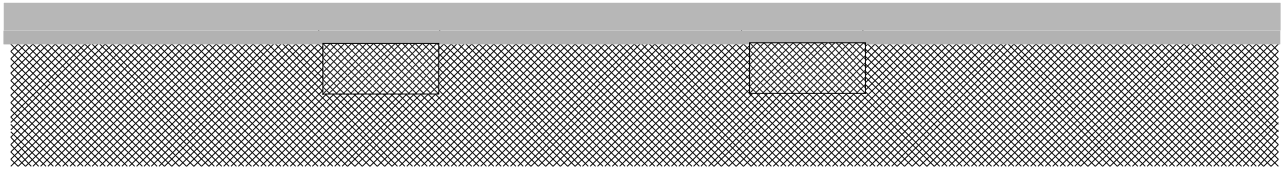


2 n-type regions produced in p-type material

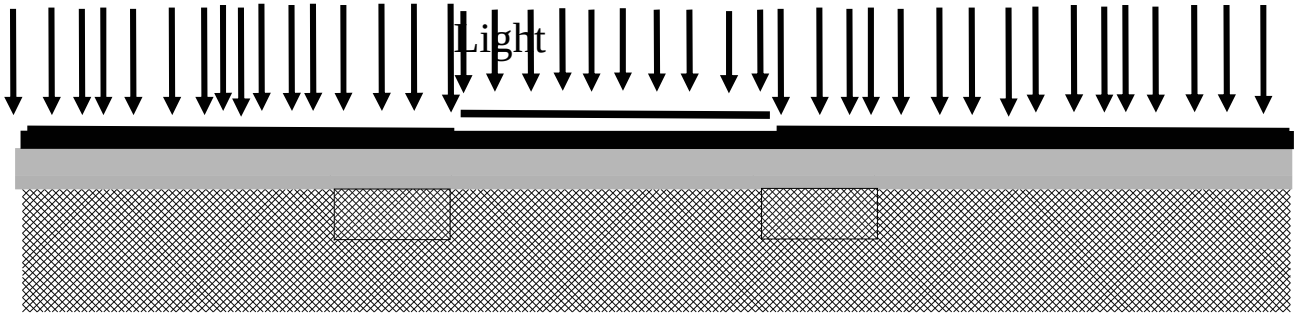
Surface exposed to oxygen again to get silicon oxide layer



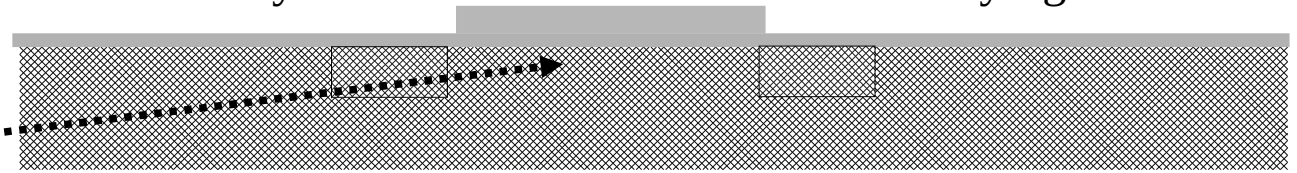
Polysilicon layer deposited over surface



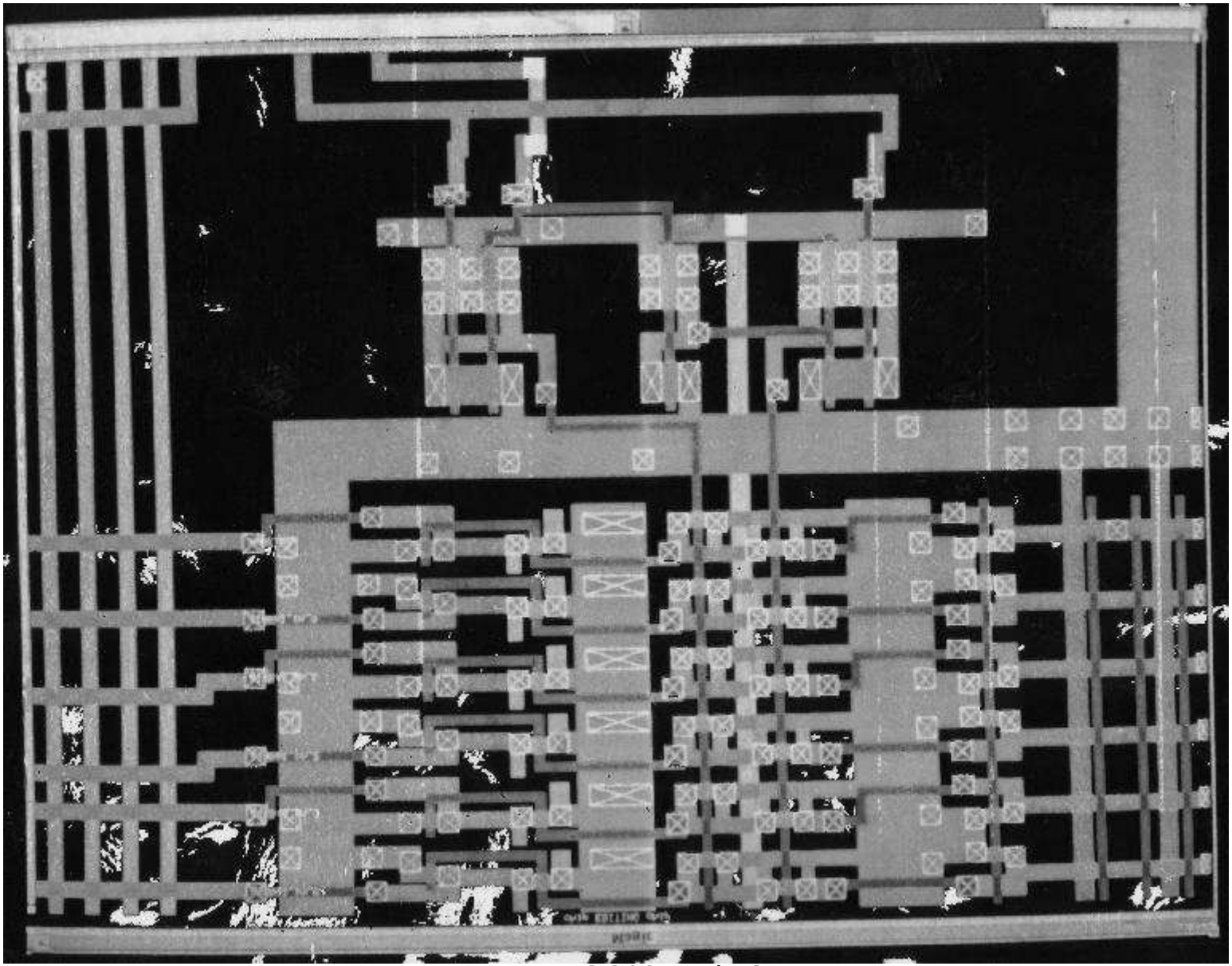
Surface is coated with photo-sensitive material, covered by a photographic mask and exposed to light

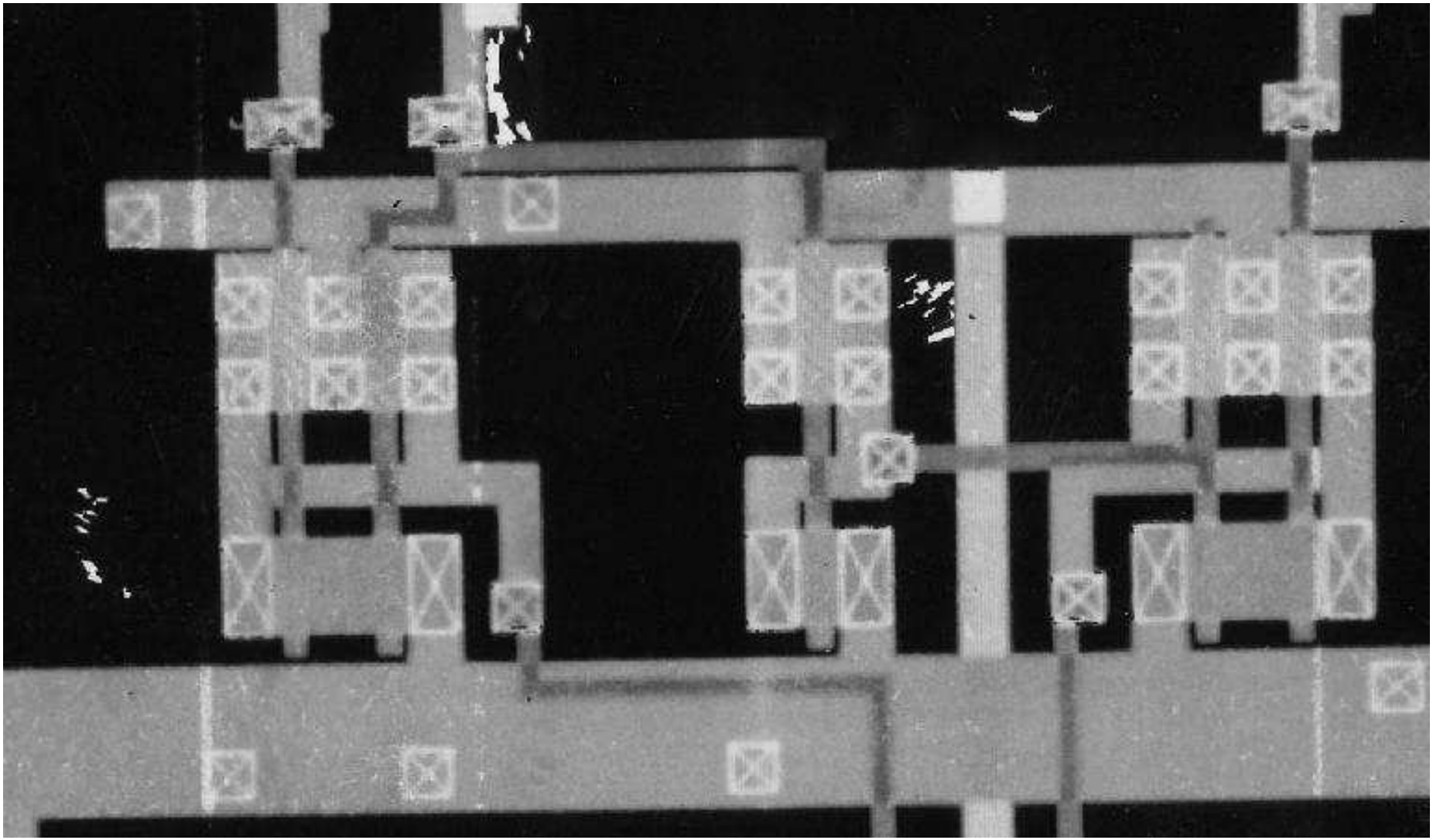


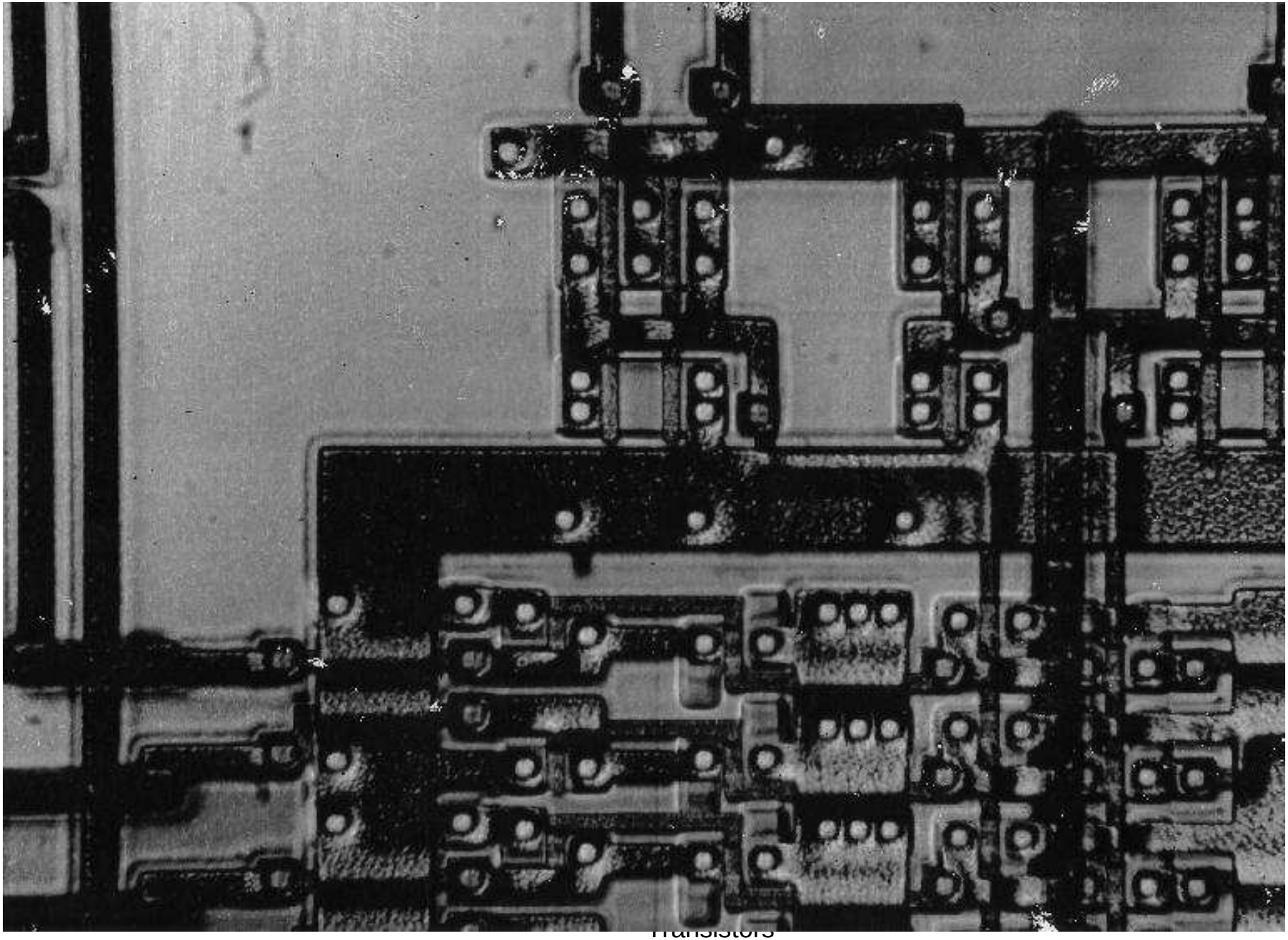
Surface is etched away to oxide surface where sensitised by light.



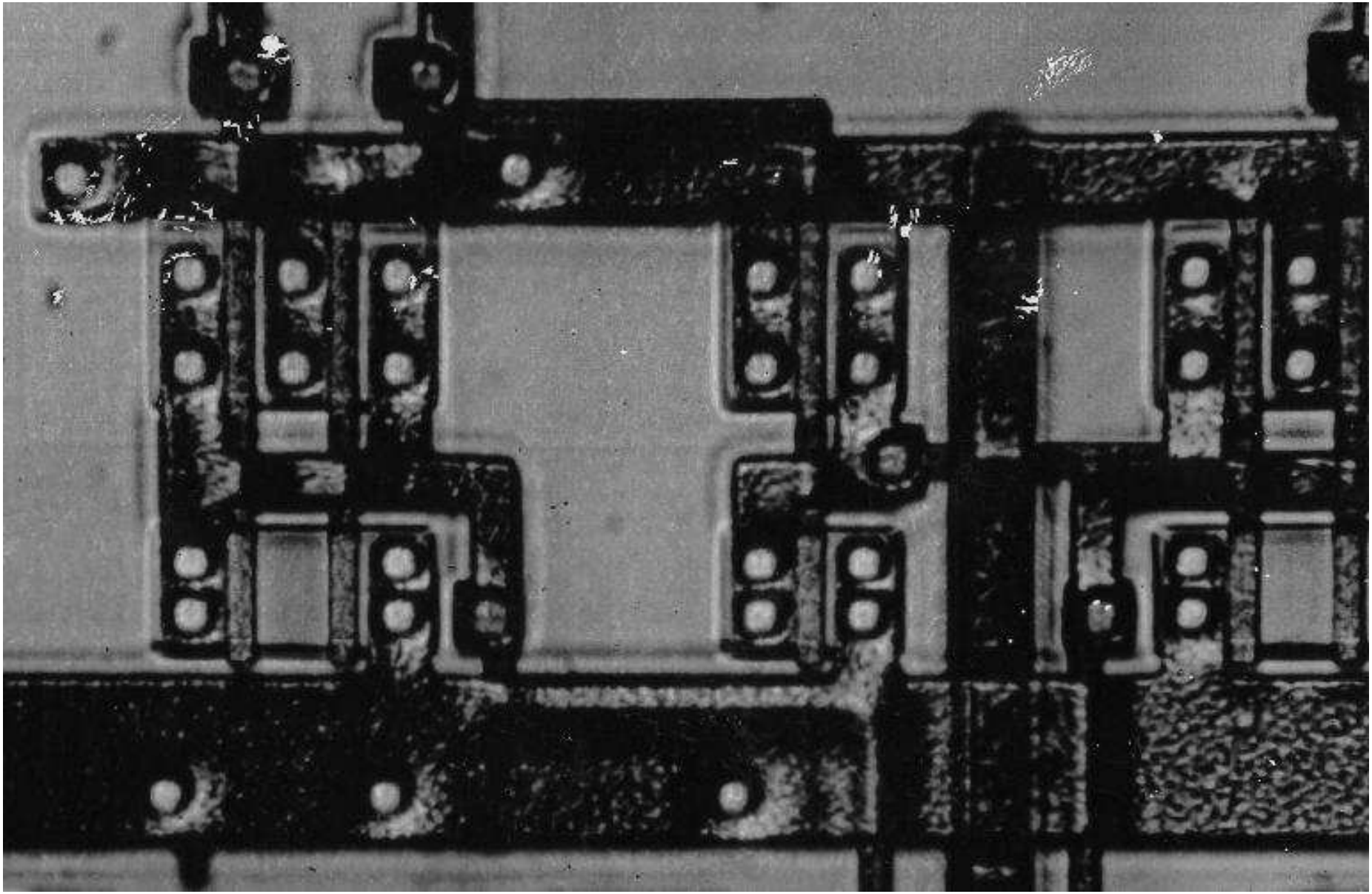
...and repeat adding metal layers, connectors between layers....

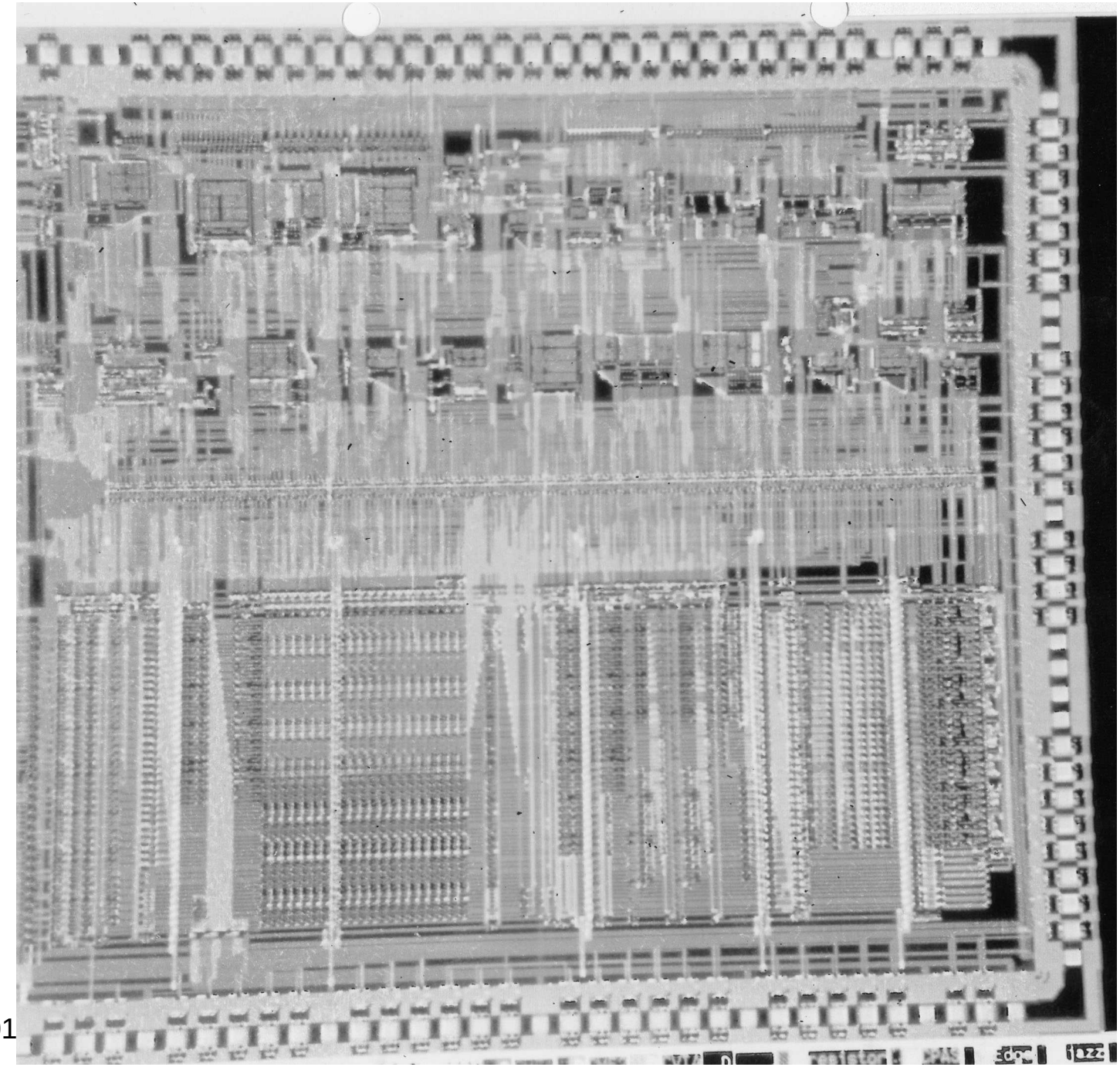


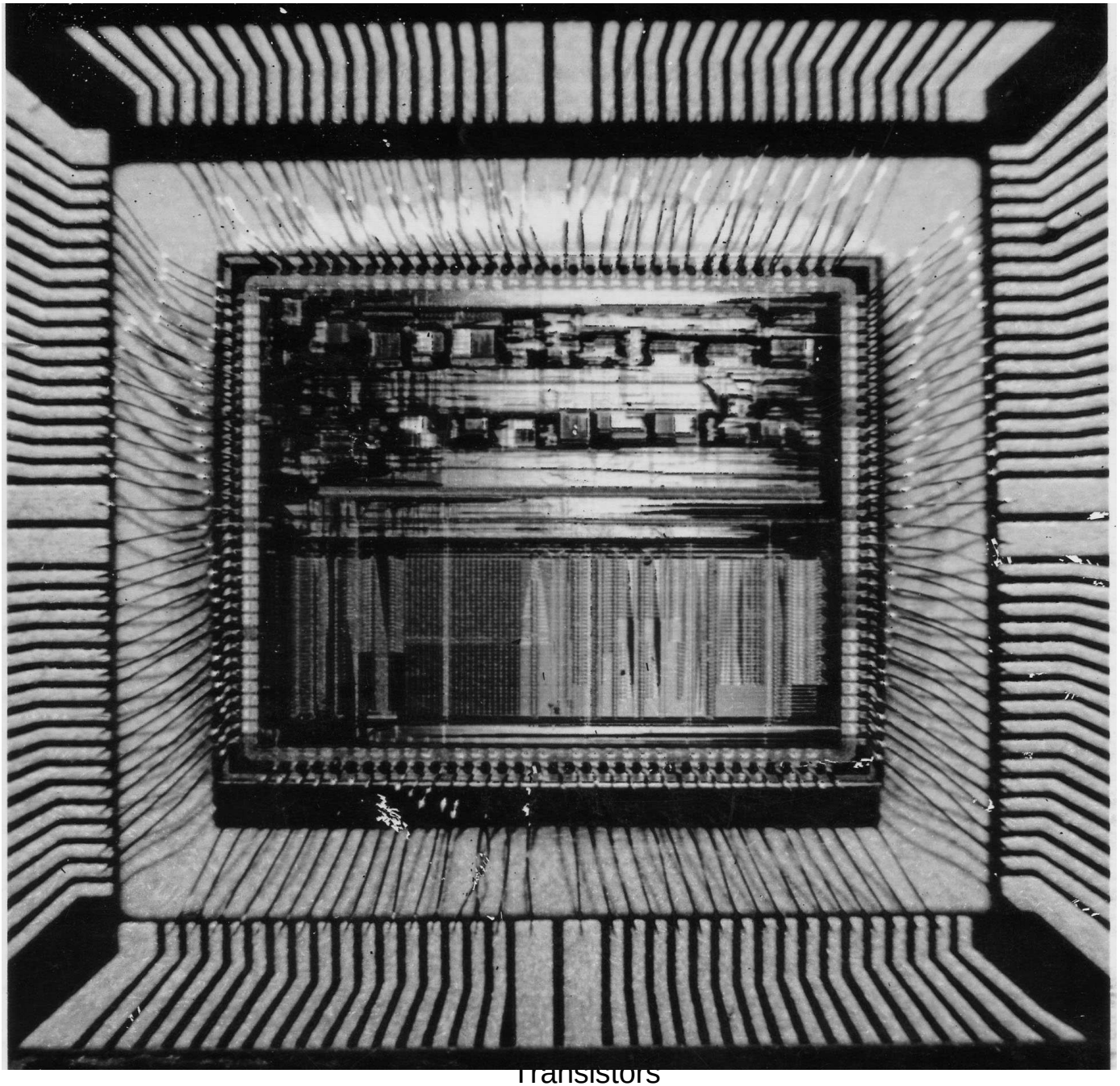


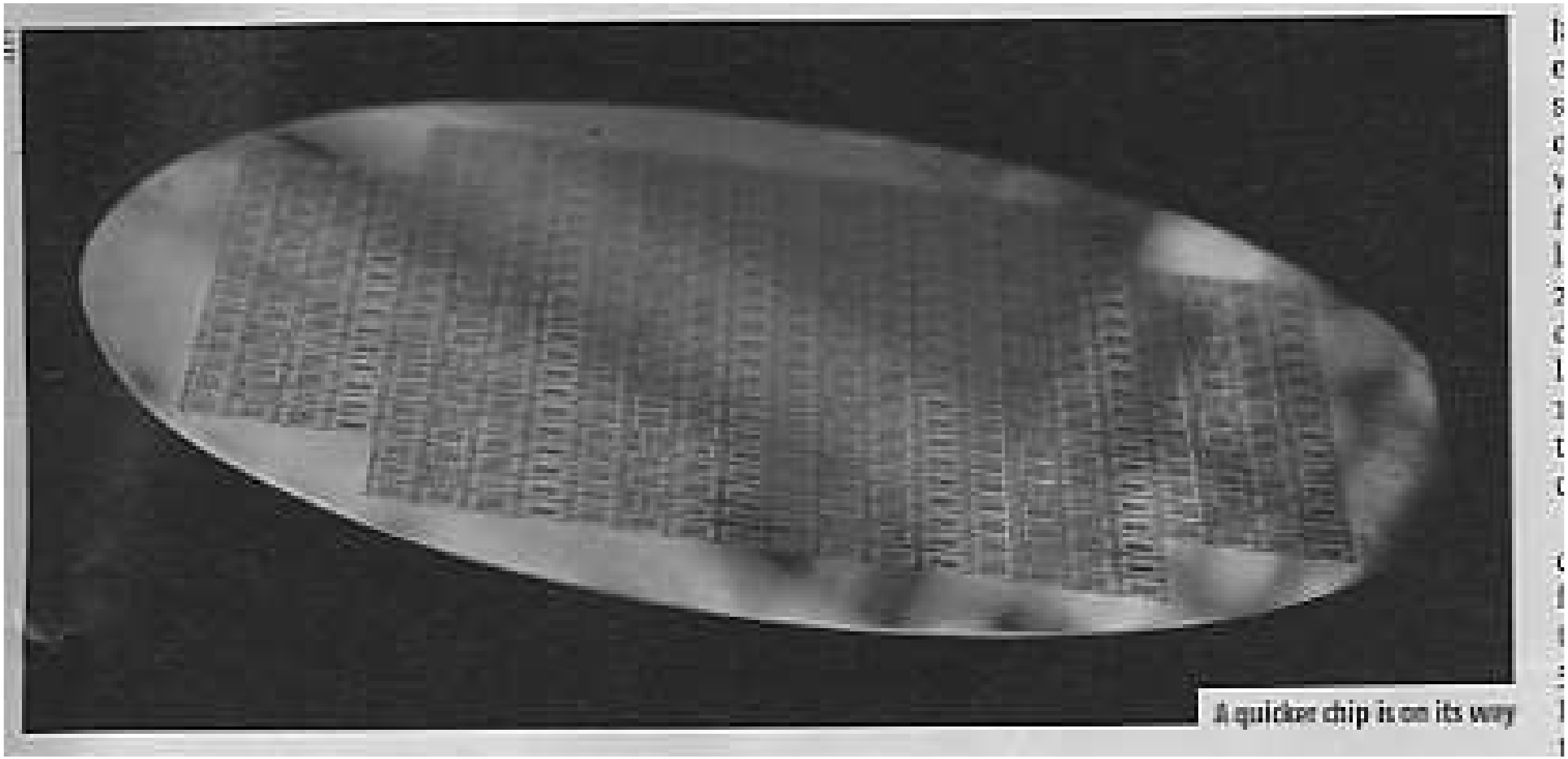


Transistors








A quicker chip is on its way

MAGNACHIP SEMICONDUCTOR STARTS PRODUCTION

THE NON-MEMORY unit of Hynix Semiconductor began operations in Korea last month under the new name of MagnaChip Semiconductor.

Huh Youm, reckons that the company, with its extensive research capabilities, could become one of the world's largest producers of semiconductors. "Our independent