This project is modified from [xhls] reed_solomon_erasure(xapp1273)

Improvement

Since both size of array c (size=4) and d (size=12) are small, use array_partition directive to partition both arrays.

Latency is improved from 1994 cycles to 25 cycles.

HLS Screenshots

Synthesis original

	ynthesis original									
Per	Performance Estimates									
	□ Timing									
	Summary									
	Clock Target Estimated Uncertainty									
	ap_clk 5.00 ns 4.229 ns 0.63 ns									
	Latency									
□ Summary										
	Latency		Latency	(absolute)	Interva	l (cycles)				
	min	max	min	max	min	max	Туре			
	1994	1994	9.970 us	9.970 us	1994	1994	none			
	⊕ Inst									
	Loo lization E	p stimate	es							
	⊕ Loo	p stimate		DSP48E	FF	LUT	URAM			
		p stimate	RAM_18K	DSP48E	FF -	LUT -	URAM -			
- C		stimate y				LUT - 486				
D	E Loo lization E Summar Name	stimate y			-	-				
D E F	E Loo Summar Name OSP	stimate y	RAM_18K - -	-	- 0	-	-			
E FI	E Loo Summar Name OSP Expression IFO Instance Memory	stimate y E	RAM_18K - -	-	- 0	- 486 -	-			
D E Ir	E Loo Summar Name OSP expression IFO nstance Memory Multiplexe	stimate y E	RAM_18K - - - -	- - -	0 - 0 25	- 486 - 21	- - -			
D E Ir	E Loo Summar Name OSP Expression IFO Instance Memory Multiplexe	stimate y E	RAM_18K 128 -	- - - - -	- 0 - 0 25 - 254	- 486 - 21 15 230	- - - - 0			
D E F Ir N	E Loo Summar Name DSP Expression IFO Instance Memory Multiplexe Register Total	stimate y E	RAM_18K 128 - 128	- - - - - -	- 0 - 0 25 - 254 279	- 486 - 21 15 230 - 752	- - - 0 -			
E FI	E Loo Summar Name OSP Expression IFO Instance Memory Multiplexe	stimate y E	RAM_18K 128 -	- - - - -	- 0 - 0 25 - 254	- 486 - 21 15 230	- - - - 0			

Synthesis improved

Performance Estimates

□ Timing

■ Summary

Clock	Target	Estimated	Uncertainty		
ap_clk	5.00 ns	4.278 ns	0.63 ns		

■ Latency

□ Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)			
min max		min	max	min	max	Туре	
	25	25	0.125 us	0.125 us	1	1	function

Detail

- Instance
- ⊥Loop

Utilization Estimates

□ Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	12912	-
FIFO	-	-	-	-	-
Instance	0	-	296	365	-
Memory	96	-	144	9	-
Multiplexer	-	-	-	-	-
Register	0	-	10161	3680	-
Total	96	0	10601	16966	0
Available	280	220	106400	53200	0
Utilization (%)	34	0	9	31	0

Cosim

Cosimulation Report for 'rs_erasure'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	24	24	24	1	1	1

Export the report(.html) using the Export Wizard

System level bring-up

The system is implemented on Pynq Screenshot of Pynq running result

- [0] 0 out of 250 test vectors failed
- [1] 0 out of 250 test vectors failed
- [2] 0 out of 250 test vectors failed
- [3] 0 out of 250 test vectors failed

Total 1000 Test Vectors, Err Count = 0 pass

Exit process