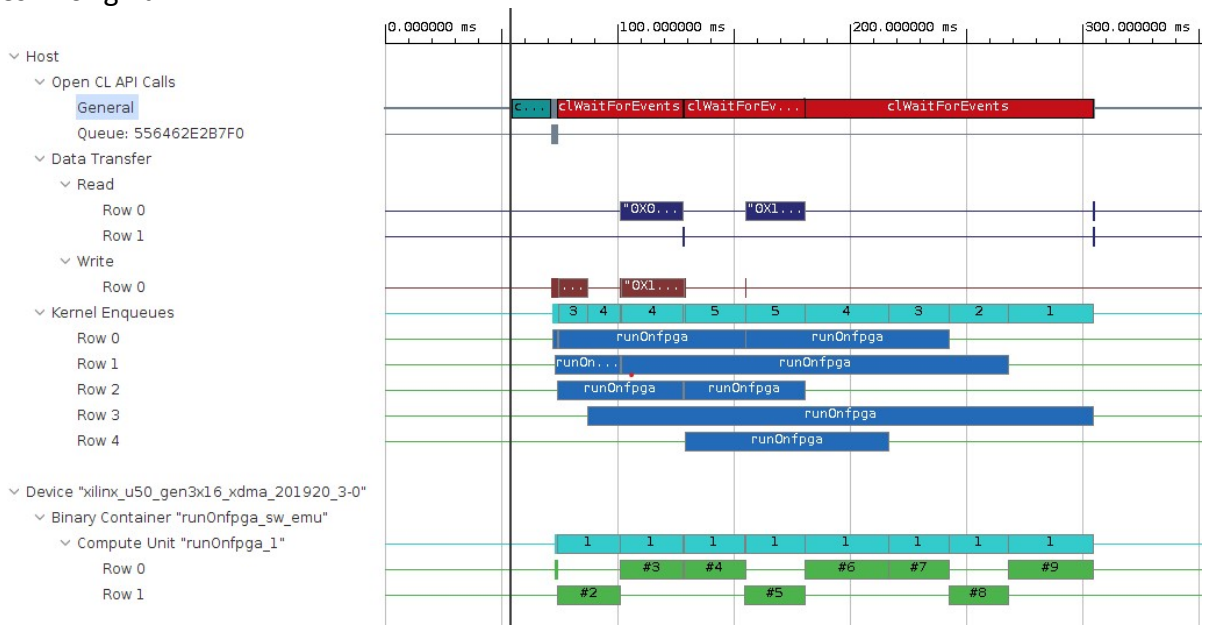
This project is modified from [vitis] Bloom

Improvement

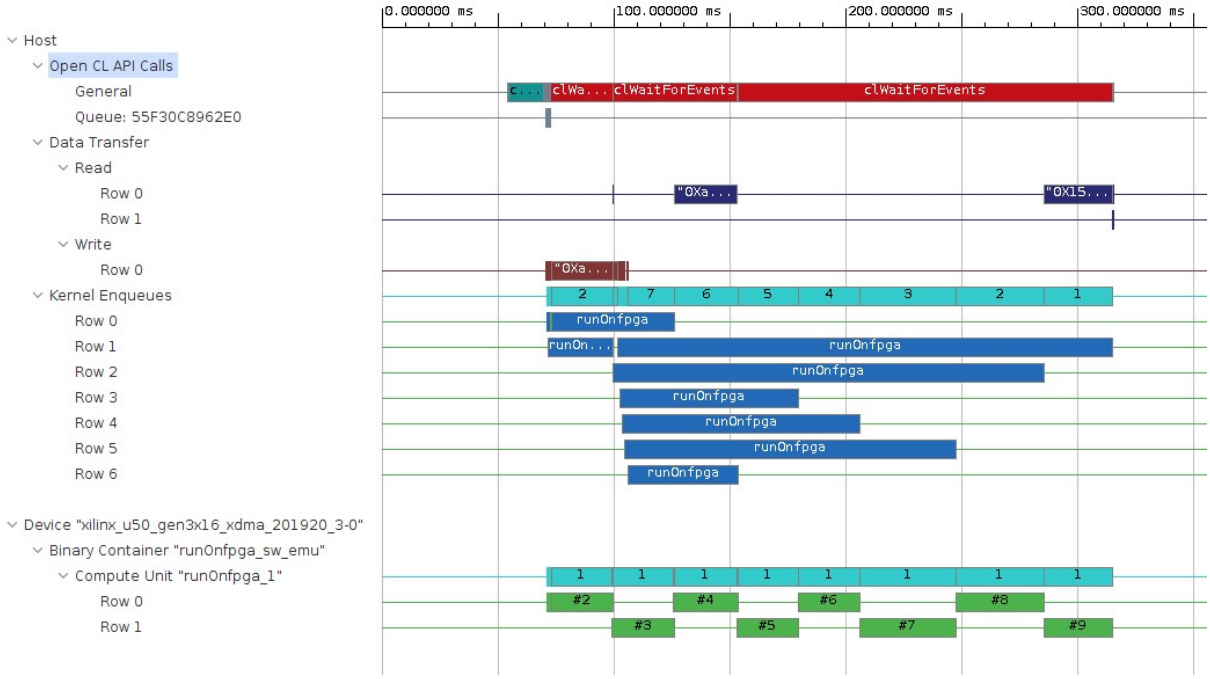
bloom_filter_local is a 2D array.
Original code only performed array partition on dimension 1 of bloom_filter_local.
Optimized code performed array partition on dimension 0 of bloom_filter_local, i.e. the array is fully partitioned.
Synthesis tool can't perform array partition with that size, so only Csim of optimized code is performed.

HLS Screenshots

Csim original



Csim optimized



Synthesis

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	3.33 ns	2.433 ns	0.90 ns

Latency

Summary

min	max	min	max	min	max	Type
?	?	?	?	?	?	none

Detail

Instance

Instance	Module	min	max	min	max	min	max	Type
grp_compute_hash_flags_dataflow_fu_274	compute_hash_flags_dataflow	?	?	?	?	?	?	dataflow

Loop

Loop Name	min	max	Latency	achieved	target	Count	Pipelined
- read_bloom_filter	16385	16385	3	1	1	16384	yes

Utilization Estimates

Summary

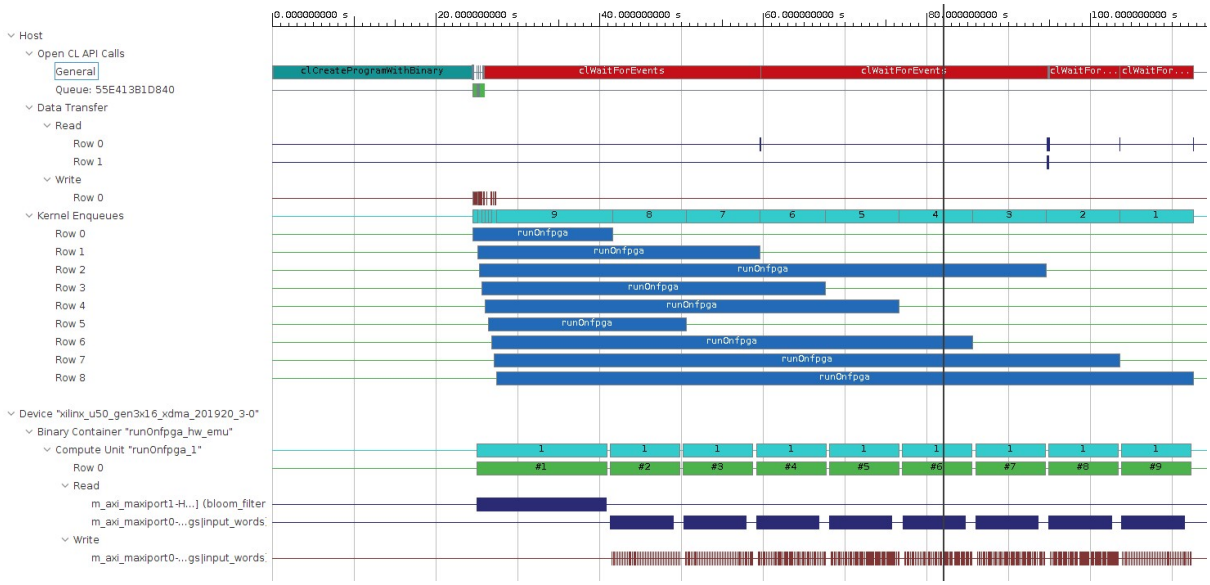
Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	48	-
FIFO	-	-	-	-	-
Instance	62	128	16043	22872	-
Memory	232	-	0	0	0
Multiplexer	-	-	-	464	-
Register	-	-	312	-	-
Total	294	128	16355	23384	0
Available	2688	5952	1743360	871680	640
Available SLR	1344	2976	871680	435840	320
Utilization (%)	10	2	~0	2	0
Utilization SLR (%)	21	4	1	5	0

Detail

Instance

Instance	Module	BRAM_18K	DSP48E	FF	LUT	URAM
grp_compute_hash_flags_dataflow_fu_274	compute_hash_flags_dataflow	58	128	14728	21222	0
runOnfpga_control_s_axi_U	runOnfpga_control_s_axi	0	0	291	490	0
runOnfpga_maxiport0_m_axi_U	runOnfpga_maxiport0_m_axi	2	0	512	580	0
runOnfpga_maxiport1_m_axi_U	runOnfpga_maxiport1_m_axi	2	0	512	580	0
Total		4	62	128	16043	22872	0

Cosim



System level bring-up

The system is implemented on U50 with Vitis.

Using directive to set I/O ports with AXI Lite interface.

It lacks CL/cl2.hpp in the source code, fetching it from https://github.com/ARM-software/ComputeLibrary/blob/master/include/CL/cl2.hpp solved the issue.