This project is modified from [pp4fpga] Matrix Multiplication
Original source URL: https://github.com/KastnerRG/pp4fpgas/tree/master/examples

HLS Screenshots

Synthesis

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	5.00 ns	4.439 ns	0.63 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
1038	1038	5.190 us	5.190 us	1038	1038	none

Detail

Instance

Loop

Cosim

Cosimulation Report for 'matrixmul'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	24952	24952	24952	NA	NA	NA

Export the report(.html) using the Export Wizard

System level bring-up

The system is implemented on Pynq

Screenshot of Pynq running result

```
Entry: /usr/lib/python3/dist-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/lib/python3/dist-packages/ipykernel_launcher.py"
setting hwh
start kernel
Kernel execution time: 0.3680450916290283 s
row  0 ans: correct
row  1 ans: correct
row  2 ans: correct
row  3 ans: correct
row  4 ans: correct
row  5 ans: correct
row  6 ans: correct
row  7 ans: correct
row  8 ans: correct
row  9 ans: correct
row 10 ans: correct
row 11 ans: correct
row 12 ans: correct
row 13 ans: correct
row 14 ans: correct
row 15 ans: correct
row 16 ans: correct
row 17 ans: correct
row 18 ans: correct
row 19 ans: correct
row 20 ans: correct
row 21 ans: correct
row 22 ans: correct
row 23 ans: correct
row 24 ans: correct
row 25 ans: correct
row 26 ans: correct
row 27 ans: correct
row 28 ans: correct
row 29 ans: correct
row 30 ans: correct
row 31 ans: correct

pass
============================
Exit process
```