This project is modified from [xhls] Squared_difference_accumulate

HLS Screenshots

Synthesis

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	5.00 ns	3.127 ns	0.63 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
15	15	75.000 ns	75.000 ns	15	15	none

Detail

Instance

Loop

Cosim

Cosimulation Report for 'diff_sq_acc'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	15	15	15	16	16	16

Export the report(.html) using the Export Wizard

System level bring-up

The system is implemented on Pynq

Screenshot of Pynq running result

```
Entry: /usr/lib/python3/dist-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/lib/python3/dist-packages/ipykernel_launcher.py"
setting hwh
start kernel
Kernel execution time: 0.0015501976013183594 s
1935955
ans = 325466
ans = 1

pass
============================
Exit process
```