This project is modified from [pp4fpga] FIR
Original source URL: https://github.com/KastnerRG/pp4fpgas/tree/master/examples

HLS Screenshots

Synthesis

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	5.00 ns	3.950 ns	0.63 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
10241	10241	51.205 us	51.205 us	10241	10241	none

Detail

Instance

Loop

Cosim

Cosimulation Report for 'block_fir'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	10241	10241	10241	NA	NA	NA

Export the report(.html) using the Export Wizard

System level bring-up

The system is implemented on Pynq

Screenshot of Pynq running result

```
Entry: /usr/lib/python3/dist-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/lib/python3/dist-packages/ipykernel_launcher.py"
setting hwh
start kernel
Kernel execution time: 0.0014128684997558594 s

iter 0 to 255 are all correct
pass
============================
Exit process
```