This project is modified from [vitis] Bloom

**Improvement**

bloom\_filter\_local is a 2D array.

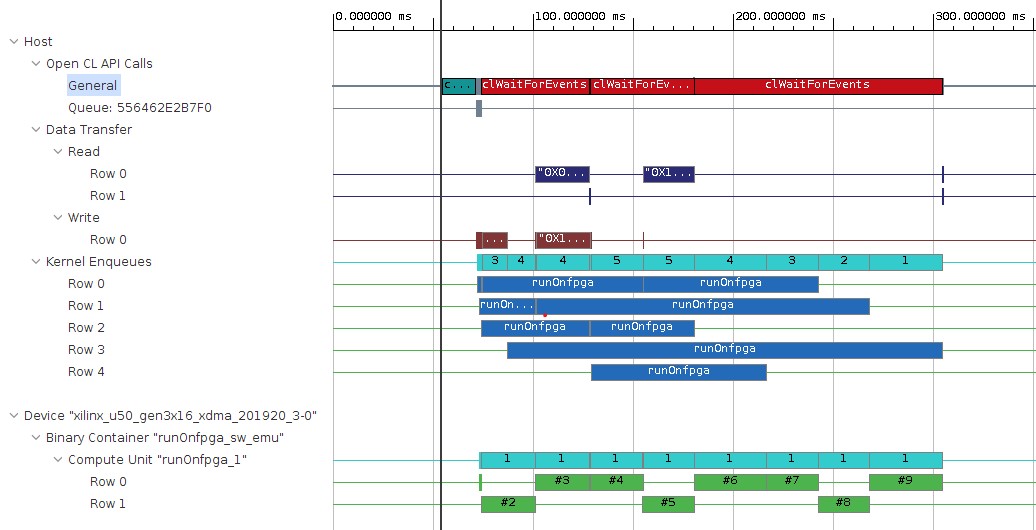
Original code only performed array partition on dimension 1 of bloom\_filter\_local.

Optimized code performed array partition on dimension 0 of bloom\_filter\_local, i.e. the array is fully partitioned.

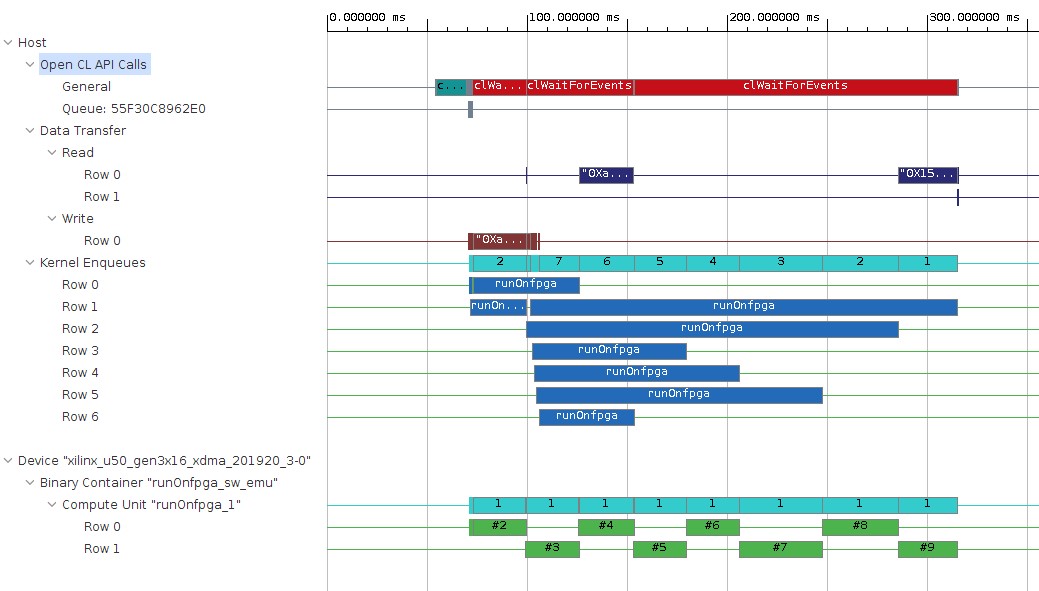
Synthesis tool can’t perform array partition with that size, so only Csim of optimized code is performed.

**HLS Screenshots**

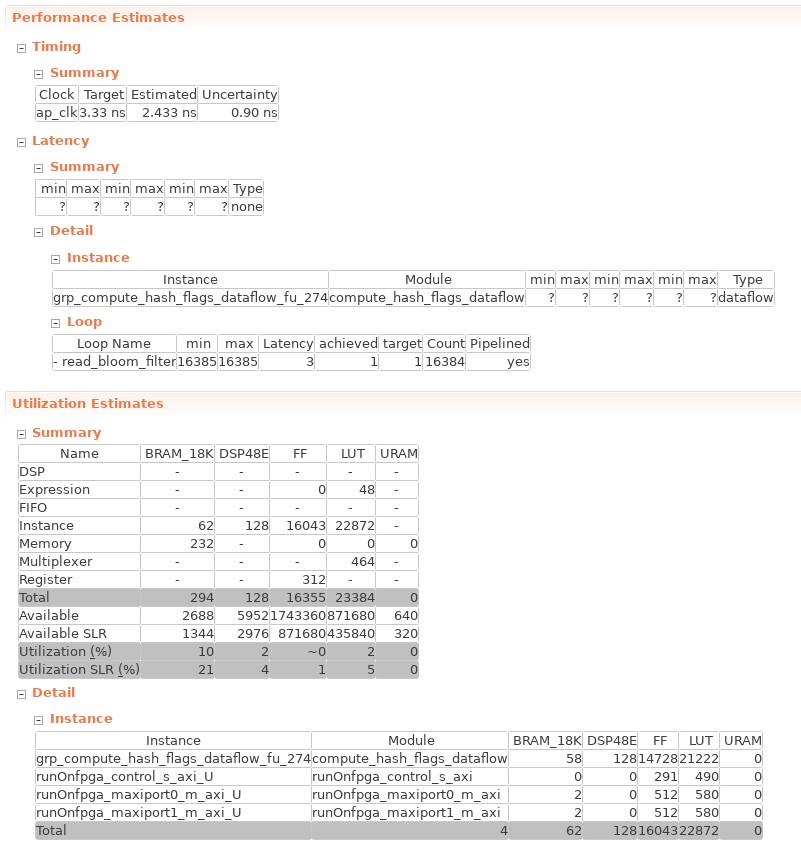
Csim original



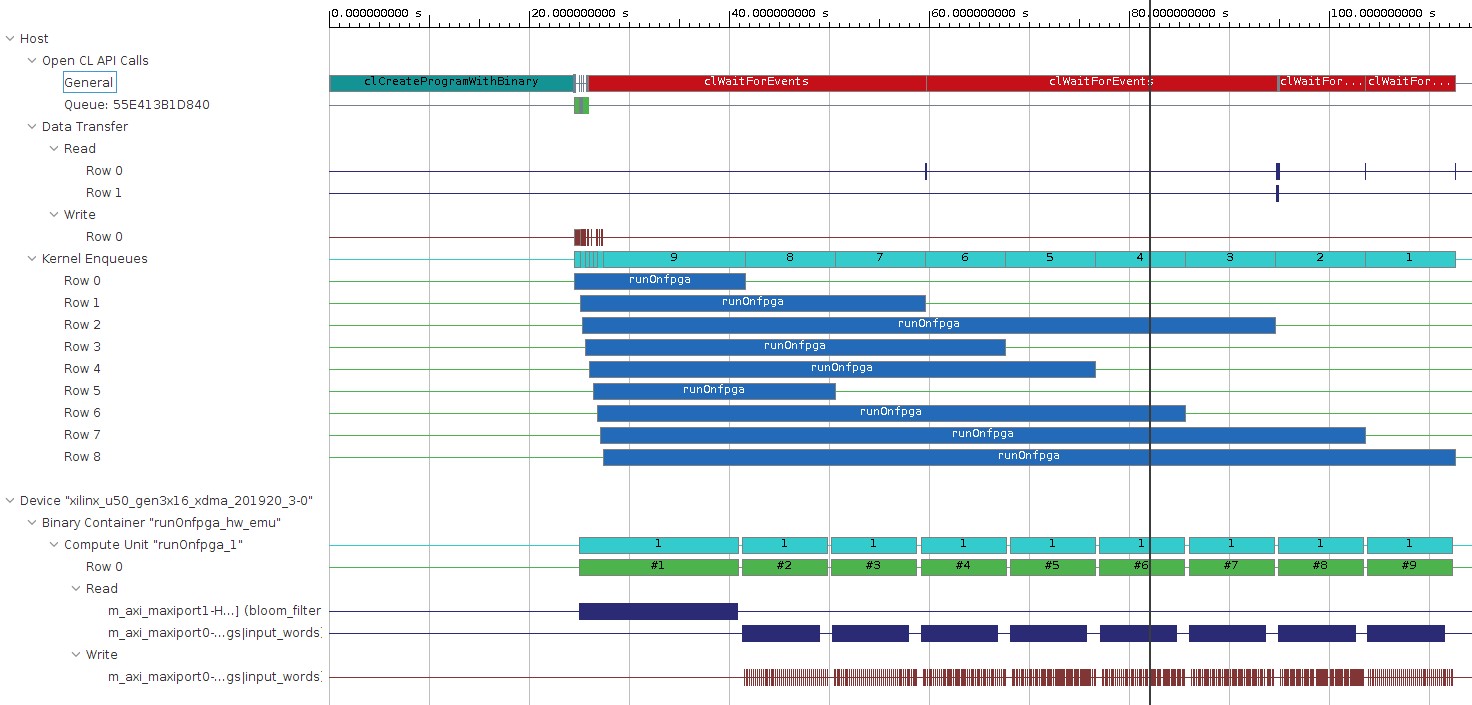
Csim optimized



Synthesis



Cosim



**System level bring-up**

The system is implemented on U50 with Vitis.

Using directive to set I/O ports with AXI Lite interface.

It lacks CL/cl2.hpp in the source code, fetching it from <https://github.com/ARM-software/ComputeLibrary/blob/master/include/CL/cl2.hpp> solved the issue.