Analog Front End Design for Tags in Backscatter-Based Tag-to-Tag Communication Networks

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***Abstract*— Backscatter-based tag-to-tag communication (BBTT) is a paradigm wherein radio-less devices communicate with each other by using purely passive backscatter modulation. This allows for highly inexpensive and low power devices. Traditional backscattering devices like RFID tags are designed to communicate directly with an active reader leading to a centralized framework centered on the reader. Under a BBTT network, the tags talk to each other using backscattering in the presence of an external excitation signal, which can come from multiple sources (e.g., dedicated exciters, WiFi access points, TV towers, or cell phone towers). The two main components that determine the range and robustness of a passive tag-to-tag link are the analog front end (AFE) and the backscatter modulator (BM). In this paper, we investigate the design constraints, optimization goals, and tradeoffs in the design of the AFE for BBTT tags. We first analyze the BBTT link mathematically and then verify the predicted optimal AFE parameters by simulations.**

I. Introduction

Backscattering tag-to-tag network concepts were first introduced by Nikitin [1] and the first study of the communication link was presented in [2]. However, the links they investigated were limited to the feasibility studies and had very close range. Most of the other work in the field has been based on the Intel WISP platform [3], [4], a programmable RFID tag with an on-board microcontroller with sensing inputs. The literature on design of the AFE and BM of traditional passive tags optimized to communicate with active readers is rich [5]–[7]. However, there has not been work in the literature that addresses different optimization aspects of tag architecture and implementation for BBTT communication.

The previous designs of power harvesting and demodulation circuits were mostly concerned with the optimization of the power harvesting. This choice prevailed in the design of conventional and computational RFID tags due to the large modulation depth in the received signals in the reader-to-tag communication. In the proposed BBTT communication, there is a need for a co-design and co-optimization of the power harvesting and the demodulation circuitry. This makes sense because of the interaction between these two circuit blocks and the complexity of the tag-to-tag communication link.

II. Review of BBTT tag architecture

In this section, we review the needed basic blocks of a passive BBTT tag for communication without an active on board transmitter. As shown in Figure 1, the basic BBTT tag consists of an antenna, a power harvesting circuit, an envelope detector as a "zero-consumption" receiver, a modulator as a low power passive transmitter, and a microcontroller for data processing.

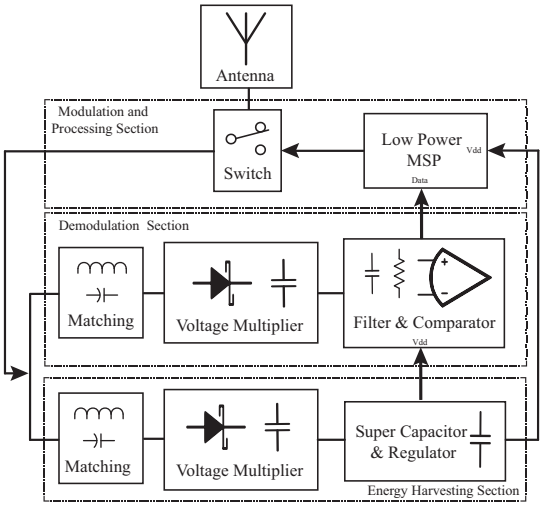

Fig. 1. A basic circuit block diagram of a BBTT tag.

The modulator modulates or backscatters the CW fields by changing the load impedance Z_L of the antenna; then the envelope detector demodulates the signal by sensing the power difference caused by the backscattered signal at different modulation states. This can be described by the following differential RCS equation [8]:

$$\Delta\sigma = \frac{\lambda^2 {G_A}^2}{4\pi}|{\Gamma^*}_{L,1} - {\Gamma^*}_{L,2}|^2, \tag{1}$$

where λ is the wavelength of the CW, G_A is the antenna gain, and $\Gamma^*_{L,i}$ is the conjugate antenna reflection coefficient at different modulation states. This coefficient can be expressed by

$$\Gamma^*_{L,i} = \frac{Z_{L,i} - Z^*_a}{Z_{L,i} + Z_a}, i = 1, 2. \tag{2}$$

The modulator is usually implemented as a switch with different terminating impedances, which depend on the employed digital modulation.

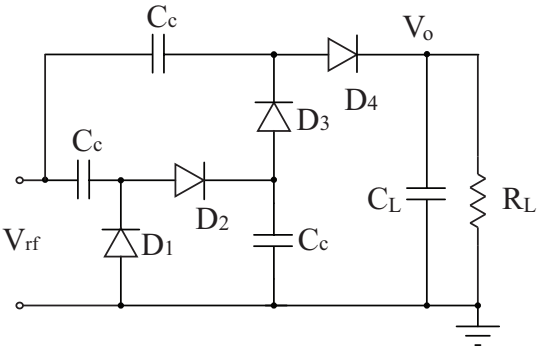

Fig. 2. Power harvesting circuitry comprising two stages of voltage multiplication.

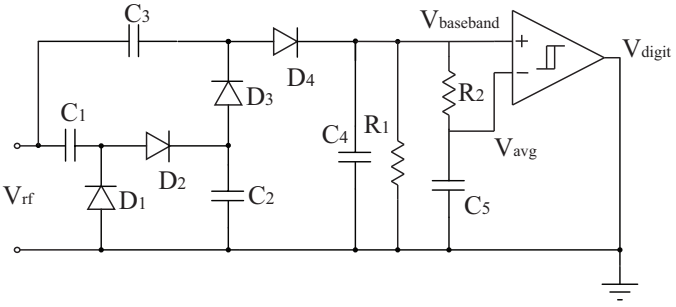

Fig. 3. A BBTT demodulator circuit.

The power harvesting circuit, shown in Fig. 2 contains a voltage multiplier that transforms a low input voltage into a voltage that matches the supply voltage of the demodulation and decoding circuits. To maximize the power transfer from the antenna and minimize the reflection of the power, the voltage multiplier is preceded by an impedance matching circuit. As the impedance of the voltage multiplier depends on the input power, the input impedance of the power harvesting circuit can be power matched to the antenna only for a single input power. To optimize the behavior of the power harvesting circuit, the impedance is exactly matched at the minimum input power at which the tag is expected to operate. For higher input power, due to mismatch in the impedance, power will be reflected at the input of the impedance matching circuit. This leads to an additional constraint on the design of the impedance matching circuit in the case of higher input power than the minimum. The voltage multiplier is followed by a voltage regulator that provides a regulated supply voltage for the demodulation circuit and the decoding logic.

The analog demodulation circuitry, shown in Fig. 3, commonly comprises a voltage multiplier, preceded by an impedance matching and followed by an envelope detection circuit that extracts the baseband signal. The task of the circuit following the envelope detector is to distinguish the different voltage levels in the baseband signal that correspond to different values of the input power at the antenna output. The common implementation of this circuit using discrete components is the generation of an average signal that is compared to the baseband signal.

III. Co-optimization of Power Harvesting and Demodulator

The power harvesting and the demodulator circuits are shown in the basic architecture of the BBTT tag in Fig. 1. A co-design of these circuits is very important due to their interaction. Both the demodulation and the harvesting circuits are getting the power from a single line, and the amount of power each one gets will affect the performance of the other one. So, finding an optimum value for dividing the power ratio between these two circuits is critical in increasing the communication range between two tags.

For the energy harvesting circuit, in addition to selecting the Schottky diode, an important choice in the design for getting higher efficiency is the selection of the optimum number of diode stages. In principle, more stages provide higher voltage. However, in a low power environment, it has been shown that a few stages are more efficient than a larger number of stages [9]. To harvest enough power for the operation of the RF tag without the use of a storage element, it has been shown that the input power has to be around -15 dBm.

For the design of the demodulator circuit, we have to determine the modulation depth in the BBTT communication. To that end, we perform a link budget analysis. We assume that the CW signal is ubiquitous and identical all over the experiment environment under investigation, within which the BBTT tags receive the same excitation signal with input power P_{tag}. To simplify the analysis, we neglect the phase cancellation problem and assume that a backscatter signal received at the Rx tag is always in phase with the CW signal. The backscattered power from the transmitter tag at a given modulation state is

$$P_{txBck,i} = P_{tag}|1 - {\Gamma^*}_{L,i}|^2, i = 1, 2, \tag{3}$$

where ${\Gamma^*}_{L,i}$ is the aforementioned conjugate antenna reflection coefficient that can be calculated by (2). By using the Friis formula, the backscatter power arrived at an Rx tag is

$$P_{rxBck,i} = \frac{P_{txBck,i} G_{tag}^2 \lambda^2}{4\pi {d_{TR}}^2}, i = 1, 2, \tag{4}$$

where d_{TR} is the distance between the communicating tags. Superposing the excitation and backscattering signals, the total power received by the Rx tag is

$$\begin{aligned} P_{rxTot,i}(d_{TR}) &= (\sqrt{P_{tag}} + \sqrt{P_{rxBck,i}})^2 \\ &= k_i(d_{TR}) P_{tag}, i = 1, 2, \end{aligned} \tag{5}$$

where

$$k_i(d_{TR}) = \left(1 + \frac{|1 - {\Gamma^*}_{L,i}| G_{tag} \lambda}{2\sqrt{\pi} d_{TR}}\right)^2, i = 1, 2. \tag{6}$$

As the received baseband data power strength is proportional to P_{tag}, the modulation depth m is only dependent on d_{TR}. For 915 MHz BBTT systems with dipole tag antennas, the modulation depth m as a function of the distance between tags is shown in Fig. 4. The transmitter tag modulates its antenna

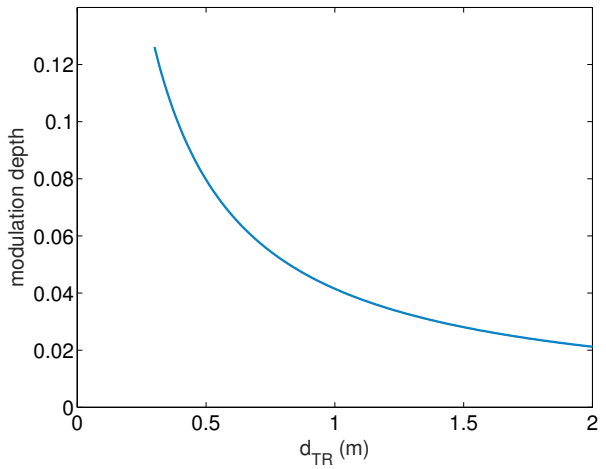

Fig. 4. Modulation depth versus distance.

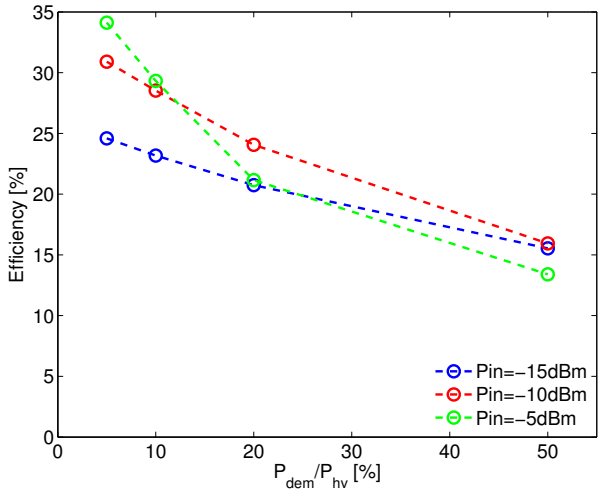

Fig. 5. Efficiency of the power harvesting circuit for different input powers as a function of the fraction of the input power transferred to the demodulator.

load between open and conjugate match impedance, which shows an extremely low m (smaller than 0.1 or even 0.05) at reasonable communication ranges.

In the conventional RFID tag design, it is common to use the voltage sensitivity in terms of absolute input power difference γ (mV/μW) as a key performance indicator for the design. The diode has a square law characteristic at low incident power and a linear characteristic at higher incident power, with the intersection point commonly around -20 dBm. This is the reason why the demodulation circuit can perform well at very low power levels, around -30 dBm. When the power is split between the power harvesting circuit and the demodulation circuit, the input power to the demodulator circuit will be low and the diode operates at low power square region. On the other hand, the difference between the modulated power levels will also be lower. This is why in BBTT communication scenario it is more convenient to define a new sensitivity indicator $\gamma_d Bm$ (mV/dBm) in terms of power ratio to assess the performance of the demodulator circuit. For a fixed d_{TR}, the difference of power at the Rx tag in dBm is:

$$\begin{aligned}&\Delta P_{rxTot\_dBm}(d_{TR})\\&= 10log\left(\frac{k_1(d_{TR})P_{tag}}{1\text{mW}}\right) - 10log\left(\frac{k_2(d_{TR})P_{tag}}{1\text{mW}}\right)\\&= 10log\left(\frac{k_1(d_{TR})}{k_2(d_{TR})}\right),\end{aligned} \tag{7}$$

which is independent of P_{tag}.

The sensitivity of the demodulator circuit depends on the selection of the values of the load capacitance and load resistance. The load capacitance and load resistance set the cutoff frequency of the low pass filter that determines the data rate. The increase of the load resistance will lead to a higher voltage at the output. On the other hand, the resistance of the load will be limited by the thermal noise. The minimum capacitance of the capacitor will be constrained by the ripple voltage.

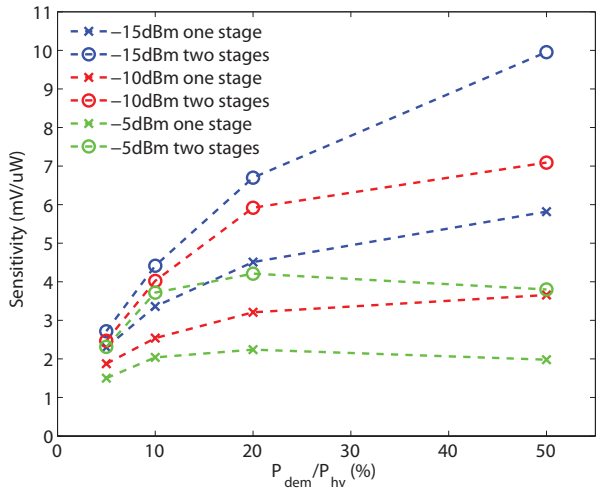

Fig. 6. Differencess in the output voltage of the demodulator circuit for a change in input power of 1 μW as a function of the fraction of input power transferred to the demodulator and at different input powers.

IV. Simulation Results

In this section, we will demonstrate the co-design of the power harvesting and demodulator circuits for the optimal power transfer and the optimal voltage sensitivity of the demodulator circuit. The voltage sensitivity of the demodulator circuit is directly related to the communication range as shown in the previous section.

The energy harvesting and demodulator circuits were simulated using the Agilent Advanced Design System (ADS) software. For the energy harvesting, we used two stages of voltage multipliers because in the applications of BBTT tags the input power levels are low. We also assumed that optimal load was present at the output of the power harvesting circuit (which leads to maximum power efficiency). We examined the performance of the demodulator circuit with one and two stages of voltage multiplication. The matching circuits were

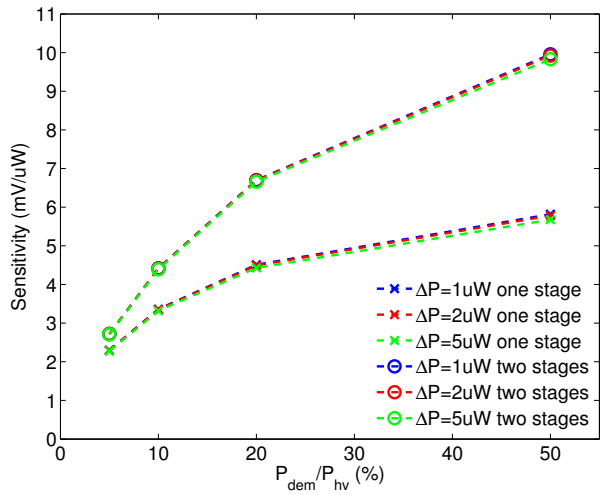

Fig. 7. Differences in the normalized output voltage of the demodulator circuit for a change in input power of 1 μW, 2 μW and 5 μW as a function of the fraction of input power transferred to the demodulator.

employed to divide the incoming power between these two sections while the overall impedance was set at 50Ω. The matching was achieved for input power of -15 dBm. The ratio of the input power of the demodulator and the power of the harvesting circuit was varied and had values 5%, 10%, 20%, and 50%. As the input power changed, due to mismatch in the impedances and the non-linear behavior of the diodes, the efficiency of the power harvesting and the voltage sensitivity changed. We also wanted to observe this effect for different input powers and the simulations were repeated for input powers of -10 dBm and -5 dBm. It is important to note that at these different input power levels, the ratio of input power of the demodulator and the power of the harvesting circuit would also change.

The efficiency of the power energy harvesting circuit, that is, the ratio of harvested power and total input power, is shown in Fig. 5 as a function of the ratio of power division between the demodulator and the power harvesting circuit. The efficiency is also shown for different input power levels. For the optimized low input power of -15 dBm, we can see that the non-linearity of the diodes does not affect the performance, as the efficiency is almost linear with the power that is actually transferred to the power harvesting circuit. For the higher input powers, we can notice that the mismatch in the matching circuit and the non-linearity of the diodes significantly reduce the efficiency.

The performance of the demodulator circuit is defined by its voltage sensitivity, i.e., by the voltage difference at the output of the demodulator circuit for a constant power difference at the input. From the simulations we obtained differences in output voltage levels for changes in input powers of 1 μW. The output voltage was obtained for different ratios in the power transferred to the demodulator circuit and for different levels of input power of -5 dBm, -10 dBm, and -15 dBm. The results are shown in Fig. 6. We also investigated the voltage sensitivity when the modulation depth was increased, i.e., when the change in the input power was 1 μW, 2 μW and 5 μW, respectively. The sensitivity is shown in Fig. 7. We can notice that the sensitivity does not change with the modulation depth at the power level of -15 dBm.

From these simulation results, we can first observe that the two stages of the voltage multiplication provide higher sensitivity as expected. When the power transferred to the demodulator circuit increases, due to the characteristic of the diode, the sensitivity is actually decreased. This effect is even more pronounced for higher input power levels. In the specific design that we investigated, we can conclude that the power ratio of 10% between the power transferred to the demodulator circuit and the power transferred to the power harvesting circuit is optimal. This ratio provides both high power efficiency and high voltage sensitivity.

V. Conclusion

The use of the BBTT communication paradigm in conjunction with multihop communication will allow for building networks with immense scalability at very low costs. This type of communication is vital in unlocking the vast potential of the Internet-of-Things. The optimization of the tag architecture in order to achieve increased communication ranges under scarce energy resources presents an important task on this path. We have demonstrated that co-design of the power harvesting and demodulator circuit enables co-optimization of the power efficiency and the voltage sensitivity of the demodulator that ultimately extend the communication range in BBTT communication.

Acknowledgment

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