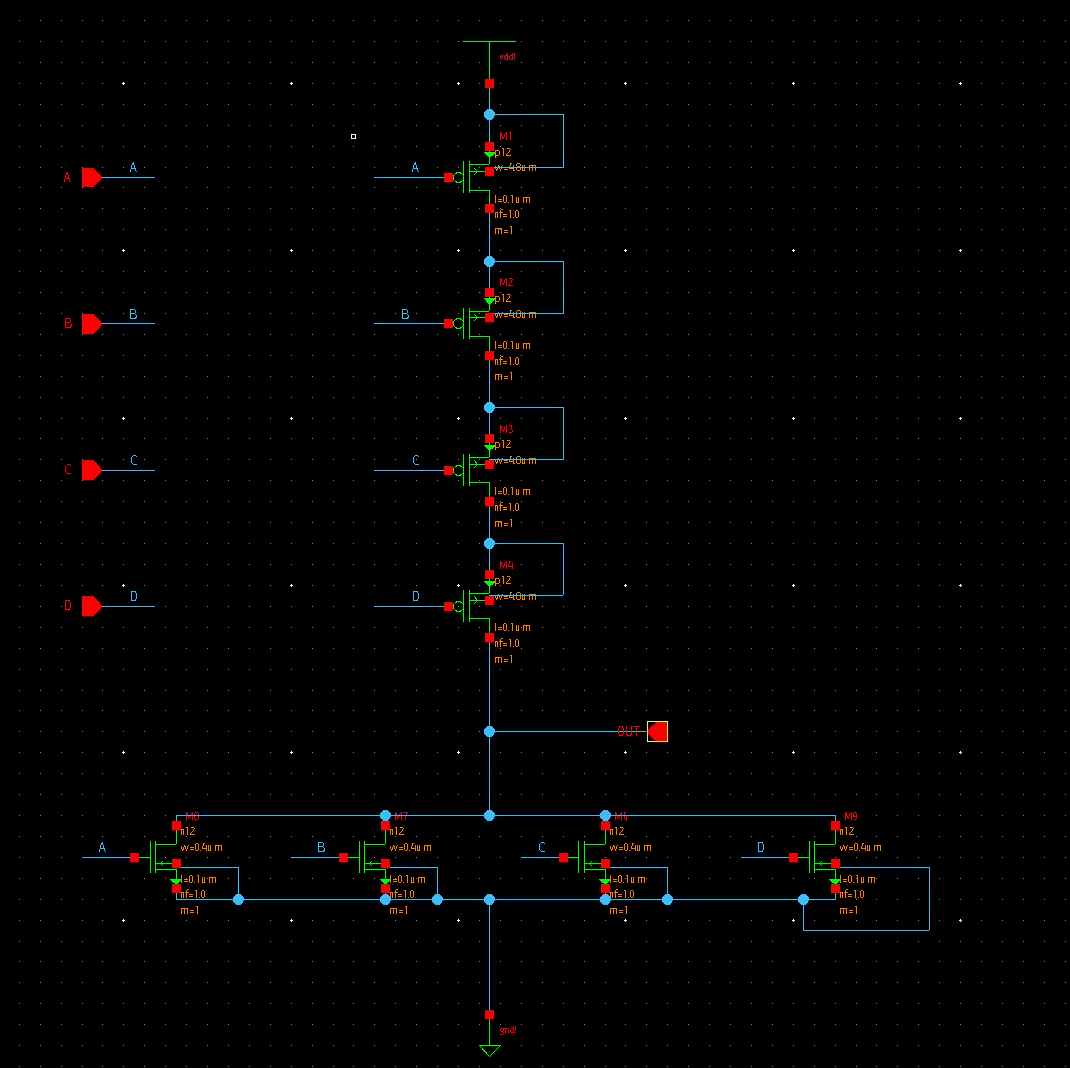
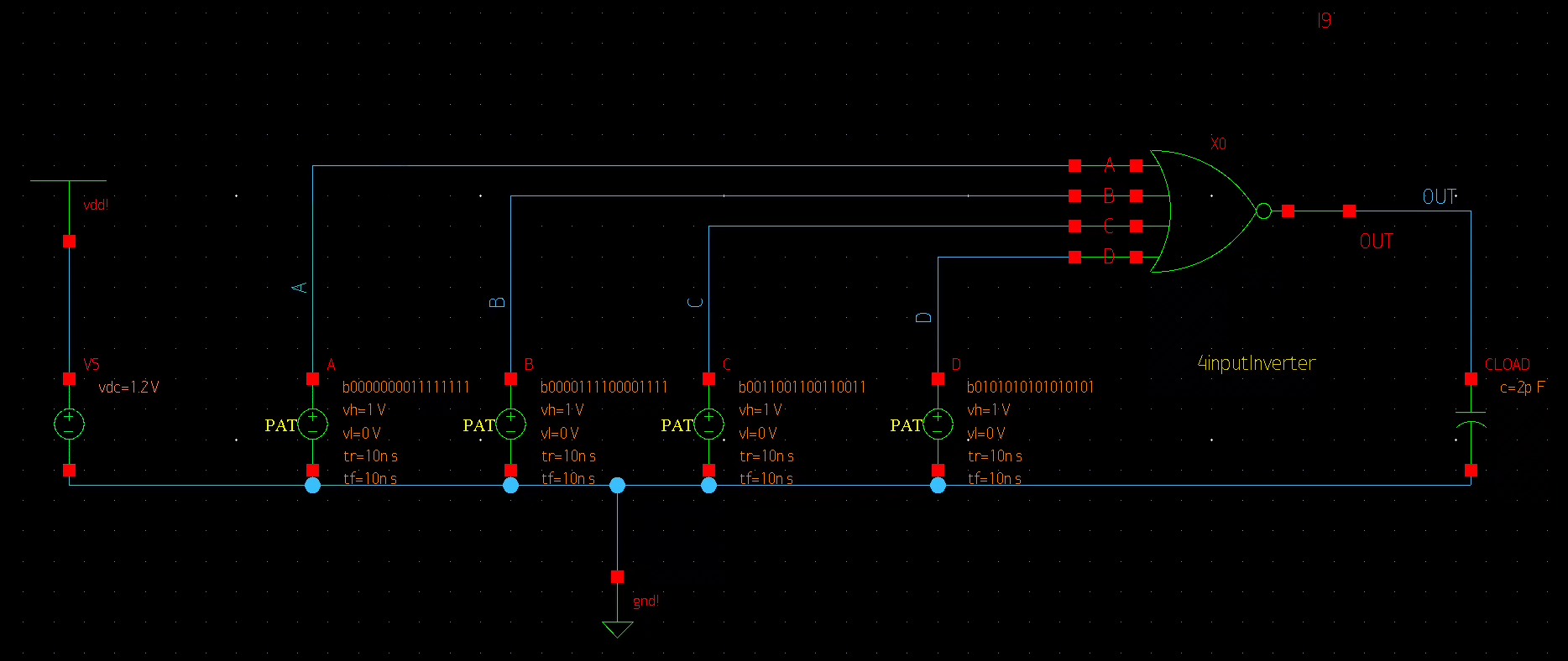
4 input NOR Schematic

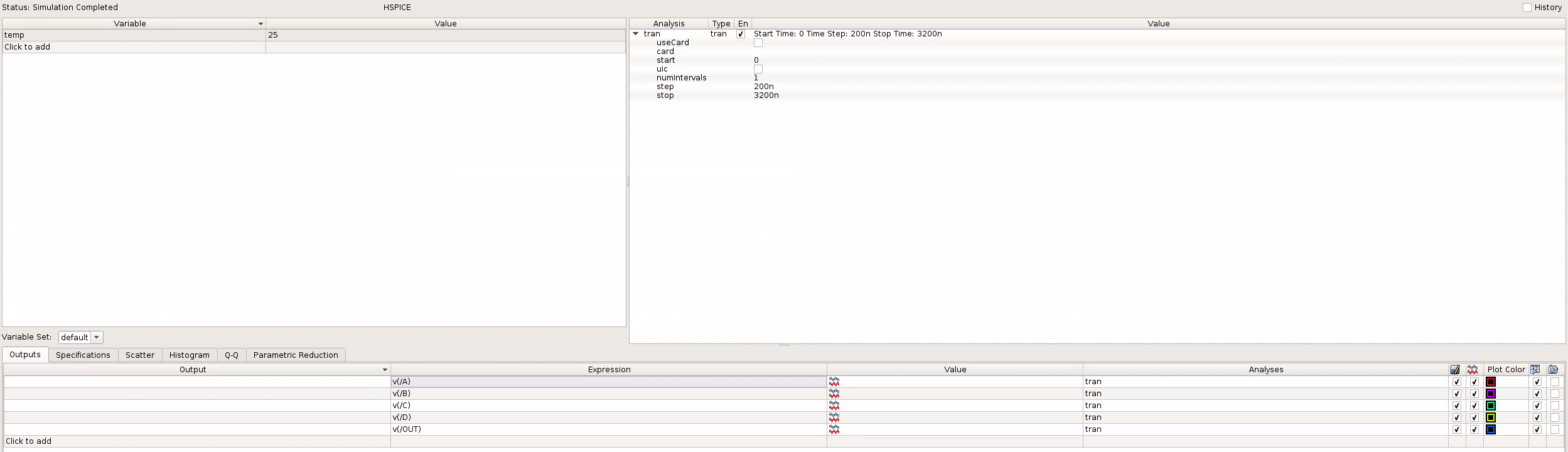


4 input NOR Symbol



Transient Simulation

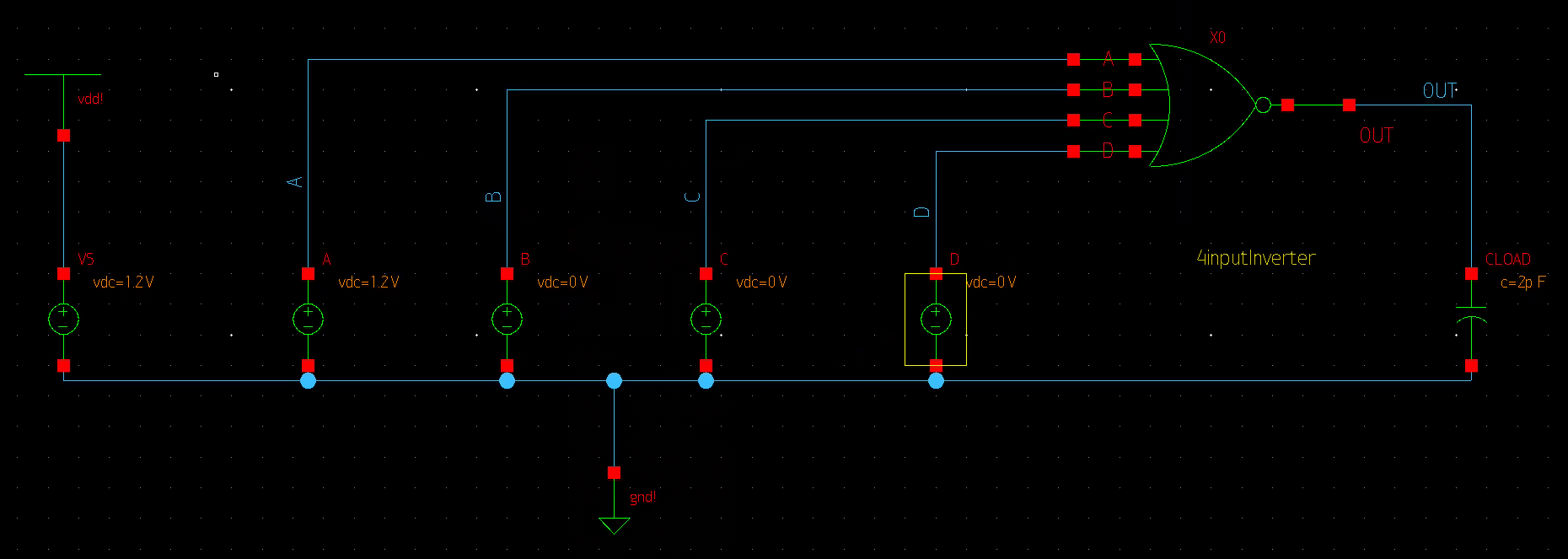


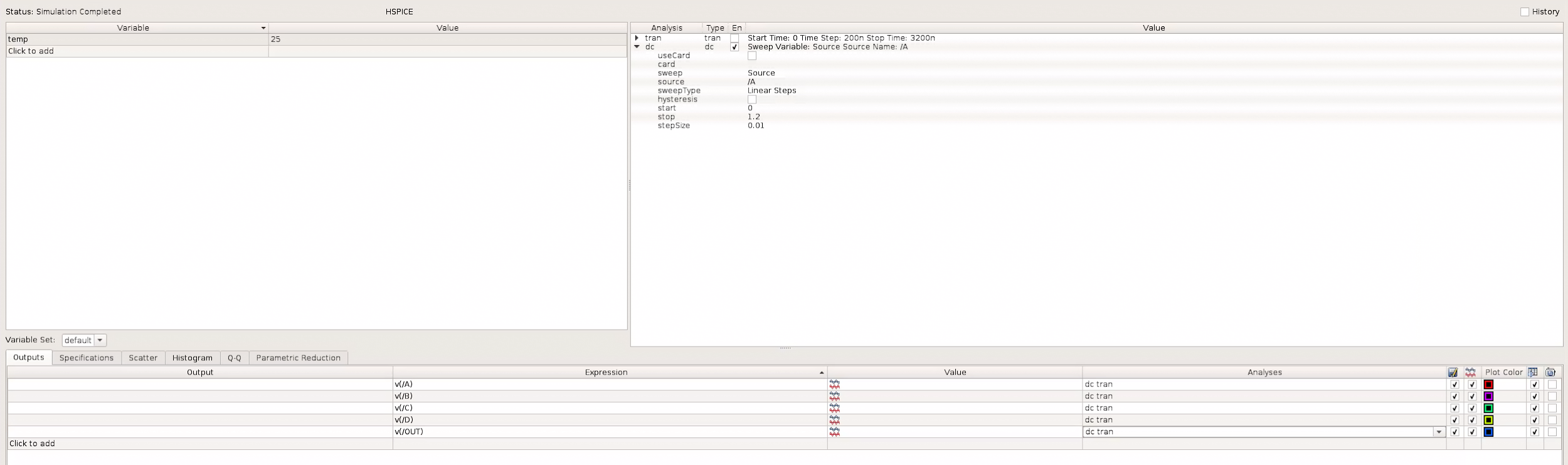


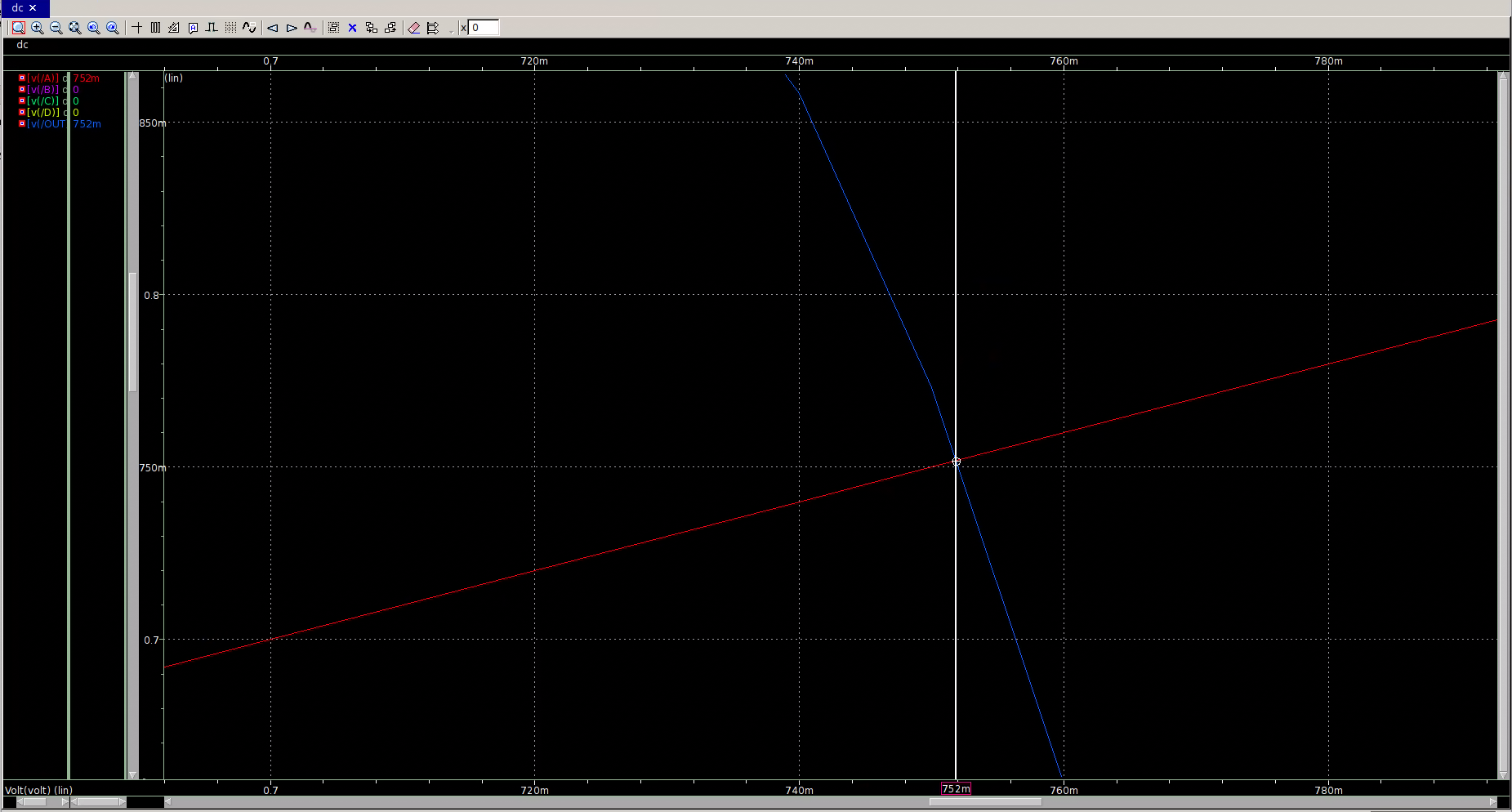


Rise and fall time of output: 10.7 ns.

Input A Sweep

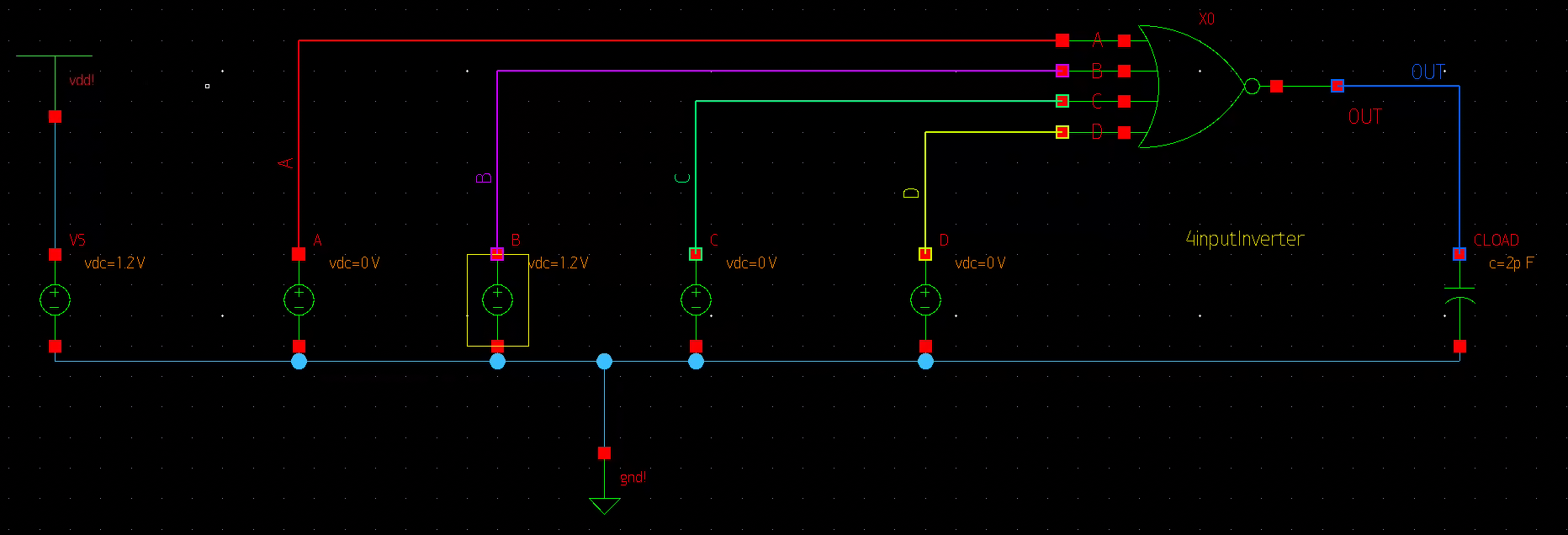


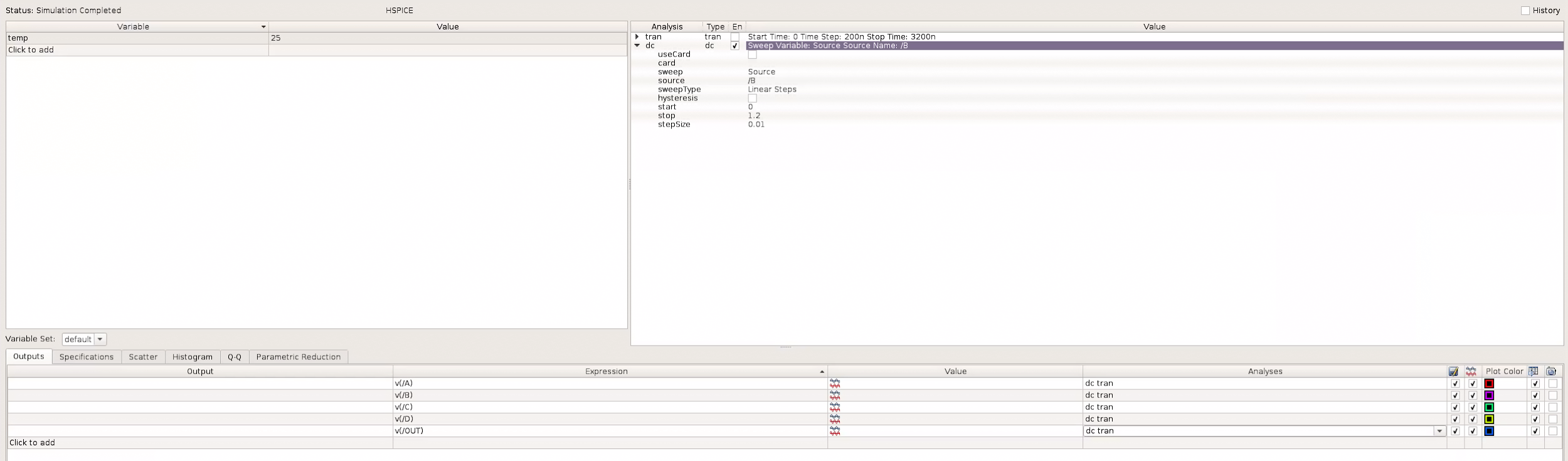


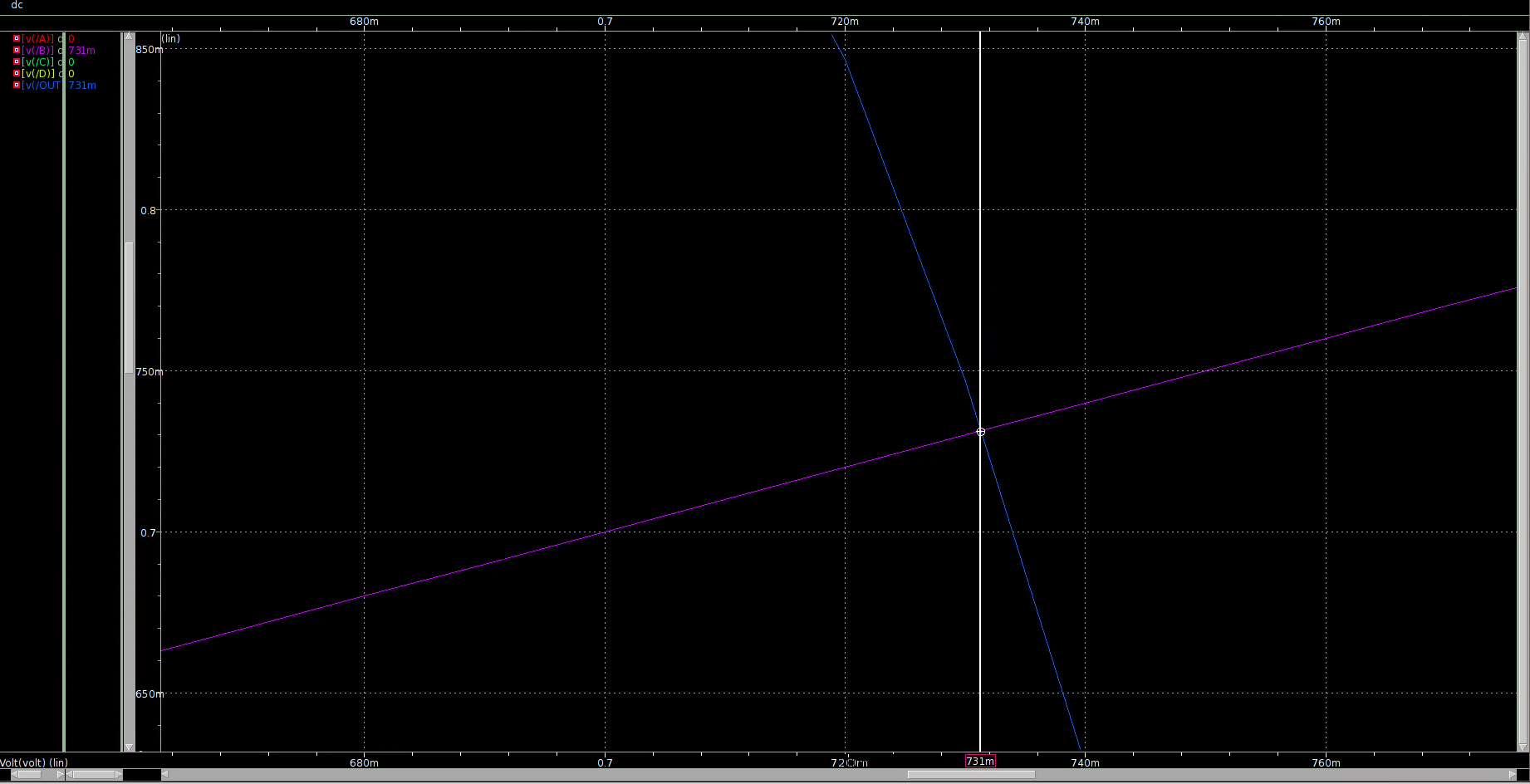


Vm = 752 mV

Input B Sweep

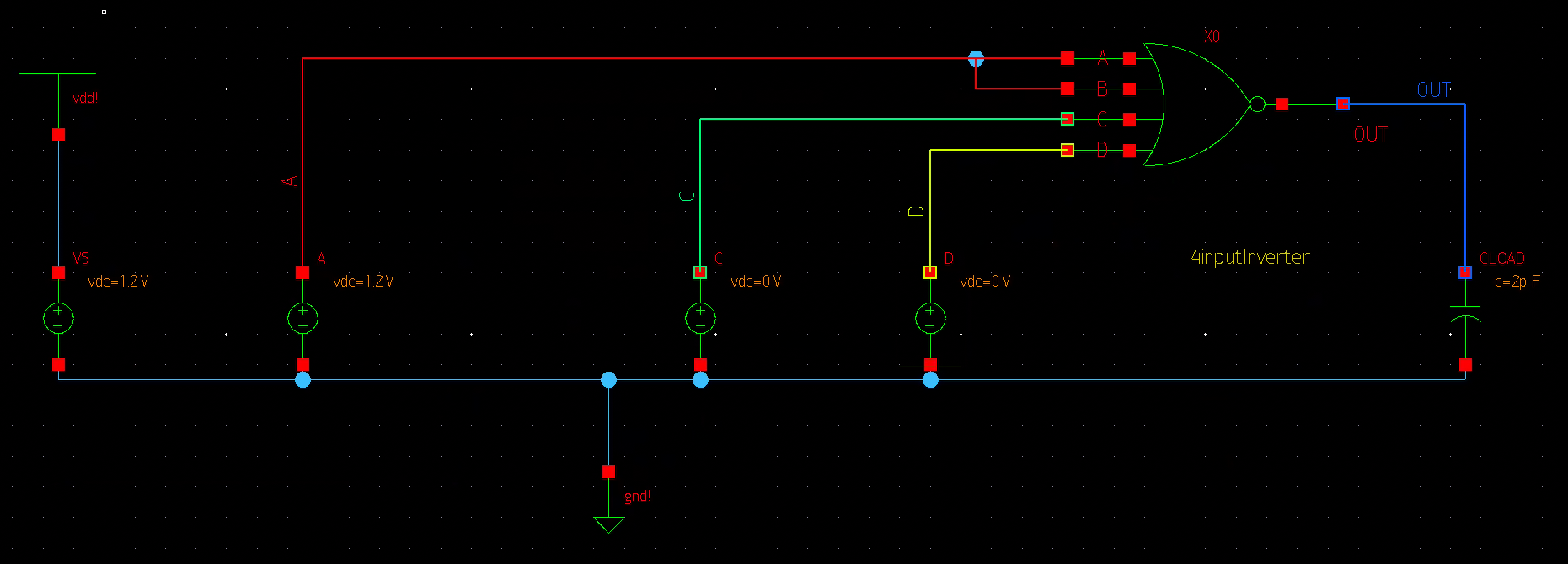


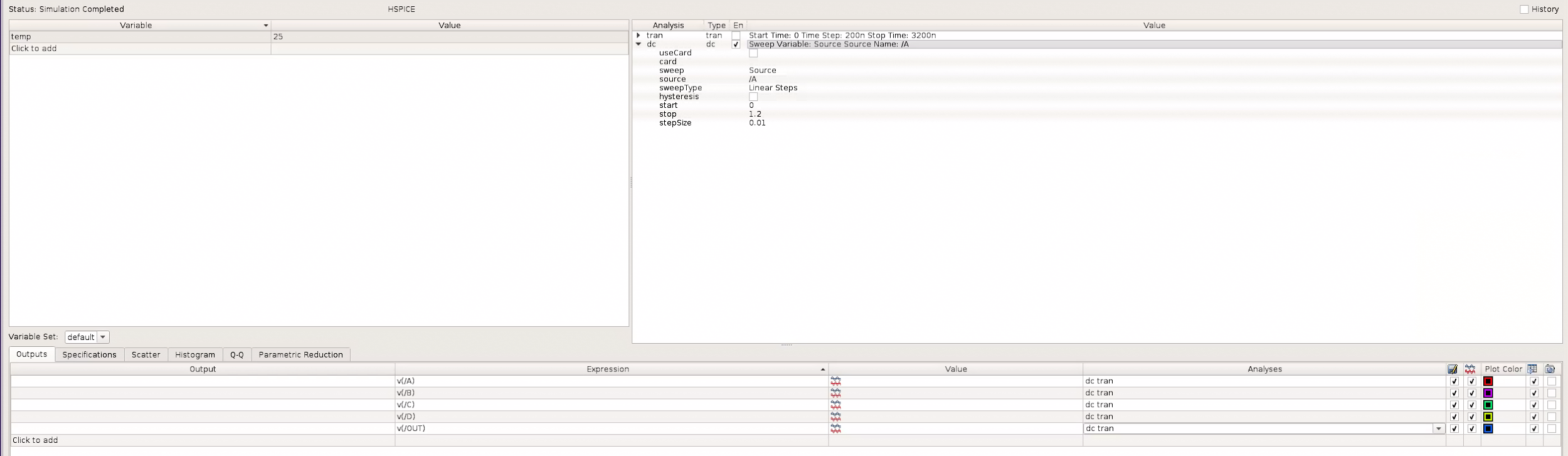


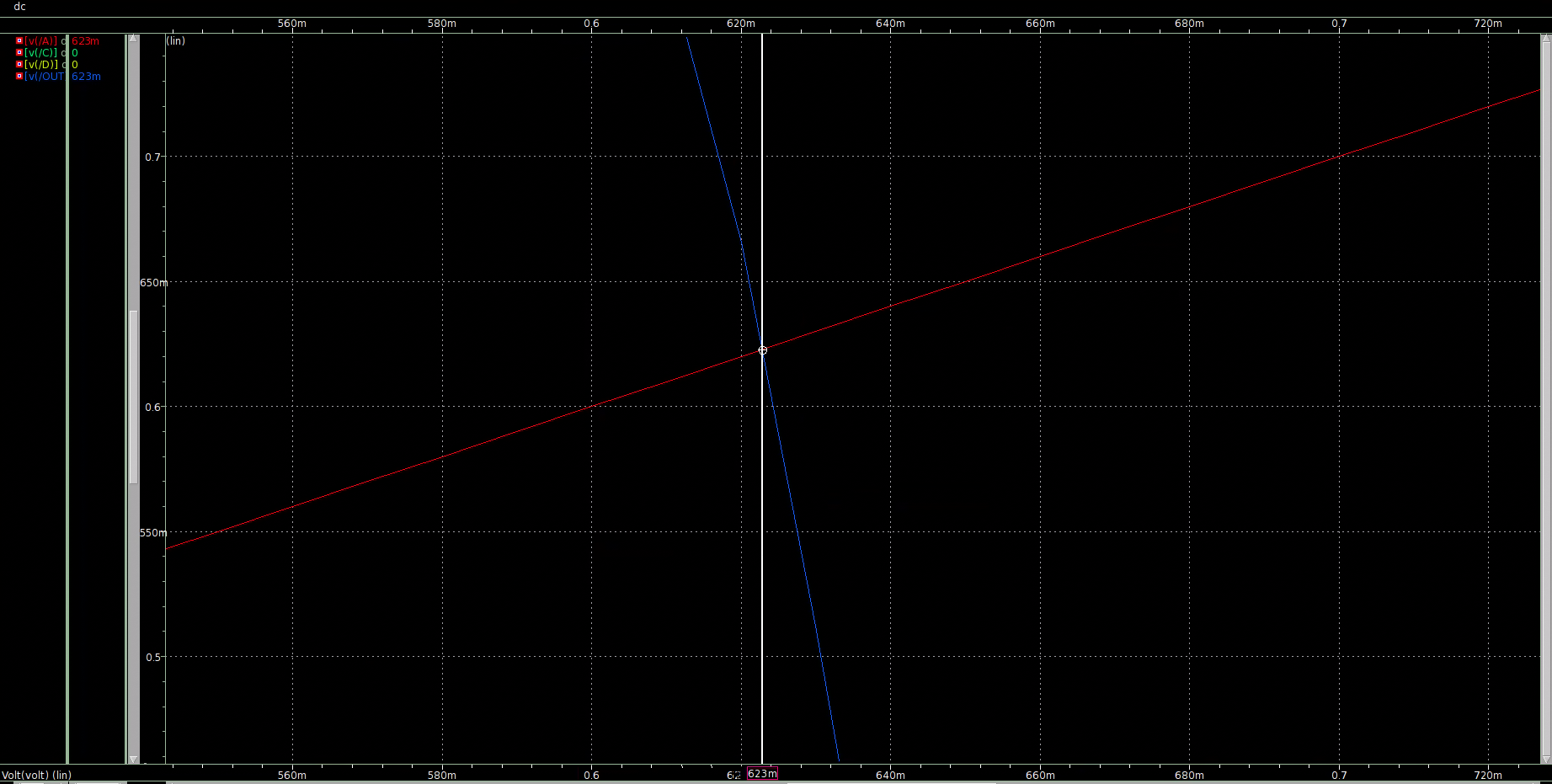


Vm = 731 mV

Inputs A and B Sweep







Vm = 623 mV

Questions:

Part A:

The width for the PMOS and NMOS in the inverter in lab 2 was 1.2um for the PMOS and 0.4 um for the NMOS. Transistors of series is equal to (# of transistors) \* (effective width required), which in this case is (4)\*(1.2) = 4.8 um. Therefore, for the PMOS’s, the width of each PMOS needs to be 4.8 um. For transistors in parallel, the width remains the same, so the width for the NMOS’s are still 0.4 um.

Part C:

Vm values are different each time due to the way how the schematic is formatted. When A is being swept, the value has to go through the entire NOR schematic, since the input A is at the top of the schematic. When B is being passed through, there are fewer transistors to go through. Finally, when both A and B are being swept, there are the fewest amount of transistors to go through.

Conclusion:

Where the input is on the transistor circuit matters as the results can change based on how many transistors that the value has to go through.