## Santa Clara University

## Department of Electrical and Computer Engineering

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ELEN 153 Fall 2020 Problem Set #2

Due: 10-8-2020, Thursday, 12:00 pm

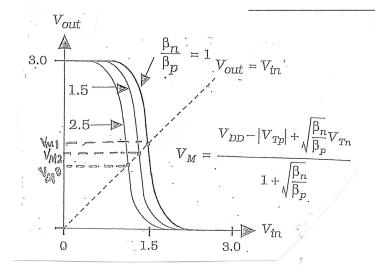
1. A CMOS asymmetrical inverter using power supply of 4.5 V and Channel length = 45 nm is built in a process with the following specification:

nFET : Process transconductance =  $163~(\mu A/V^2)$ ; Threshold voltage = 0.57~V; Width =  $8~\mu m$  pFET : Process transconductance =  $74~(\mu A/V^2)$ ; Threshold voltage = -0.63~V; Width =  $12~\mu m$ 

- a) Calculate Device transconductances of the nFET and the pFET.
- b) Estimate the Midpoint voltage  $V_{\text{M}}$  of the inverter.

2. a) Find the ratio of device transconductances of nFET and pFET needed to obtain a CMOS inverter midpoint voltage to be 2.68 V. The inverter uses a power supply of 5.0 V with nFET Threshold voltage = 0.58 V and pFET Threshold voltage = -0.62 V.

b) In a CMOS process, the Gate oxide thickness and the Channel length of both the nFET and the pFET are kept same. What would be the relative width sizes of the nFET and pFET in the inverter in 2a) if the electron mobility the nFET and hole mobility in the pFET are related by  $\mu_n = 3.47 \ \mu_p$ ?



Dependence of  $V_M$  on the device ratio

$$V_{DD} = 3 \text{ V}$$
  $V_{Tp} = -0.7 \text{ V}$   $V_{Th} = +0.7 \text{ V}$ 

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b) 
$$V_{m} = \frac{V_{DD} - |V_{TP}| + \sqrt{\frac{B_{D}}{B_{P}}} V_{Tn}}{1 + \sqrt{\frac{B_{D}}{B_{P}}}}$$
 
$$V_{DD} = 4.5 \text{ V}$$

$$= \frac{4.5 - (0.63) + \sqrt{\frac{29.93}{19.73}} \cdot 0.57}{14 \sqrt{\frac{29.99}{19.73}}} = 2.06 \text{ V}$$

2) a) 
$$V_{DD} = 5.0 \text{ V}_{Tn} = 0.58 \text{ V}_{Tp} = -0.62 \text{ V}_{m} = 2.68 \text{ V}_{m} = 2.68$$

b) 
$$\frac{\beta_{n}}{\beta_{p}} = \frac{\mu_{n} \aleph_{w} \left(\frac{w_{n}}{k}\right)}{\mu_{p} \aleph_{w} \left(\frac{w_{n}}{k}\right)} = \frac{3.47 \mu_{p} \left(w_{n}\right)}{\mu_{p} \left(w_{p}\right)} = \frac{3.47 (w_{n})}{w_{p}}$$

$$0.655 = \frac{3.43 w_{n}}{w_{p}} \qquad 0.655 w_{p} = 3.47 w_{n}$$

$$W_{p} = 5.300 w_{n}$$