SANTA CLARA UNIVERSITY	ELEN 153	TA: Vinay Krishna vandra@scu.edu
Pre-Lab #1: Circuit Analysis Review		

(1) Carry out a "paper-and-pencil" analysis of the voltage divider circuit given in Figure 1.

Note: Credits will be given only for presented proof of calculation.

(i) What would be the value of Vout, when

(a) R1 >> R0, eg: R1 = 10 MΩ

(b) R1 = R0, eg: R1 = 1 KΩ

(c) R1 << R0, eg: R1 = 1 Ω

(ii) If Vout needs to be close in value to ground which condition (a) or (b) or (c) is suitable?

(iii) If Vout needs to be close to Vdd which condition (a) or (b) or (c) is suitable?

(iv) If Vout needs to be exactly half of Vdd which condition (a) or (b) or (c) is suitable?

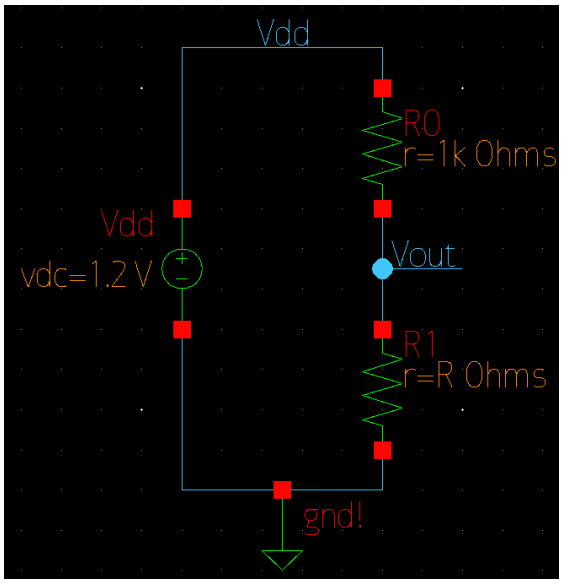

Figure 1

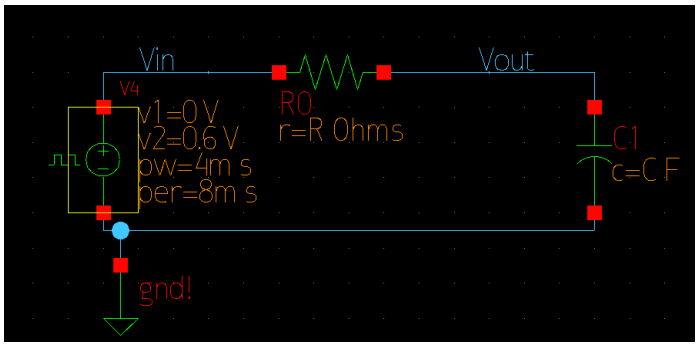

Figure 2

(2) Carry out a "paper-and-pencil" analysis of the RC circuit given in Figure 2.

Assume that Vin switches instantaneously from 0 to Vdd. Vout is also referred as $V_C(t)$

Note: For Vin parameters look for Figure 2. : pw = Pulse Width, per = period. Vin is a Square wave.

(i) Write the charging and discharging equations for $V_C(t)$. Draw the rough sketch for Vin and $V_C(t)$ waveforms with respect to time for the circuit. Assume the initial capacitor voltage is 0V.

(ii) What is the value of $V_C(t)$ when R0 = 1 KΩ and C1 = 1 µF at

(a) t = 4 m.sec

(b) t = 8 m.sec

(iii) Given R0 = 1 KΩ, and C1 = 1 µF. How long will it take for the capacitor to reach 63% of its applied input voltage? Credits will be only given for presented proof of calculation.