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Pre-Lab #2: The CMOS Inverter		

For the MOS devices in 90nm technology use the parameters listed below.

NMOSFET no bias threshold voltage is 0.39 V
PMOSFET no bias threshold voltage is 0.27 V
NMOSFET Process transconductance is 200 µA/V^2
PMOSFET Process transconductance is 60 µA/V^2

Given VDD = 1.2 V, Voltage Input High is 0.8 V, Voltage Input Low is 0.4 V, Voltage Output High is 1.1 V and Voltage Output Low is 0.1 V.

(a) Draw the rough sketch of Voltage Transfer Characteristics (VTC) for this inverter
(b) When Vin = 1.2 V; Define operating region for PMOS and NMOS transistors. Explain why so?
(c) When Vin = 0 V; Define operating region for PMOS and NMOS transistors. Explain why so?
(d) Calculate the logic swing and Noise margins for this inverter?

Note: Logic Swing is difference between output logic levels 1 and 0.
1 can be referred as High and 0 as Low.
Questions b and c will not be credited without valid explanation.