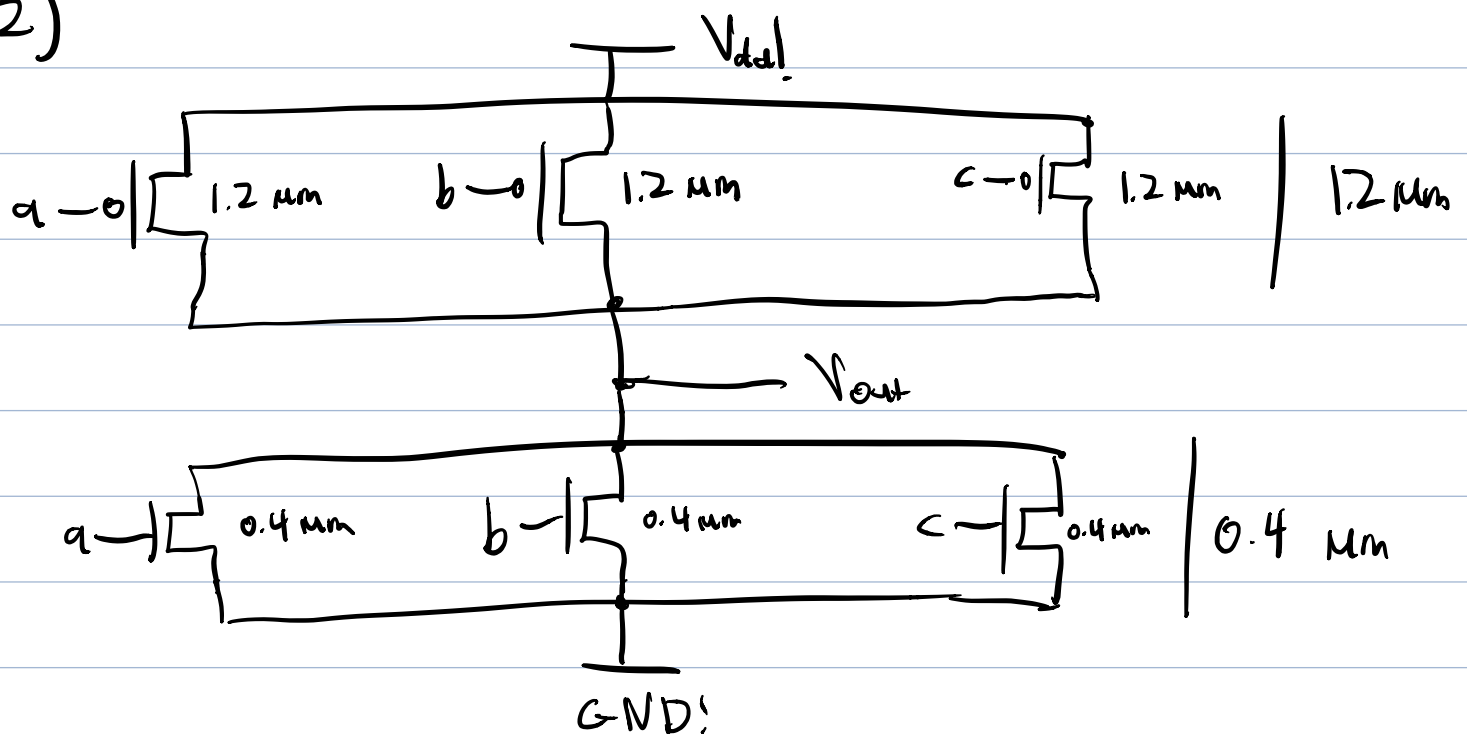


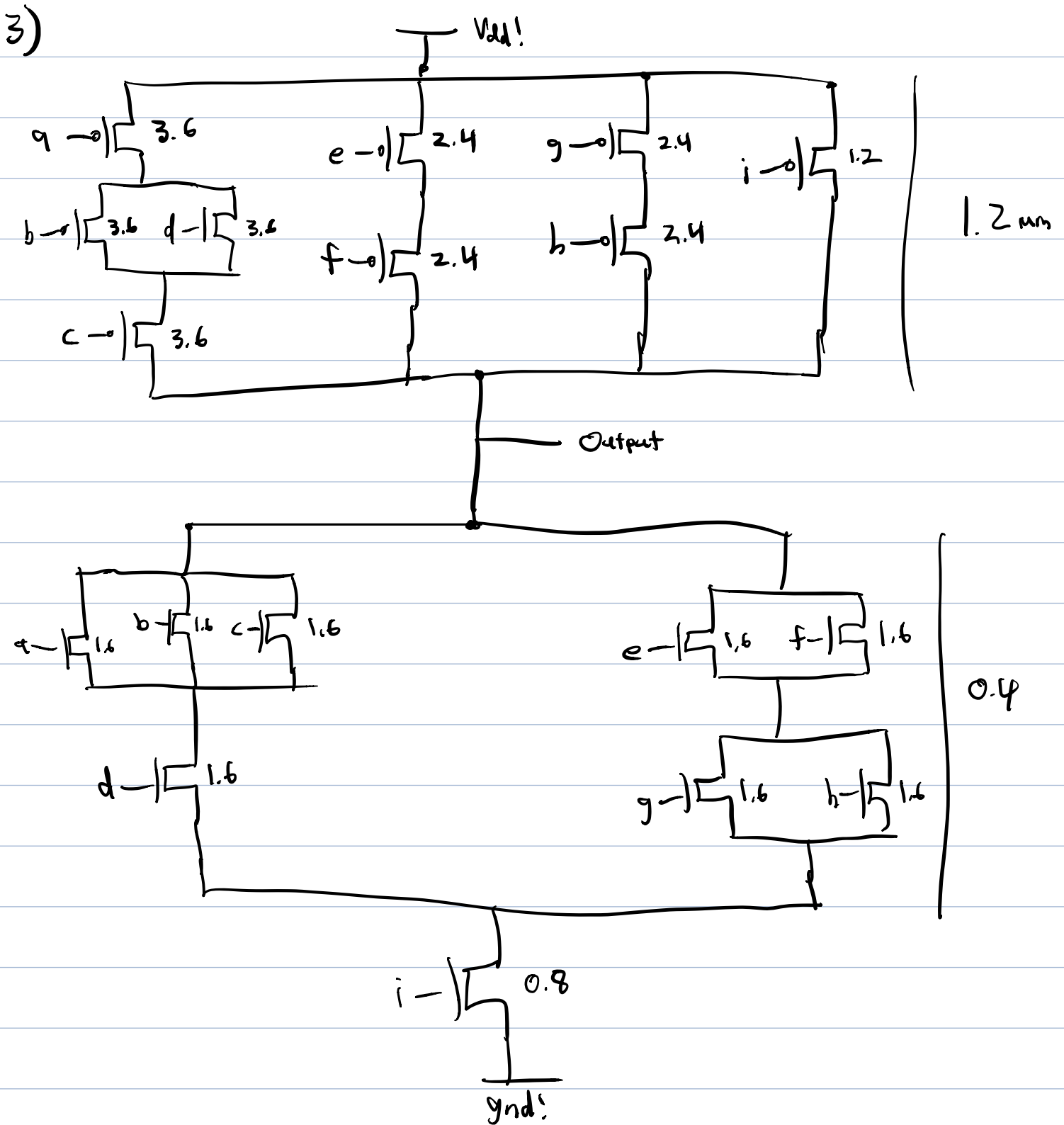
Hand-drawn schematic of a 3-stage CMOS inverter chain. The top input is labeled 'C' with a width of 3.6 μm . The middle input is labeled 'B' with a width of 3.6 μm . The bottom input is labeled 'A' with a width of 3.1 μm . The output of the first stage is labeled 'Output' and has a width of 1.2 μm . The second stage has an input labeled 'A' with a width of 1.2 μm . The third stage has an input labeled 'B' with a width of 1.2 μm . The final output is labeled 'C' with a width of 1.2 μm . The circuit is connected to V_{dd} at the top and GND at the bottom.

$$3(0.4) = 1.2 = w_n$$

2)



All 6 transistors have length $L = 3(0.7) = 2.1 \mu\text{m}$



All 9 transistors have length $L = 9(0.7) = 6.3 \mu m$