VLSI
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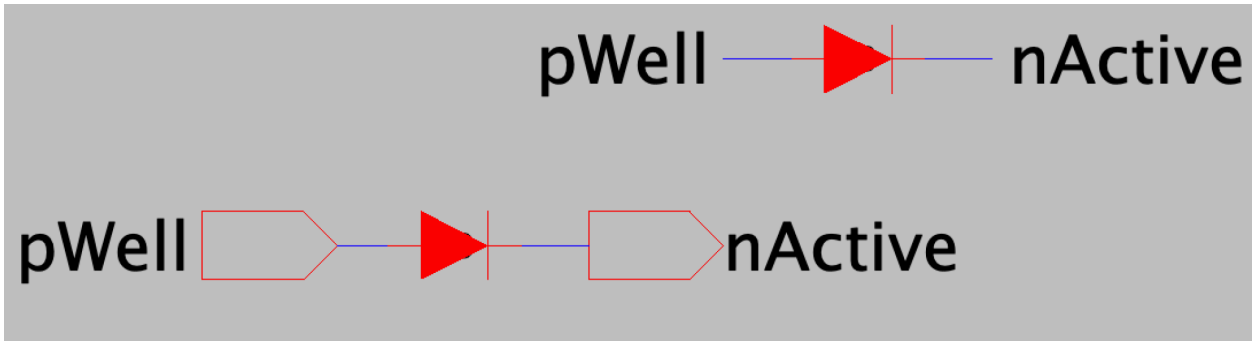
Lab 3: ESD

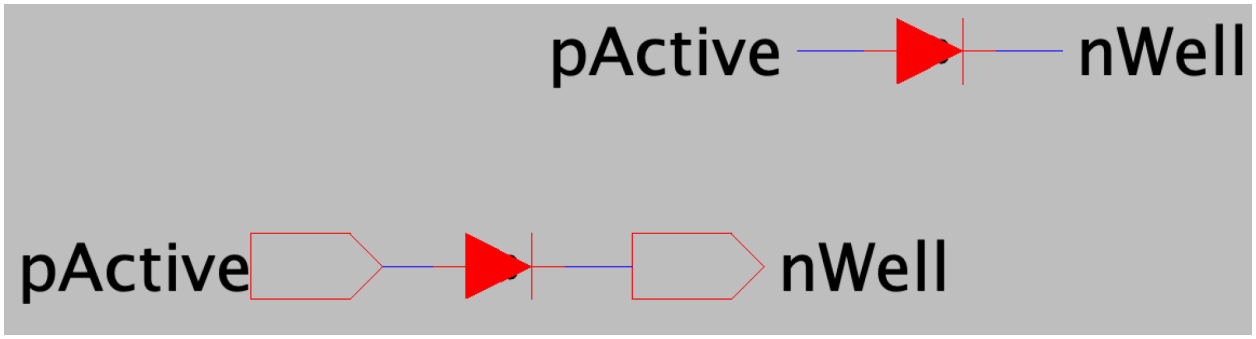
Introduction:

In this lab, I was tasked with designing a die to connect a standard NMOS transistor to the outside world. The primary goal was to create a padframe that not only provides physical connection points but also incorporates a basic ESD protection circuit. To make it, I first designed the fundamental ESD protection components: a pWell-nActive diode and a pActive-nWell diode. These diodes were then used to create a protected pad cell. Finally, I instantiated multiple protected pad cells to build a complete, square padframe and routed the connections from the pads to the terminals of the NMOS transistor placed in the center.

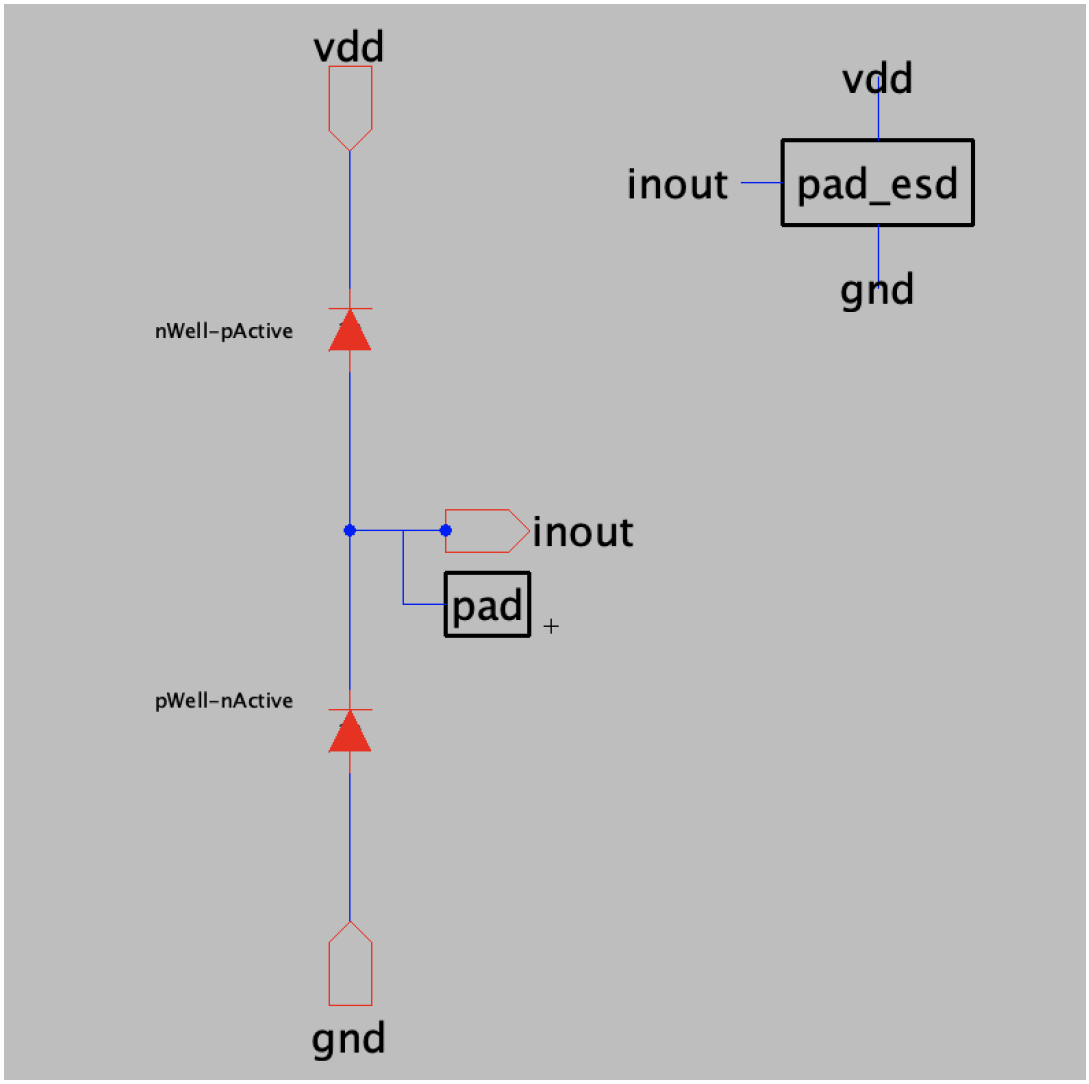
Lab work:
SCHEMATIC

- The schematic of the pWell-nActive and pActive-nWell diodes

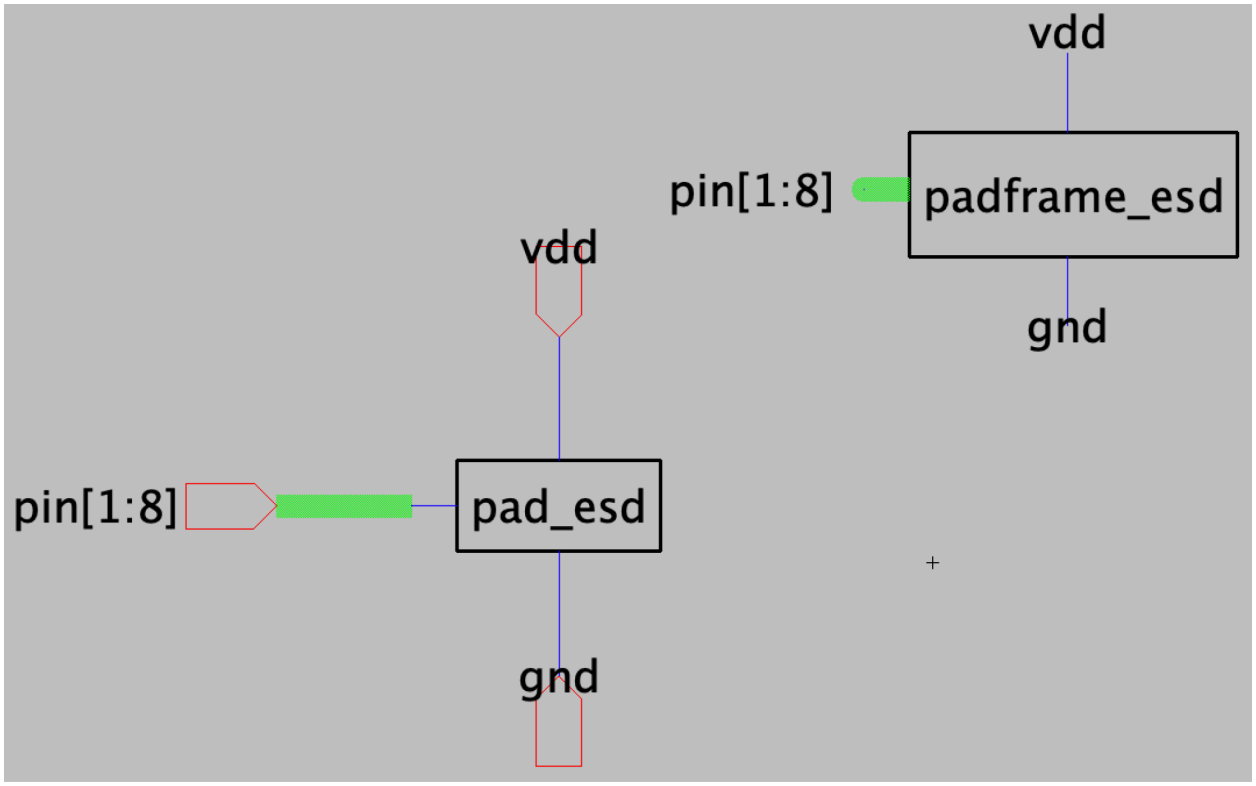




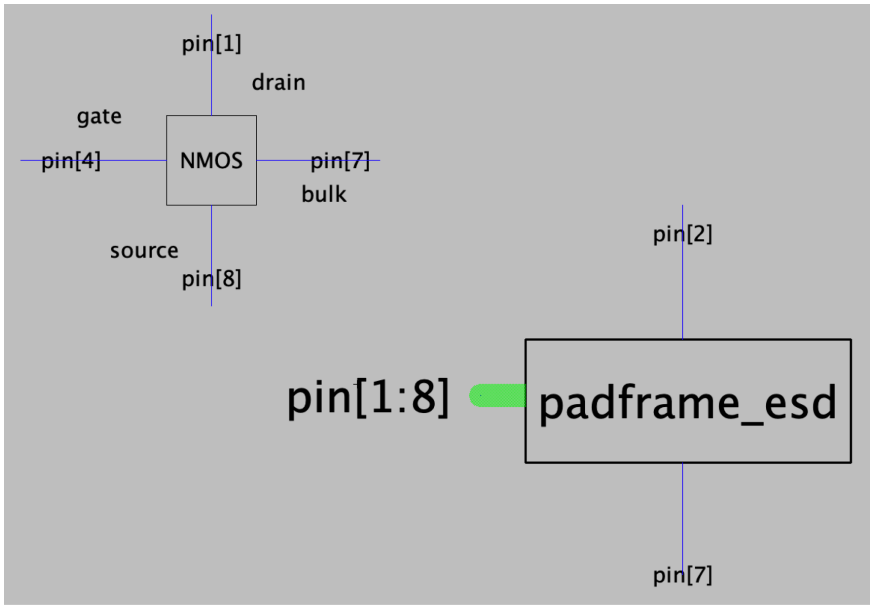
- The schematic of the pad cell with ESD protection



- The schematic of the padframe with the VDD and GND bus connected together. The padframe should be a square and you should design it to have the minimum number of required pad cells to connect all the NMOS Pinouts.



- The schematic of the padframe with the NMOS.

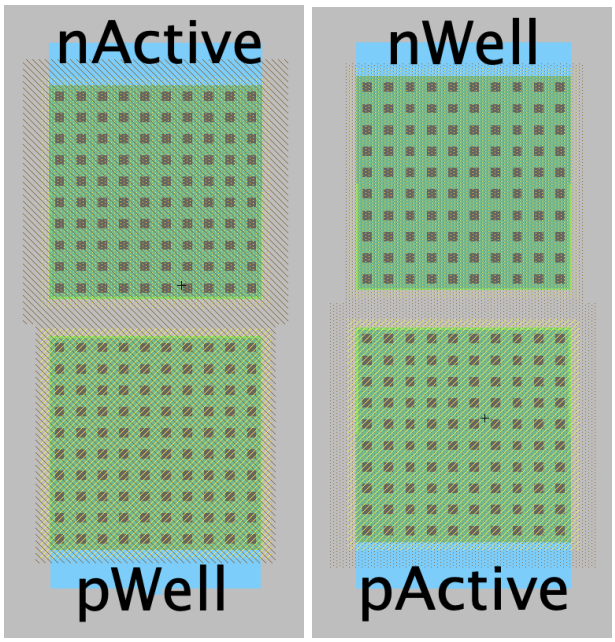


- All necessary explanations to support all the decisions taken during the design of the schematics.

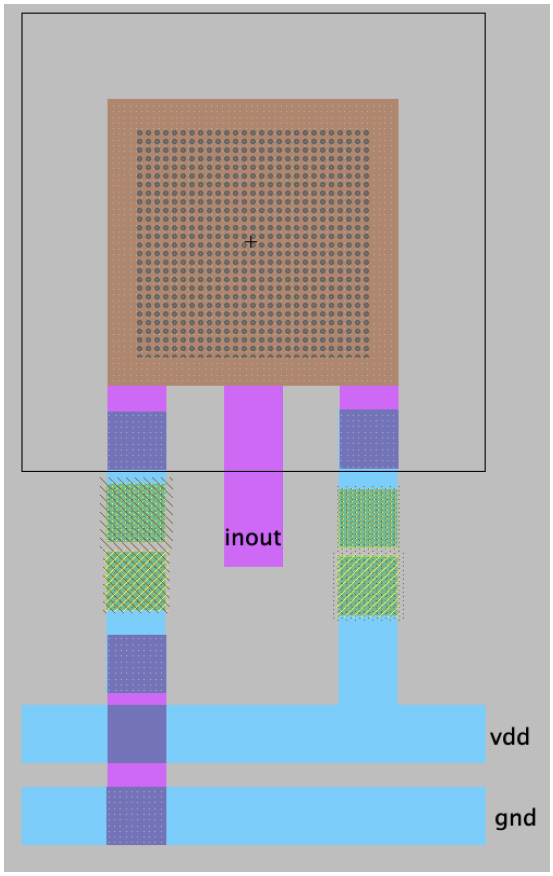
To get the schematics done, I started with the smallest pieces first and built my way up. The whole point of the ESD protection was to use a dual-diode clamp, so I used the nActive-pWell and pActive-nWell cells provided in the tutorial sheet. These are the basic building blocks for the protection circuit. Once I had those, I created a new schematic for the protected pad itself, called pad_esd. There, I connected the pActive-nWell diode between the pad's I/O pin (inout) and VDD, and the pWell-nActive diode between the inout pin and GND. This setup ensures that if a large voltage spike hits the pad, it gets safely redirected to either the VDD or GND rail instead of frying the internal components. After the single pad was designed, I built the full padframe. Even though the NMOS only has four terminals, I used eight pads to make a nice, symmetrical square frame, connecting 4 and leaving the other four hanging. In the final top-level schematic, I just dropped in the NMOS icon and the new padframe_esd icon and connected the NMOS terminals (Drain, Gate, Source, and Bulk) to four of the pads(1,4,7 & 8).

LAYOUT

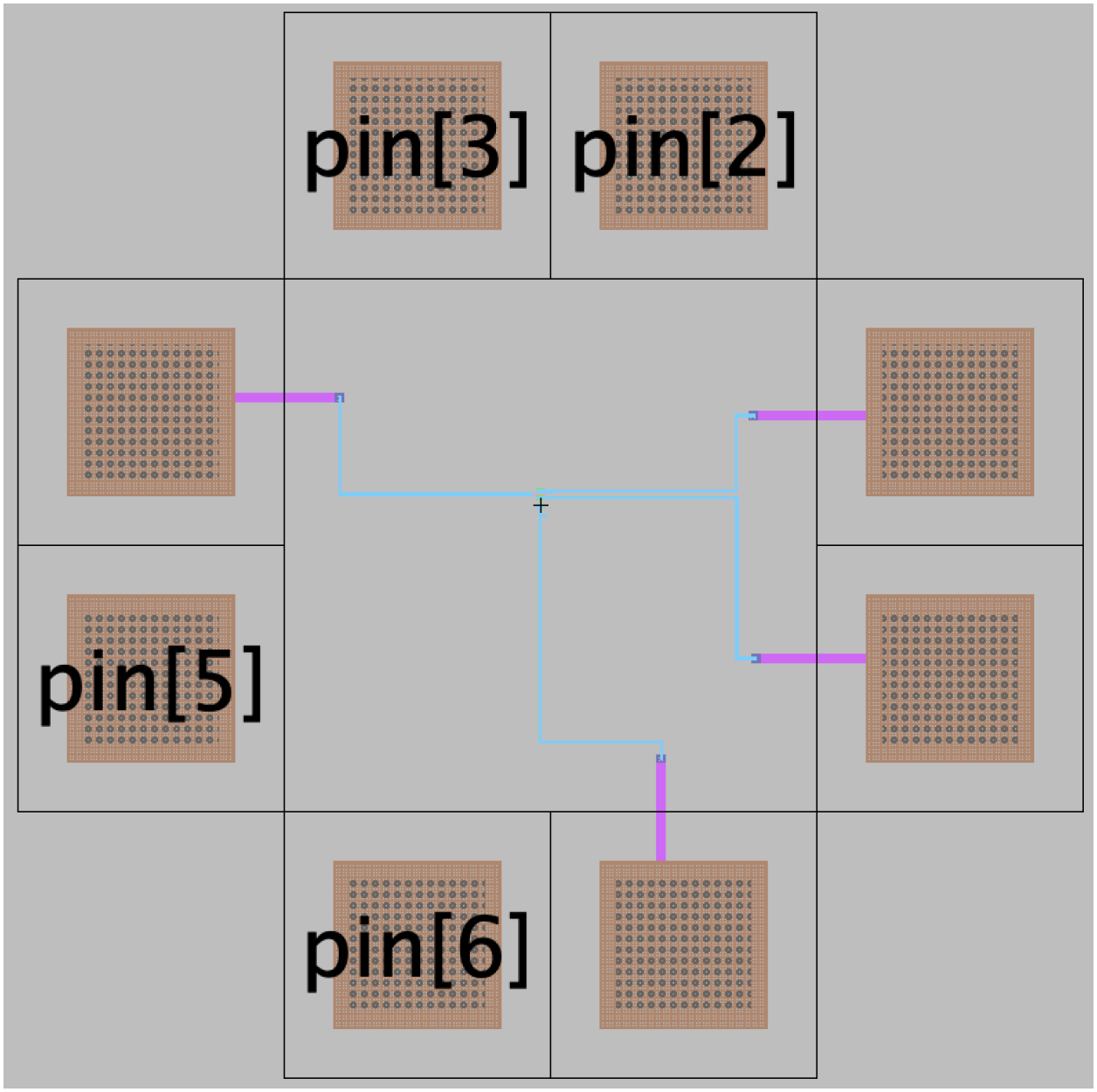
- The layout of the pWell-nActive and pActive-nWell diodes



- The layout of the pad cell with the ESD protection



- The layout of the padframe with the NMOS inside of it.
First photo is of the non-esd pads with the nmos connected, the second is with ESD pads with nmos connected.


pin[3]
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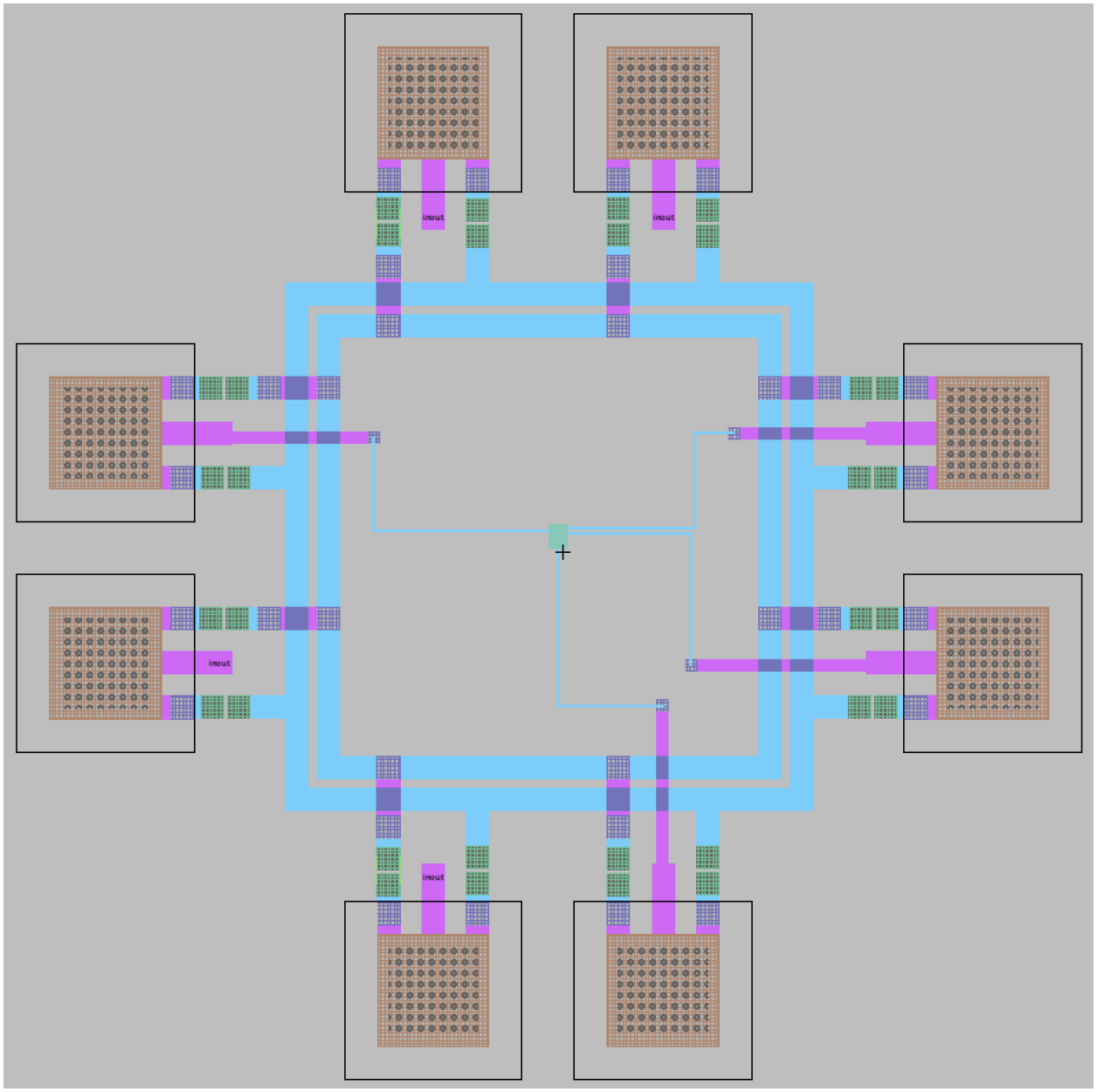
pin[6]



- All necessary explanations to support all the decisions taken during the design of the layout.

The process for making the layout was pretty smooth since it followed the same bottom-up approach as the schematics. I started by laying out the two individual diodes, making sure the active regions and contacts were all correct. Then, I moved on to creating the layout for the complete pad_esd cell. This was mostly about arranging the pieces: I placed the big top-level metal square for the bonding pad, put the two diode layouts I just made underneath it, and then routed the inout connection from the pad down to the diodes. I also ran the VDD and GND metal lines across the bottom of the cell to power the protection circuit, initially the error checker in Electric was all annoying

about these lines. I figured out after clicking around for a while that it was due to me placing the central bridge-metal-2 pin after I created the Metal 1 line from left to right. Placing the metal 1 from the left to the pin then to the right fixed this issue. For the final chip layout, I arranged eight of these pad_esd cells in a square (placing two then using duplicate, rotate and mirror to place the other ones in the correct area. The rings for gnd and vdd were then connected together. After placing the NMOS layout in the center of the frame, the last step was just routing. I carefully drew metal traces from the NMOS terminals out to their assigned pads, using vias where needed to connect the different metal layers, I had to keep these at 25 x 25 to keep from looking too weird but also not too large. I tried to keep the routes as direct as possible to make sure the connections were good.

Conclusion:

Overall this lab wasn't too bad. I felt like it was good practice in making pad frames with ESD and no ESD protection. I felt like it was a good use of the knowledge that we covered in class this week and was a good practice of VLSI tools. There were some parts that were finicky, par for the course with using Electric I guess. There were issues with aligning things especially for the ESD pad components but these were fixed by just nudging things until I could eyeball the alignment to look visually okay and error checker stop bothering me. After a bunch of fiddling I got all the errors to disappear so that's good as well.