

## Lab 4: Inverters

### Introduction:

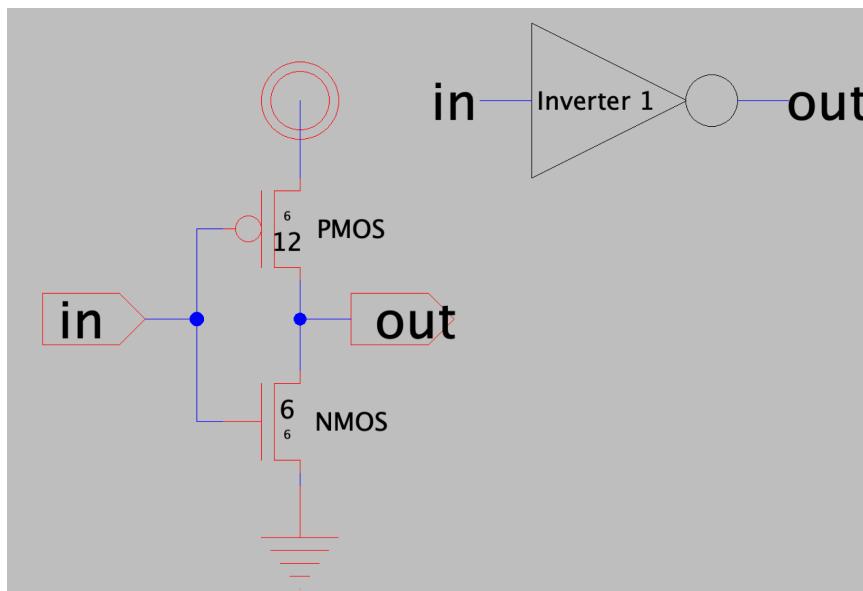
In this lab, I was tasked with designing and analyzing two different CMOS inverters to understand the relationship between transistor sizing, switching thresholds, and drive strength. The primary goal was to create a standard inverter and a larger, high-drive inverter, simulate their behavior under various conditions, and finally create their physical layouts. To do this, I first designed the schematics for both inverters, sizing the PMOS transistors to be wider than the NMOS to balance the rise and fall times. I then performed DC sweeps to find the switching points and transient simulations with varying capacitive loads to observe delay. Lastly, I laid out both cells following standard design practices, ensuring VDD and GND(exports on the bars) ran horizontally at the top and bottom of the cells via Metal 1.

### Lab work:

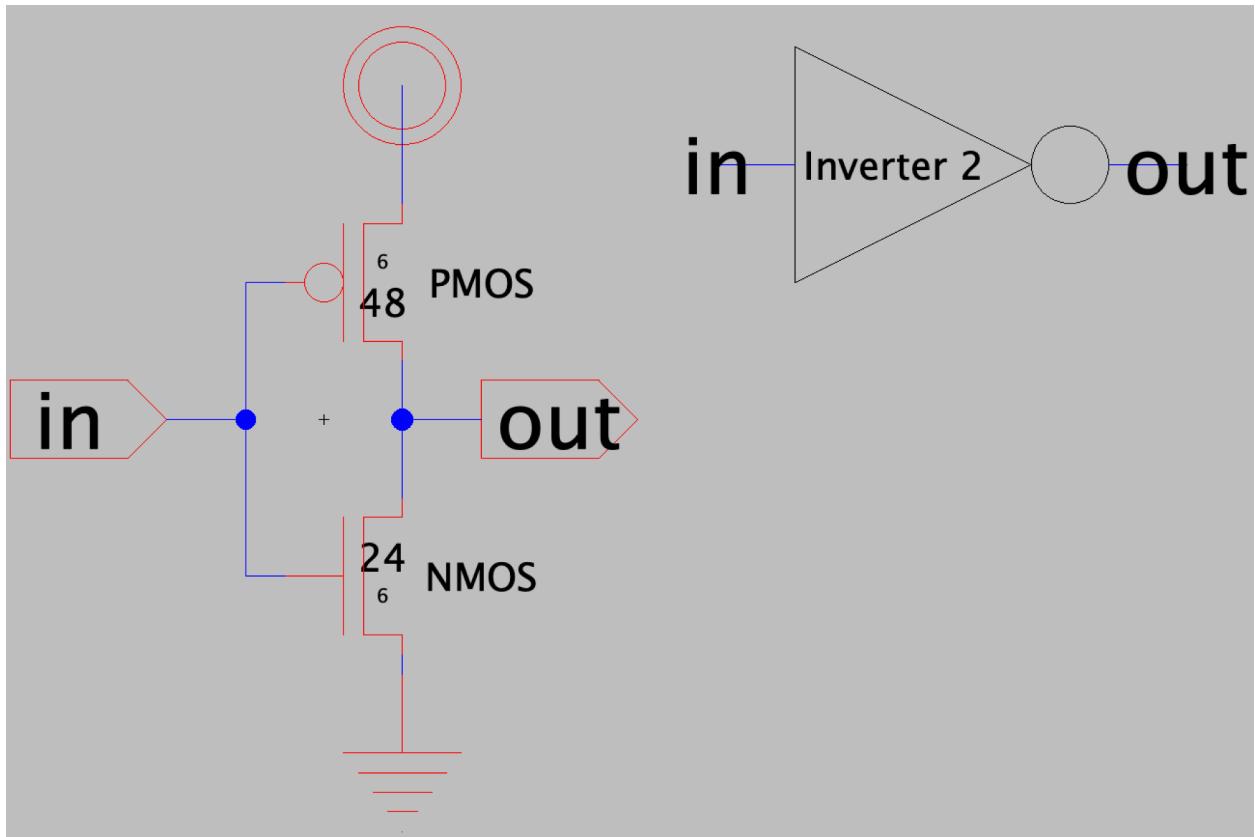
#### SCHEMATIC

- The schematics for the inverters and respective simulations to show the switching point.

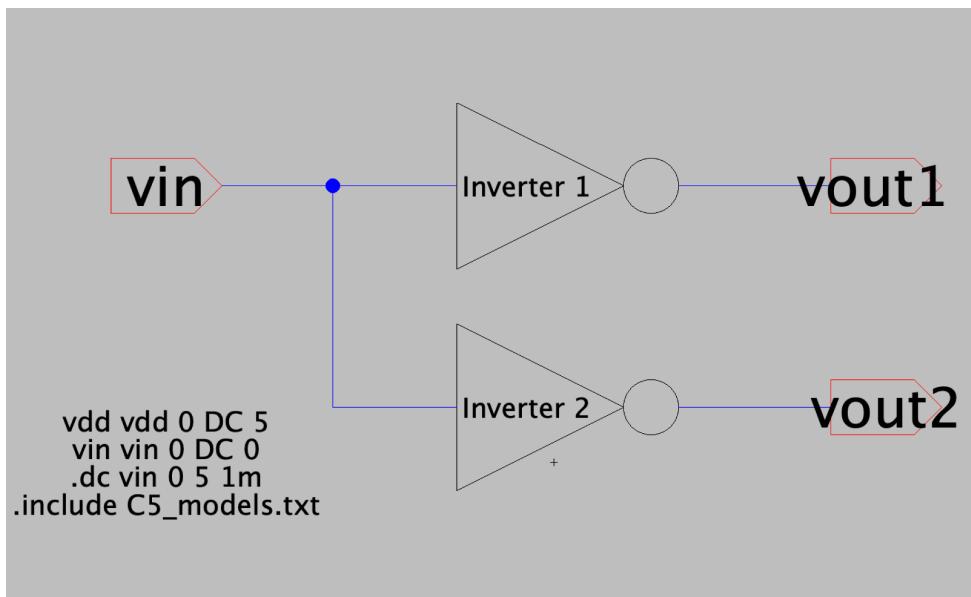
#### Inverter 1: 6 12 pmos, 6 6 nmos



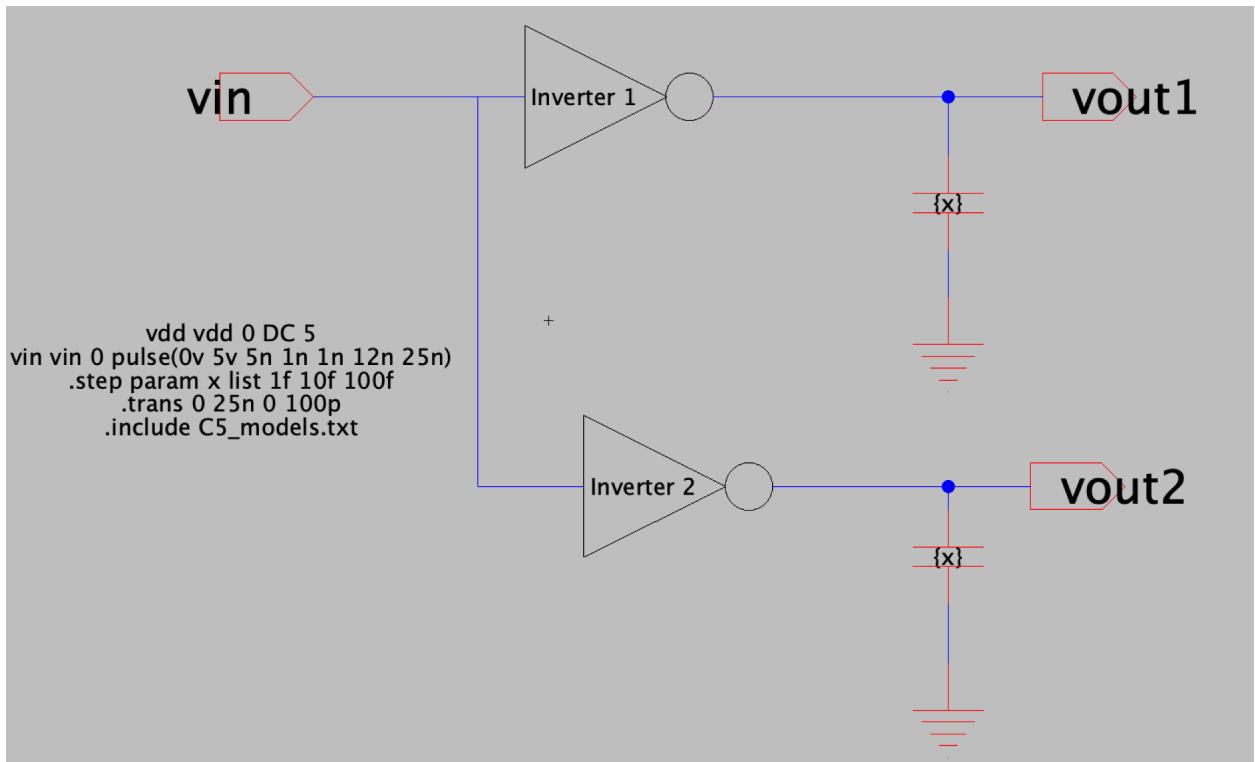
Inverter 2: 6 48 pmos, 24 6 nmos



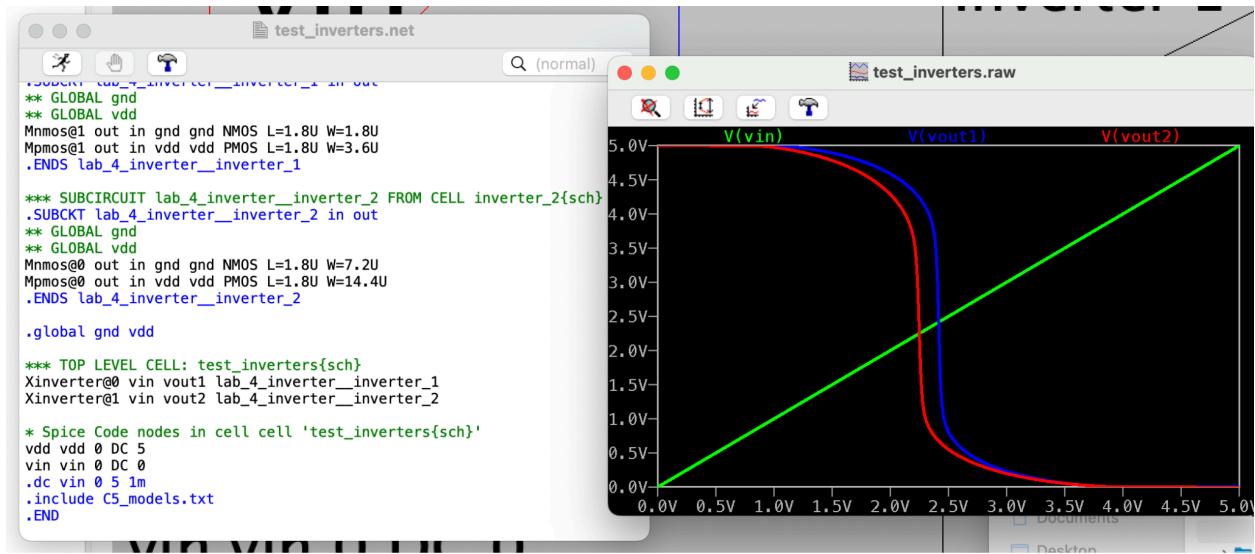
Inverter simulation constant



### Inverter simulation switching load



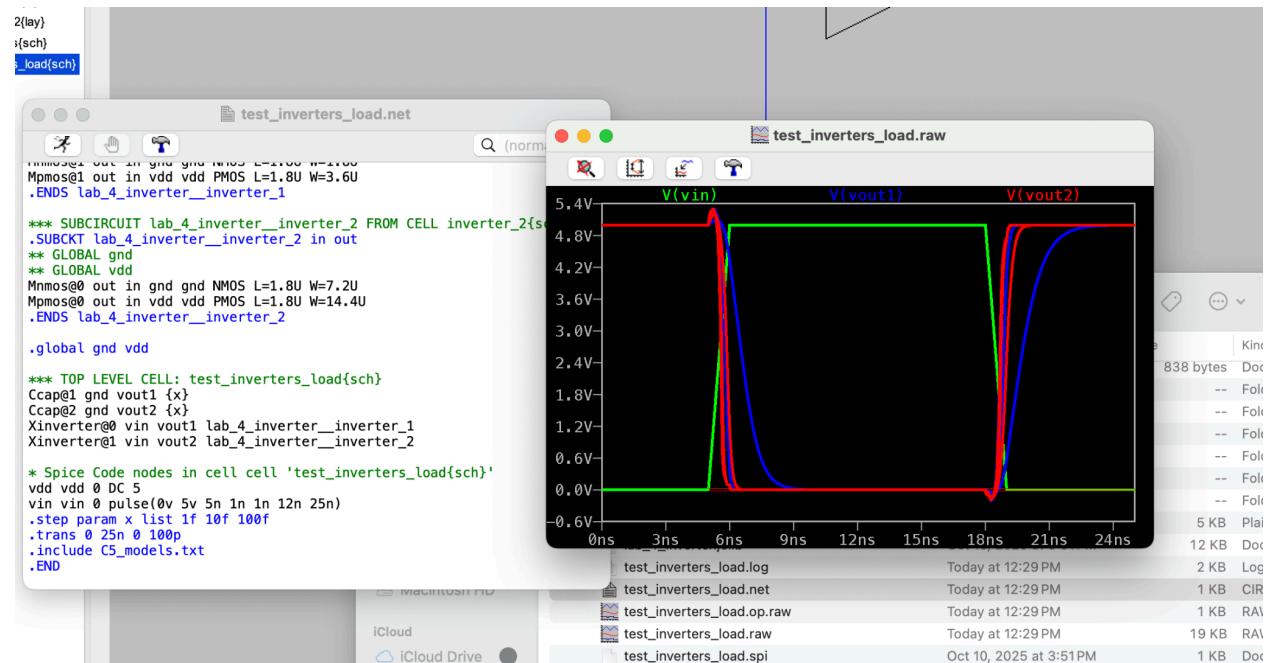
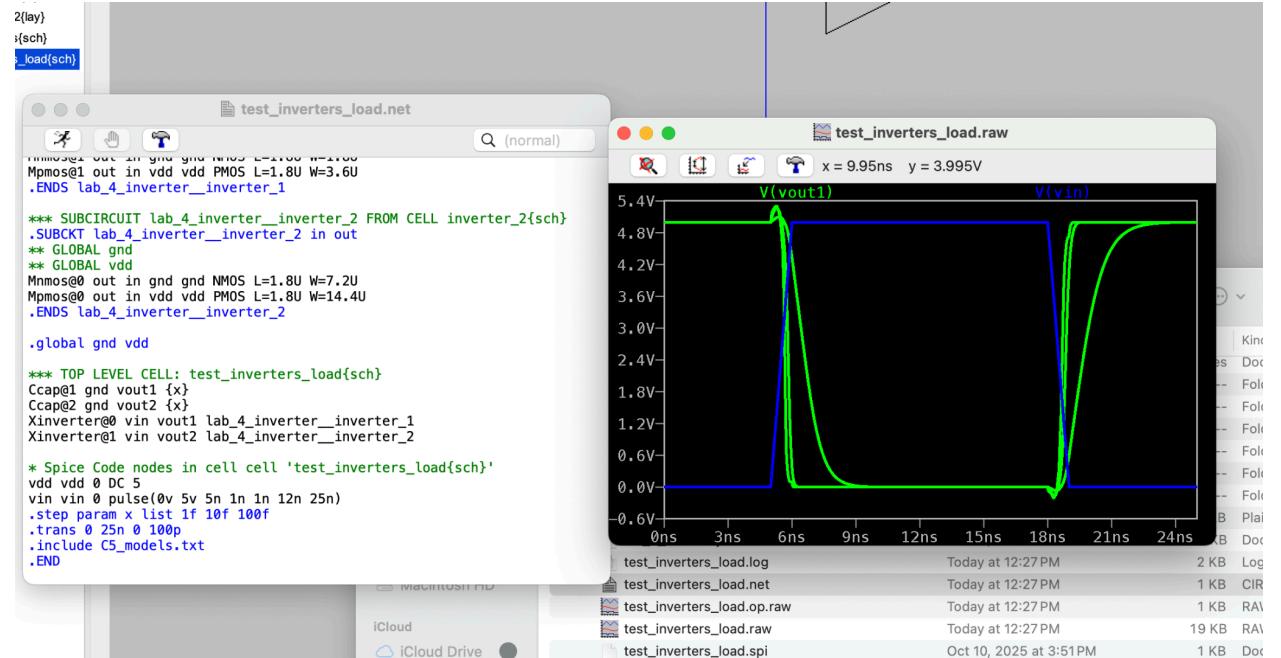
### Simulation no switching load (for verification of functionality)



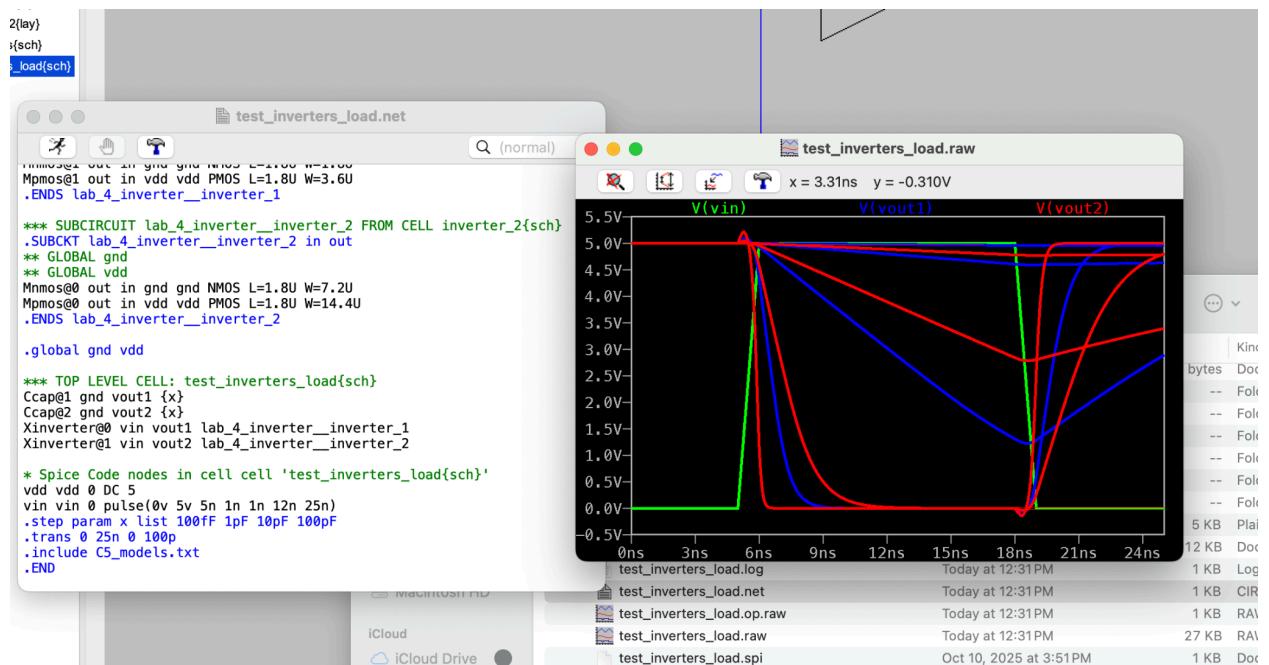
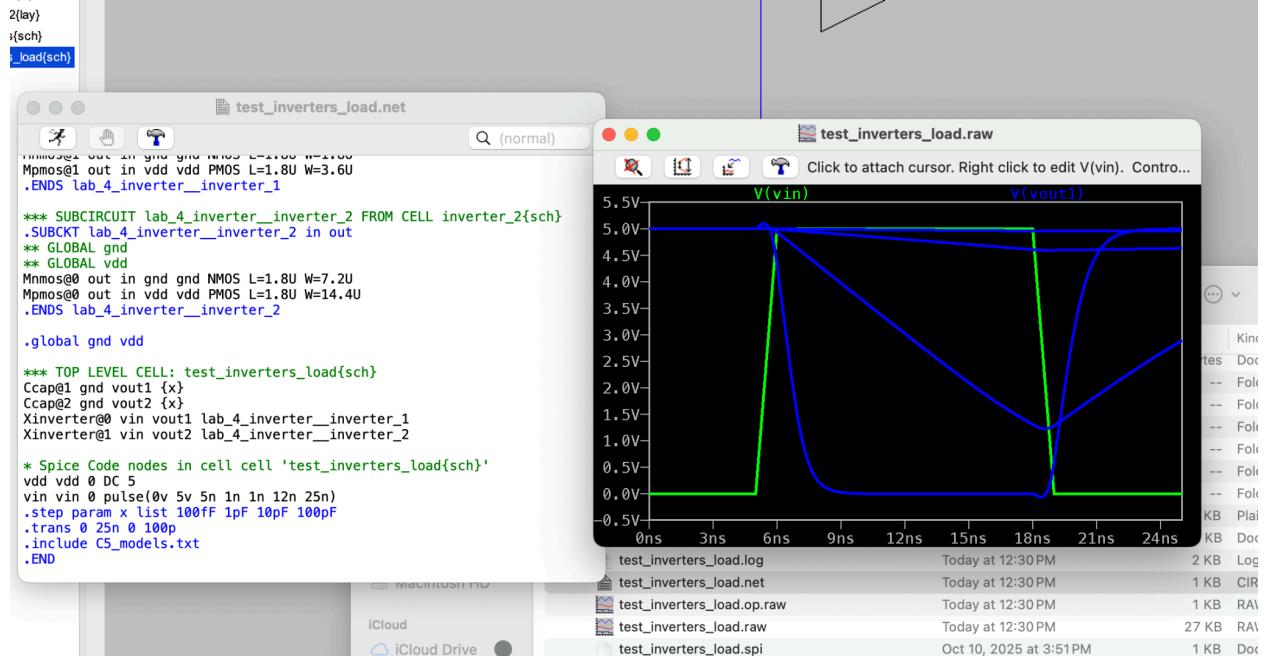
- Apply a pulse waveform to both inverters each driving a 100 fF, 1pF, 10pF,

and 100 pF capacitive load. Comment the results on the report.

## Simulation 1f 10f 100f



## Simulation 100fF 1pF 10pF 100pF



First, the DC sweep simulation showed that both inverters switch right around 2.5V, confirming that the 2:1 PMOS-to-NMOS sizing ratio successfully balanced the logic threshold.

For the transient response, applying the pulse waveform with varying capacitive loads showed a clear difference between the two designs. At lower loads (like 100 fF), both

inverters produced sharp edges with minimal delay. However, as I increased the load to 1pF, 10pF, and finally 100 pF, the rise and fall times became much slower. Inverter 2, with its much wider transistors, has a lower output resistance and demonstrated a significantly higher drive strength. Consequently, it was able to charge and discharge the larger capacitors much faster than Inverter 1, resulting in smaller delays and cleaner logic transitions under heavy loading.

- All necessary explanations to support all the decisions taken during the design of the schematics.

To design the schematics, I aimed to create a balanced inverter where the switching threshold is close to VDD/2 (2.5V). Since the mobility of holes in PMOS is roughly half that of electrons in NMOS, the PMOS needs to be about twice as wide as the NMOS to balance the current drive.

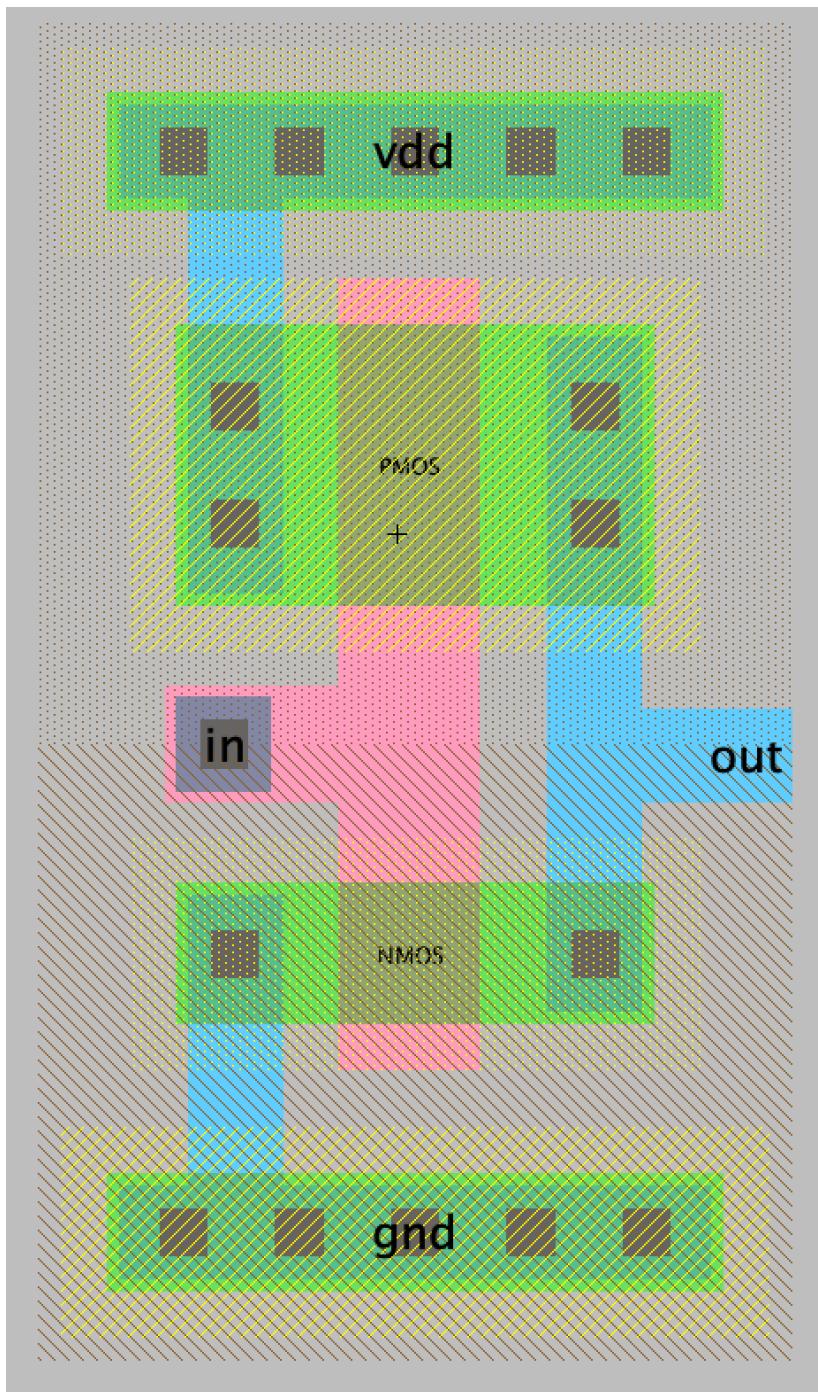
For Inverter 1, I used a total PMOS width of 12 (using a multiplier of m=2 with width=6) and an NMOS width of 6.

For Inverter 2, I wanted a much higher drive strength, so I scaled up the widths while keeping the roughly 2:1 ratio. I used a PMOS width of 48 (m=8, w=6) and an NMOS width of 24 (m=4, w=6). Using multipliers in the schematic makes the eventual layout easier to manage using finger techniques.

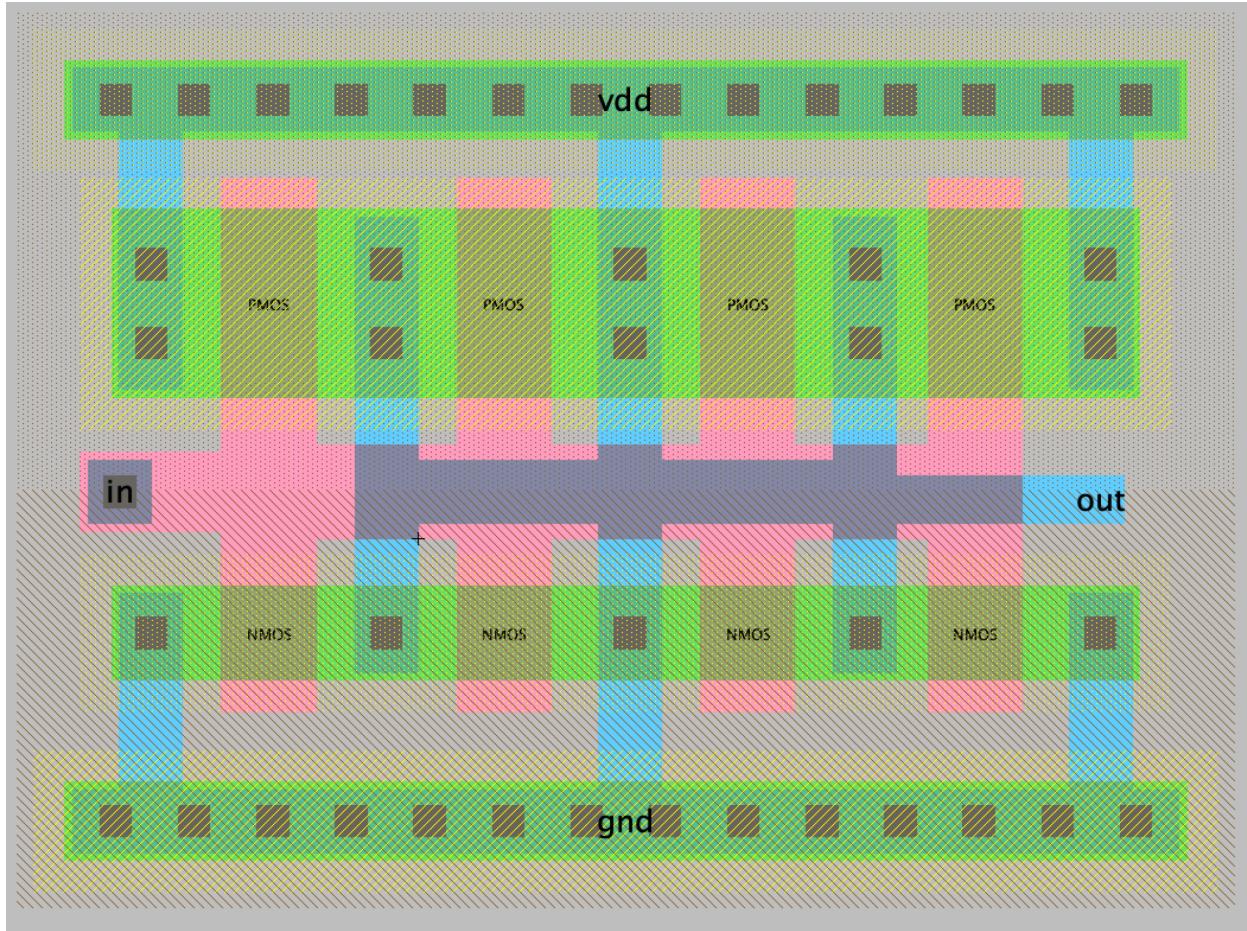
## LAYOUT

- The layouts for the inverters

## Layout inverter 1



## Layout Inverter 2



- The power should run on the top of the cell via metal1 and ground should run on the bottom of the cell also via metal1

**See screenshots above**

- All necessary explanations to support all the decisions taken during the design of the layout

**The process for making the layout followed the schematics. I utilized the multi-finger approach dictated by the multipliers set in the schematics. For Inverter 1, it was pretty simple to arrange the two PMOS fingers and one NMOS finger. For Inverter 2, it was a bit more complex to manage the 8 PMOS and 4 NMOS fingers. I arranged them to share source and drain diffusion areas to save space and reduce parasitic capacitance. I connected all the polysilicon gates together for the input and routed the drains together using Metal 1 for the output. As required, I ran thick Metal 1 rails across the entire top for VDD and the bottom for GND, connecting the sources and substrate taps to them.**

Initially, I had some DRC spacing errors between the poly contacts and the diffusion, but after some nudging and aligning, I got both layouts to be DRC and LVS clean.

#### Conclusion:

Overall, this lab was a good exercise in connecting transistor sizing theories to actual simulation and layout results. I felt it was good practice in using multipliers to scale transistor widths without changing the layout of a single finger too much. At the start I completely blanked on how to make a nmos and pmos (like the part where you put the pAct or nAct next to the p or n transistor, but eventually I remembered what to do. While laying out Inverter 2 with so many fingers was a bit finicky to get everything aligned perfectly for the error checker, seeing the simulation results clearly show how the larger inverter handles big capacitive loads much better than the smaller one made it make sense. If you can see in the screenshot of the layout the NMOS' aren't exactly vertically aligned, but the simulations seem to be correct. After a bit of fiddling with the metal routing to keep the cell compact, I successfully got all schematics, simulations, and layouts completed. And, this time I didn't struggle with the DRC throwing a lot of errors!