

*** State_Table: Circuit_7_State_Table

Page 1

ASSIGN	PS	NS	OUTPUTs*															
		0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1															
		0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1	0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1															
		0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1	0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1															
		0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1															
00	S0	S0 S0 S0 S0 S0 S0 S0 S0 S0 S0 S0 S0 S0 S0 S0 S1 S0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0															
01	S1	S0 S0 S0 S0 S0 S0 S2 S0 S0 S0 S0 S0 S0 S0 S0 S0 S0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0															
10	S2	S0 S0 S0 S0 S0 S0 S0 S0 S0 S0 S0 S3 S0 S0 S0 S0 S0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0															
11	S3	S0 S0 S0 S0 S0 S0 S0 S0 S0 S0 S0 S0 S0 S0 S0 S0 S0	0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0															

* Z

*** State_Table: Circuit_7_State_Table

Page 2

INPUT-VARS

1	1	1	A
1	1	1	B
0	1	1	C
1	0	1	D

0	0	0
0	0	0
0	0	0
0	0	0
