2026 Digital IC Design Homework 1

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| **Functional Simulation Result** | | | | | | |
| Stage 1 | | Pass | Stage 2 | Pass | Stage 3 | Pass |
| **Stage 1** | | | | | | |
| # === Testing Half Adder ===  # PASS: #0 data is correct  # PASS: #1 data is correct  # PASS: #2 data is correct  # PASS: #3 data is correct  # PASS: #4 data is correct  # PASS: #5 data is correct  # PASS: #6 data is correct  # PASS: #7 data is correct  # >>> [HA] TEST PASSED | | | | | | |
| **Stage 2** | | | | | | |
| # === Testing Full Adder ===  # PASS: #0 data is correct  # PASS: #1 data is correct  # PASS: #2 data is correct  # PASS: #3 data is correct  # PASS: #4 data is correct  # PASS: #5 data is correct  # PASS: #6 data is correct  # PASS: #7 data is correct  # >>> [FA] TEST PASSED | | | | | | |
| **Stage 3** | | | | | | |
| # === Testing Ripple Carry Adder ===  # PASS: #0 data is correct  # PASS: #1 data is correct  # PASS: #2 data is correct  # PASS: #3 data is correct  # PASS: #4 data is correct  # PASS: #5 data is correct  # PASS: #6 data is correct  # PASS: #7 data is correct  # PASS: #8 data is correct  # PASS: #9 data is correct  # >>> [RCA] TEST PASSED | | | | | | |
| **Description of your design** | | | | | | |
| Half Adder: （輸入輸出皆為1 bit）   * 輸入：x, y 輸出：s (sum), c (carry) * c和 s 是先進行concatenation ，再接收x+y 得到的結果   Full Adder: （輸入輸出皆為1 bit）   * 輸入：x, y, c\_in (carry in) 輸出：s (sum), c\_out (carry out) * 此模組調用HA 先將x+y得到s1, c\_out1。在用一個HA將x+y 相加的結果s1與c\_in 相加得到總和s和c1。將c1和c2進行or得到最終的carry bit c。   Ripple Carry Adder:   * 輸入：x, y, c\_in (carry in) 輸出：s (sum), c\_out (carry out) * Carry wire 連接每一個位輸出的carry，並將c\_in 連接上carry[0] 方便在generate 中調用。利用generate 中的for迴圈來生成四個full adder 建立ripple carry adder 結構進行多位數加法。最後將carry[4] assign 給c\_out | | | | | | |