计算机组成小测3答案

I. Choose true or false

a. It is possible to execute the stages of the single cycle data path in parallel to speed up execution of a single instruction. (F)

b. Single-cycle processors are typically limited in their clock speed due to the necessity of completing the longest instruction within one clock cycle, which affects the overall performance scalability of the processor. (T)

c. Branch prediction in a RISC-V pipelined processor improves performance by guessing the outcome of branch instructions and pre-fetching the next instructions, but it introduces a risk of performance degradation due to branch mispredictions. (T)

d. The execution time of a single instruction in a pipelined RISC-V processor is faster than in a single-cycle processor because it moves through multiple stages more quickly. (F)

II. Choose the best answer

a. Processor P1 has CPIs of 1, 2, 3, and 4 for instructions A, B, C, and D. What is the global CPI for the program (10% A, 20% B, 30% C, 40% D)? (C)

A: 2　　B: 2.5　　C: 3　　D：3.5

b. "results≧0 indicates an overflow" can be applied to which of the following two operations? (D)

A: Operation 1: A+B, A≧0, B≧0; Operation 2: A-B, A≧0, B＜0.

B: Operation 1: A+B, A＜0, B＜0; Operation 2: A-B, A≧0, B＜0.

C: Operation 1: A+B, A≧0, B≧0; Operation 2: A-B, A＜0, B≧0.

D: Operation 1: A+B, A＜0, B＜0; Operation 2: A-B, A＜0, B≧0

III. Calculation

1. Assume that the logic blocks used to implement a processor's datapath have the following latencies:

Clk-to-Q	RegFile Read	Register Setup	MUX	Adder	ALU	ImmGen	I/D-Mem Read	D-Mem Setup	Single Gate
5ns	35ns	20ns	15ns	20ns	90ns	40ns	300ns	200ns	5ns

"Clk-to-Q" is the time needed after the rising clock edge for the new register value to appear on the output. This value applies to the PC only. **"Register setup"** is the amount of time a register's data input must be stable before the rising edge of the clock. This value applies to both the PC and Register File. **"D-Mem Setup"** is the amount of time a D-Mem's data input must be stable before the rising edge of the clock. This value applies to the D-Mem. Ignore the delay of the control signal.

Quesition: Calculate the latency of add, addi, lw, sw, beq, jal.

Answer:

add: 5ns + 300ns + 35ns + 15ns + 90ns + 15ns + 20ns = 480ns

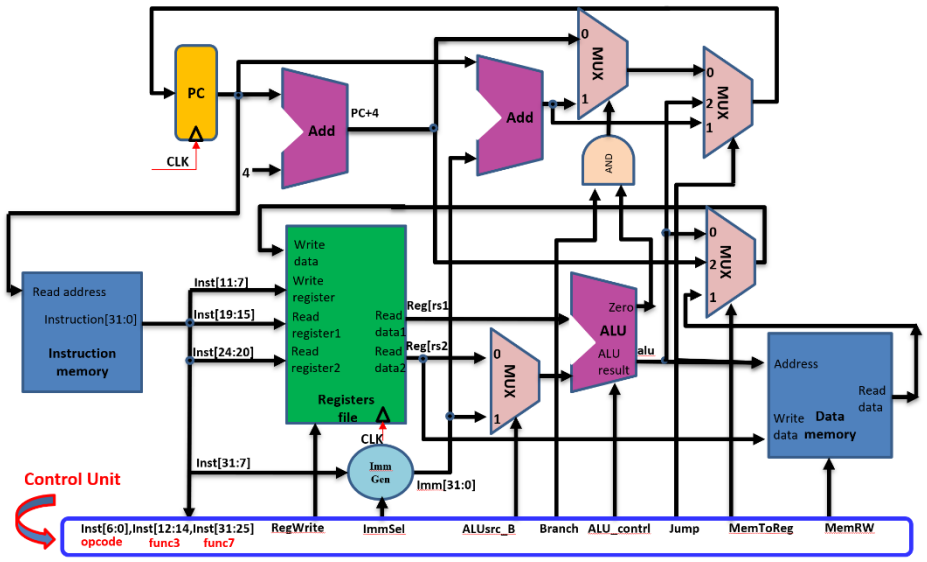
addi: 5ns + 300ns + 40ns (Imm) + 15ns (Mux) + 90ns + 15ns + 20ns = 485ns

lw: 5ns + 300ns + 40ns + 15ns + 90ns + 300ns + 15ns + 20ns = 785ns

sw: 5ns + 300ns + 40ns + 15ns + 90ns + 200ns = 650ns

beq: 5ns + 300ns + 35ns + 15ns + 90ns + 5ns + 15ns (Mux) + 15ns (Mux) + 20ns = 500ns

jal: 5ns + 300ns + 40ns + 20ns (Adder) + 15ns (Mux) + 20ns = 400ns



2. Write the RISC-V assembly code that creates the 64-bit constant 0x0123456789ABCDEF and stores that value to register x10.

Answer:

```
lui x10, 0x01234
addi x10, x10, 0x568
slli x10, x10, 32
lui x5, 0x89ABD
addi x5, x5, 0xDEF
add x10, x10, x5
```

IV. Pipeline

3. Consider a five-stage pipeline CPU. It does not consider structural hazard and allows the register file to be read and written in the same clock cycle. Branches are resolved in the ID Stage.

And consider the following code segment:

```
Loop:   lw x1, 0(x4)        Instr. 1/7
        lw x2, 400(x4)      Instr. 2
        add x3, x1, x2      Instr. 3
        sw x3, 0(x4)        Instr. 4
        addi x4, x4, -4     Instr. 5
        bne x0, x4, loop    Instr. 6
```

Pipeline execution table sample:

Instr	Clock Cycle					
	1	**2**	**3**	**4**	**5**	**...**
1	F	D	E	M	W	
...		F	...	...	...	...

a) No forwarding mechanism is used. Show a pipeline execution diagram for the first loop iteration.

b) Forwarding mechanism is used. Show a pipeline execution diagram for the first loop iteration.

Answer:

a) 采用 stall 机制对冒险进行处理,寄存器堆采用下降沿写

Instr	Clock Cycle															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	F	D	E	M	W											
2		F	D	E	M	W										
3			F	D	D	D	E	M	W							
4				F	F	F	D	D	D	E	M	W				
5							F	F	F	D	E	M	W			
6										F	D	D	D	E	M	W

b) 采用 forwarding 解决数据冒险，但发生 load-use 情况时仍需要 stall 进行指令的暂停。跳转指令在 ID 阶段进行处理，**不考虑对 ID 阶段支持 forwarding**，所有的 forwarding 均在 EX 阶段。指令 7 表示 bnez 跳转的指令“lw x1, 0(x4)”,处理控制冒险仅需考虑对 IF 到 ID 阶段寄存器是否施加 flush 信号。

Instr	Clock Cycle														
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	F	D	E	M	W										
2		F	D	E	M	W									
3			F	D	D	E	M	W							
4				F	F	D	E	M	W						
5						F	D	E	M	W					
6							F	D	D	D	E	M	W		
7											F	D	E	M	W