计算机组成小测1答案

1.Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (classes A, B, C, and D).
P1 with a clock rate of 4 GHz and CPIs of 3, 5, 4, and 4, and P2 with a clock rate of 2.5 GHz and CPIs of 1, 3, 3, and 3. Given a program with a dynamic instruction count of 2.0×10^6 instructions divided into classes as follows: 10% class A, 20% class B, 40% class C, and 30% class D.

a. What is the **global CPI** for each implementation?
b. Find the **execution time** required in both cases.

a. P1: 4.1 P2: 2.8
b. P1: 2.05×10^{-3} s P2: 2.24×10^{-3} s

2. Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 2.5 GHz clock rate and a CPI of 2. P2 has a 1.8 GHz clock rate and a CPI of 1.2. P3 has a 5.75 GHz clock rate and has a CPI of 2.3.

a. Which processor has the highest performance expressed **in instructions per second**?
(The calculation process needs to be given)
b. We are trying to reduce the execution time by 40%, but this leads to an increase of 50% in the CPI. What **clock rate** should we have to get this time reduction for each processor?

a. IPS = f / CPI P1: 1.25×10^9 P2: 1.5×10^9 P3: 2.5×10^9
b. $f_{new} = 2.5f_{old}$ f1: 6.25 GHz f2: 4.5 GHz f3: 14.375 GHz

3. P1 has a clock rate of 4 GHz, average CPI of 0.8, and requires the execution of 5.0×10^9 instructions. P2 has a clock rate of 3 GHz, an average CPI of 0.75, and requires the execution of 1.0×10^9 instructions.

a. Find the **execution time** required in both processors.

b. What is the **MIPS** (millions of instructions per second) for each processor?

a. P1 : 1s P2 : 0.25s

b. MIPS = f / (CPI × 10^6)

P1 : 5000 P2 : 4000

4. Use IEEE 754 to represent single-precision floating-point numbers. The results should be presented in hexadecimal.

Sign	Exponent	Fraction
1 bit	8 bits	23 bits

e.g. 2 → 0 10000000 00000000000000000000000 → 0x40000000

1) -3.5 2) 2024.0 3) 0.3

1) 0xC0600000 2) 0x44FD0000 3) 0x3E99999A