Ruiyang Chou

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Education Background

University of California, Santa Barbara(UCSB), Santa Barbara, USA 2024/9-2025/6

- Exchange student in the department of Electrical and Computer Engineering
- Core Courses: Tensor computation; VLSI project design

Southwest Jiaotong University (SWJTU), Chengdu, China 2021/9-2024/8

- Bachelor of Engineering in Electronic Science and Technology (with an emphasis on microelectronics technology)
- GPA: 3.52/4.0
- The Second Prize Scholarship（29/245 in 2021）
- Core Courses: Fundamentals of Digital Integrated Circuit Analysis and Design(93); Signals and Systems(90); Fundamentals of Analog Integrated Circuit Analysis and Design (90); Microwave Integrated Circuit (89);

Publication

Lin, W., Zhou, R., & Di, Z.* (2024). Design and Optimization of Chip Defect Detection Model Based on YOLOv3. *School of Information Science and Technology, Southwest Jiaotong University, Chengdu 611756, China*. Early Release Online on 2024-05-07.

Research Experience

FPGA-Accelerated Low-Precision Tensorized Transformer Training System, Santa Barbara, USA 2024/ 9-present

Advisor: Zheng Zhang, Professor in Electrical & Computer Engineering, UCSB

- Developed a low-precision tensorized Transformer training system on FPGA, utilizing an FP16 matrix-multiplication framework as the baseline to support tensor-tensor contraction
- Collaborated to integrate tensor operations with a Transformer training framework, optimizing contraction sequences and maximizing hardware parallelism for efficient training.
- explore FP8 and FP6 implementations for reduced precision, conducting simulations to validate performance and energy savings, aiming to extend low-precision hardware capabilities for AI model training.

RISC-V CPU Design using Cadence Virtuoso, Santa Barbara, USA 2024/9 – 2024/12

Advisor: Bongjin Kim, Professor in Electrical & Computer Engineering, UCSB

- Designed a pipelined RISC-V CPU in Verilog with a multi-stage pipeline to improve instruction throughput and overall CPU efficiency.
- Developed all supporting digital circuits for the CPU pipeline architecture, including ALU, control units, and memory blocks, using Cadence Virtuoso for schematic design and simulation.
- Conducted extensive performance testing and verification to ensure timing accuracy, resource efficiency, and operational stability, achieving successful simulation and integration of the CPU in a VLSI environment.

IoT Design: Voice Impairment Assistance System Based on ESP32, Chengdu, China 2024/4-2024/9

Advisor: Xing Ding, Assistant Researcher at the School of Information Science and Technology, SWJTU

- Developed a speech impairment assistance system on a microcontroller (ESP32-S3).
- Implemented a two-way voice communication system using MQTT.
- Used a piezoelectric sensor to replace a regular microphone, reducing noise in noisy environments for clearer voice transmission.

Chip Defect Detection System Design on edge device, Chengdu, China 2023/4-2023/9

Undergraduate Research Assistant; Advisor: ZhixiongDi, professor at the School of Information Science and Technology, SWJTU

- Implemented a chip defect detection system and an intelligent management system with user interface on a embeded device.
- Trained neural network models for chip defect recognition and deployed the model on PYNQ platform.
- The project achieved third place in the national awards, showcasing its innovative approach to enhancing functionality within limited hardware constraints.

MathorCup College Mathematical Modeling Challenge, Chengdu, China 2023/4

Advisor: Wang Lu, professor at the School of Mathematics, SWJTU

- Developed a multi-objective model to enhance parcel flow, route count, and workload efficiency in response to disruptions like site closures or transport route halts in the logistics network.
- Created a logistics-based road multi-objective planning model, utilizing the simulated annealing algorithm to optimize the volume of road transportation.
- Employed the Monte Carlo algorithm for random attacks, assessing and comparing the robustness of the original logistics network against the network with newly added sites.

Skills and Others

Language: Chinese (Native); English (Fluent)

Programming Skills: Proficient in C, C++, Verilog, Python, Matlab, STM32 programming (ARM Cortex-M microcontroller development), Espressif development tools

Tools: Cadence Virtuoso, Keil, STM32CubeMX, Synopsys DC Compiler

Hobbies: Swimming, Badminton, Cycling, Singing