

# Ruiyang Zhou

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## Education

### University of California, Santa Barbara

Santa Barbara, USA

Exchange Student in the Department of Electrical and Computer Engineering

Sep 2024 - Jun 2025

Core Courses: Tensor Computation; VLSI Project Design

### Southwest Jiaotong University

Chengdu, China

Bachelor of Engineering in Electronic Science and Technology

Sep 2021 – Aug 2024

Average: 87.88/100

GPA: 3.52/4.0;

Relevant Coursework: Fundamentals of Digital Integrated Circuit Analysis and Design (93); Signals and Systems (90); Fundamentals of Analog Integrated Circuit Analysis and Design (90); Microwave Integrated Circuit (89)

## Publication

Lin, W., Zhou, R., & Di, Z.\* (2024). Design and Optimization of Chip Defect Detection Model Based on YOLOv3. *School of Information Science and Technology, Southwest Jiaotong University, Chengdu 611756, China*. [Early Release Online](#) on 2024-05-07.

## Research Experience

### FPGA-Accelerated Low-Precision Tensorized Transformer Training System

Santa Barbara, USA

Advisor: Zheng Zhang, Professor in Electrical & Computer Engineering

Sep 2024 - Present

- Developed a low-precision tensorized Transformer training system on FPGA, utilizing an FP16 matrix-multiplication framework as the baseline to support tensor-tensor contraction
- Collaborated on integrating tensor operations into a Transformer training framework, optimizing contraction sequences and maximizing hardware parallelism to enhance training efficiency.
- Explored FP16 and FP8 implementations for reduced precision, conducting simulations to validate performance and energy savings, with the goal of extending low-precision hardware capabilities for AI model training.

### RISC-V CPU Design

Santa Barbara, USA

Advisor: Bongjin Kim, Professor in Electrical & Computer Engineering

Sep 2024 – Dec 2024

- Designed a pipelined RISC-V CPU in Verilog, incorporating a multi-stage pipeline to improve instruction throughput and overall CPU efficiency.
- Developed supporting digital circuits for the CPU pipeline architecture, including the ALU, control units, and memory blocks, utilizing Cadence Virtuoso for schematic design and simulation.
- Conducted extensive performance testing and verification to ensure timing accuracy, resource efficiency, and operational stability, achieving successful simulation and integration of the CPU within a VLSI environment.

### IoT Design: Voice Impairment Assistance System Based on ESP32

Chengdu, China

Advisor: Xing Ding, Assistant Researcher, Information Science & Technology

Apr 2024 – Sep 2024

- Designed and developed a speech impairment assistance system on a microcontroller (ESP32-S3).
- Implemented a two-way voice communication system using MQTT for seamless data transmission.

- Integrated a piezoelectric sensor as a microphone alternative, reducing environmental noise for clearer voice transmission.

### **Chip Defect Detection System Design on Edge Device**

Chengdu, China

*Advisor: ZhixiongDi, Professor of Information Science & Technology*

Apr 2023 – Sep 2023

- Implemented a chip defect detection and intelligent management systems with user interface on an embedded device.
- Trained neural network models for chip defect recognition and successfully deployed them on the PYNQ platform.
- Achieved third place in the national competition, demonstrating an innovative approach to enhancing functionality within limited hardware constraints.

### **MathorCup College Mathematical Modeling Challenge**

Chengdu, China

*Advisor: Wang Lu, Professor at School of Mathematics*

Apr 2023

- Developed a multi-objective model to optimize parcel flow, route count, and workload efficiency, addressing disruptions such as site closures or transport route halts within the logistics network.
- Created a logistics road multi-objective planning model, utilizing the simulated annealing algorithm to enhance road transportation volume and efficiency.
- Employed the Monte Carlo algorithm to simulate random attacks, evaluating the robustness of the original logistics network against an enhanced network with newly added sites.

### **Skills & Interests**

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**Language:** Chinese (Native), English (Fluent)

**Programming Skills:** C, C++, Verilog, Python, Matlab, STM32 Programming (ARM Cortex-M Microcontroller Development), Espressif Development Tools

**Tools:** Cadence Virtuoso, Keil, STM32CubeMX, Synopsys DC Compiler, Vivado, Quartus

**Hobbies:** Badminton, Swimming, Cycling, Singing